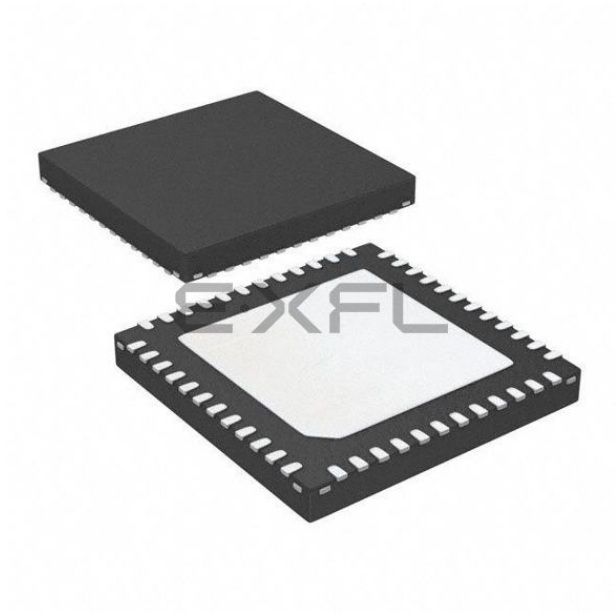
Renesas Electronics America Inc - R7FS124773A01CNE#AC1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 14x14b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs124773a01cne-ac1

Ultra-low power 32-MHz Arm® Cortex®-M0+ microcontroller, 128-KB code flash memory, 16-KB SRAM, Capacitive Touch Sensing Unit, 14-bit A/D Converter, 12-bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M0+ Core
- Armv6-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, BPU, CoreSight™ MTB-M0+
- CoreSight Debug Port: SW-DP

■ Memory
- 128-KB code flash memory
- 4-KB data flash memory (100,000 erase/write cycles)
- Up to 16-KB SRAM
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN)

■ Analog
- 14-Bit A/D Converter (ADC14)
- 12-Bit D/A Converter (DAC12)
- Low-Power Analog Comparator (ACMPLP) × 2
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-Bit (GPT32)
- General PWM Timer 16-Bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- SRAM Parity Error Check
- Flash Area Protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) Calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO Readback Level Detection
- Register Write Protection
- Main Oscillator Stop Detection

■ System and Power Management
- Low-power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection with voltage settings

■ Security and Encryption
- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Independent watchdog timer OCO (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 51 input/output pins
  - Up to 3 CMOS input
  - Up to 48 CMOS input/output
    - Up to 6 input/output 5 V tolerant
    - Up to 16 pins high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = –40°C to +85°C
  - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
- Ta = –40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

Based on the energy-efficient Arm Cortex®-M0+ core, the MCU is particularly well suited for cost-sensitive and low-power applications with the following features:

- 128-KB code flash memory
- 16-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M0+	• Maximum operating frequency: up to 32 MHz • Arm Cortex-M0+: - Revision: r0p1-00rel0 - Armv6-M architecture profile - Single-cycle integer multiplier. • SysTick timer - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 128 KB code flash memory. See section 37, Flash Memory in User's Manual.
Data flash memory	4 KB data flash memory. See section 37, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with even parity bit. See section 36, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes in User's Manual.
Reset	9 types of resets: • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • Software reset. See section 5, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual.

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
On-chip debug	SWDIO	I/O	Serial Wire debug Data Input/Output pin.
	SWCLK	Input	Serial Wire Clock pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Maskable interrupt request pins.
GPT	GTETRGA, GTETRGB	Input	External trigger input pin.
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, Output Compare, or PWM output pin.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable.
	AGTIO0, AGTIO1	I/O	External event input and pulse output.
	AGTO0, AGTO1	Output	Pulse output.
	AGTOA0, AGTOA1	Output	Output compare match A output.
	AGTOB0, AGTOB1	Output	Output compare match B output.
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock.

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC).
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC).
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI).
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI).
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI).
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low.
IIC	SCL0, SCL1	I/O	Input/output pins for clock.
	SDA0, SDA1	I/O	Input/output pins for data.
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master.
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection.
CAN	CRX0	Input	Receive data.
	CTX0	Output	Transmit data.
USBFS	VSS_USB	Input	Ground pins.
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator.
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
ADC14	AN000 to AN010, AN016 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DA0	Output	Output pins for the analog signals to be processed by the D/A converter.

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs		HMI	
LQFP64, QFN64	LQFP48	QFN48	QFN40	LGA36			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI	ADC14	DAC12, ACMPLP	CTSU	Interrupt
35	27	27	23	D5		P110		GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/SS0_C/RXD9_B/MISO9_B/SCL9_B		MISOB_B		VCOUT	TS11	IRQ3
36	28	28	24	D6		P111			GTIOC3A_A			SCK0_C/SCK9_B		RSPCKB_B			TS12	IRQ4
37	29	29	25	C6		P112			GTIOC3B_A			TXD0_C/MOSI0_C/SDA0_C					TSCAP_C	
38	-	-	-	-		P113												
39	30	30	-	-	VCC													
40	31	31	-	-	VSS													
41	-	-	-	-		P107			GTIOC0A_B									KR07
42	-	-	-	-		P106			GTIOC0B_B					SSLA3_A				KR06
43	-	-	-	-		P105		GTETRGA_C						SSLA2_A				KR05/IRQ0
44	32	32	26	-		P104		GTETRGB_B				RXD0_C/MISO0_C/SCL0_C		SSLA1_A			TS13	KR04/IRQ1
45	33	33	27	C3		P103		GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/SS0_A		SSLA0_A	AN019	CMPREF1	TS14	KR03
46	34	34	28	C4		P102	AGTO0	GTOWLO_A	GTIOC2B_A		CRX0_C	SCK0_A		RSPCKA_A	AN020/ADTRG0_A	CMPIN1	TS15	KR02
47	35	35	29	C5		P101	AGTEE0	GTETRGB_A	GTIOC5A_A			TXD0_A/MOSI0_A/SDA0_A/CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	AN021	CMPREF0	TS16	KR01/IRQ1
48	36	36	30	B6		P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A			RXD0_A/MISO0_A/SCL0_A/SCK1_A	SCL1_B	MISOA_A	AN022	CMPIN0	TS26	KR00/IRQ2
49	37	37	-	-		P500	AGTOA0	GTIU_B	GTIOC2A_B						AN016		TS27	
50	-	-	-	-		P501	AGTOB0	GTIV_B	GTIOC2B_B						AN017			
51	-	-	-	-		P502		GTIW_B	GTIOC3B_B						AN018			
52	38	38	31	A6		P015									AN010		TS28	IRQ7
53	39	39	32	A5		P014									AN009	DA0		
54	40	40	33	B5		P013									AN008			
55	41	41	34	B4		P012									AN007			
56	42	42	35	A4	AVCC0													
57	43	43	36	A3	AVSS0													
58	44	44	37	B3	VREFL0	P011									AN006		TS31	
59	45	45	38	A2	VREFH0	P010									AN005		TS30	
60	-	-	-	-		P004									AN004		TS25	IRQ3
61	-	-	-	-		P003									AN003		TS24	
62	46	46	-	-		P002									AN002		TS23	IRQ2
63	47	47	39	-		P001									AN001		TS22	IRQ7
64	48	48	40	B2		P000									AN000		TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

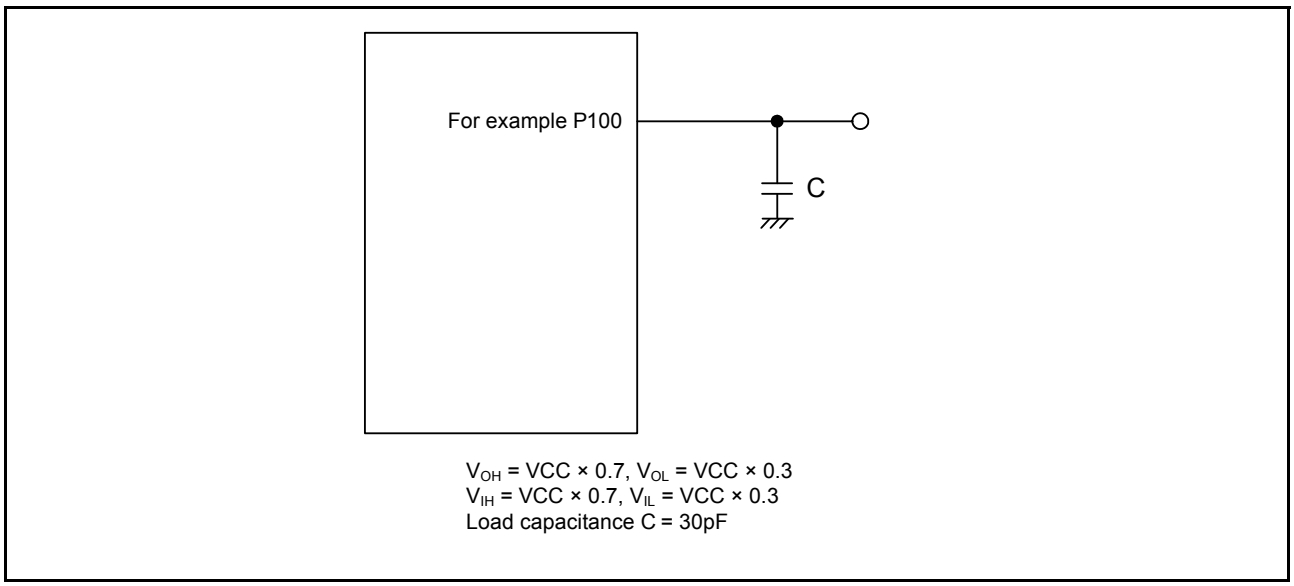


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pins to meet your conditions.

Each function pin used for the same function must select the same drive ability. If I/O drive ability of each function is mixed, the AC specification of the function is not guaranteed.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.7 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = 4.0 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA
			V_{OL}	-	-	1.0		I_{OL} = 20 mA
	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.8	-			I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.8	-			I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.8	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive*5	V_{OH}	VCC – 0.8	-	-		I_{OH} = –4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for Ports P200, P214, and P215, which are input ports.
Note 5. Except for P212, P213.

Table 2.8 I/O V_{OH}, V_{OL} (2)
Conditions: VCC = AVCC0 = 2.7 to 4.0 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1, *2		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	Ports P408, P409*2, *3		V_{OH}	VCC – 1.0	-	-		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P000 to P004 P010 to P015	Low drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC – 0.5	-	-		I_{OH} = –1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive*5	V_{OH}	VCC – 0.5	-	-		I_{OH} = –2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 8 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for Ports P200, P214, P215, which are input ports.
Note 5. Except for P212, P213.

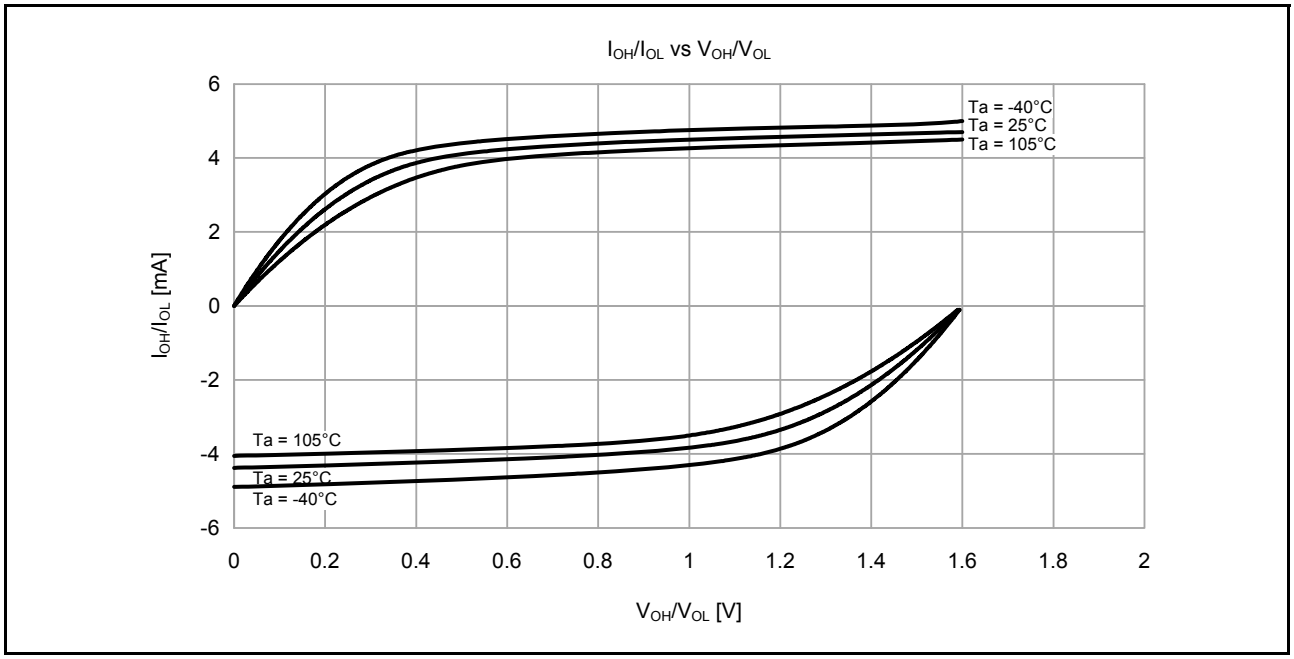


Figure 2.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data)**

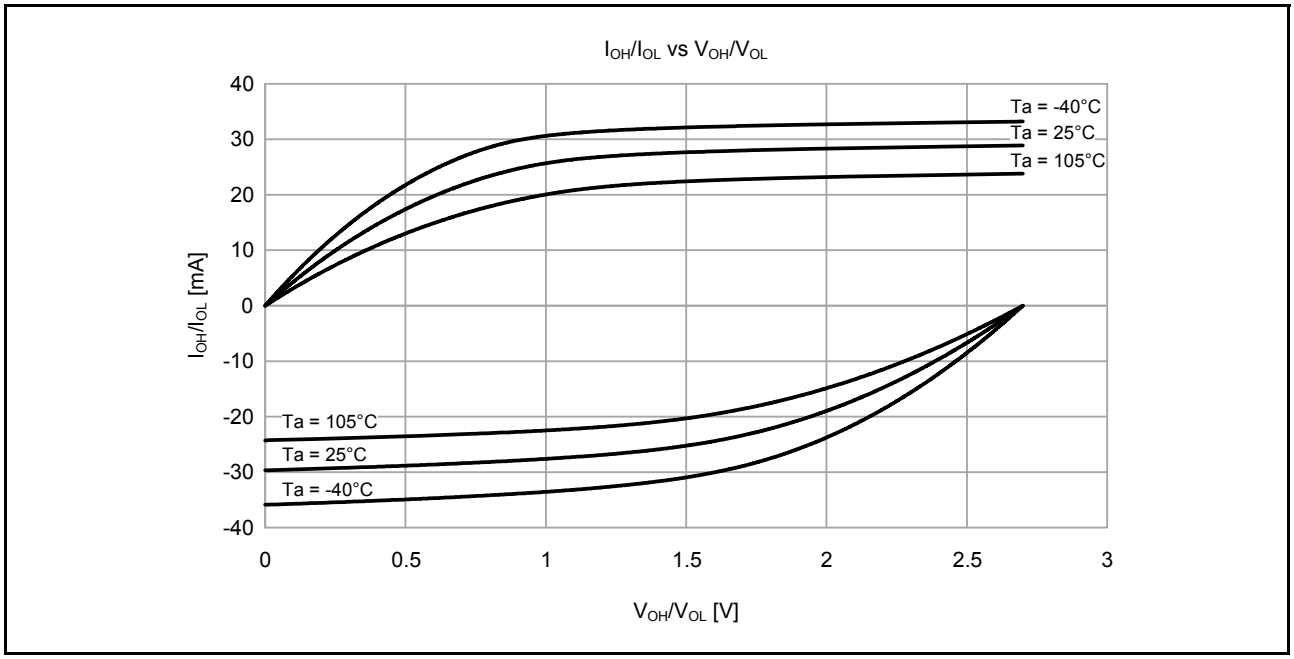
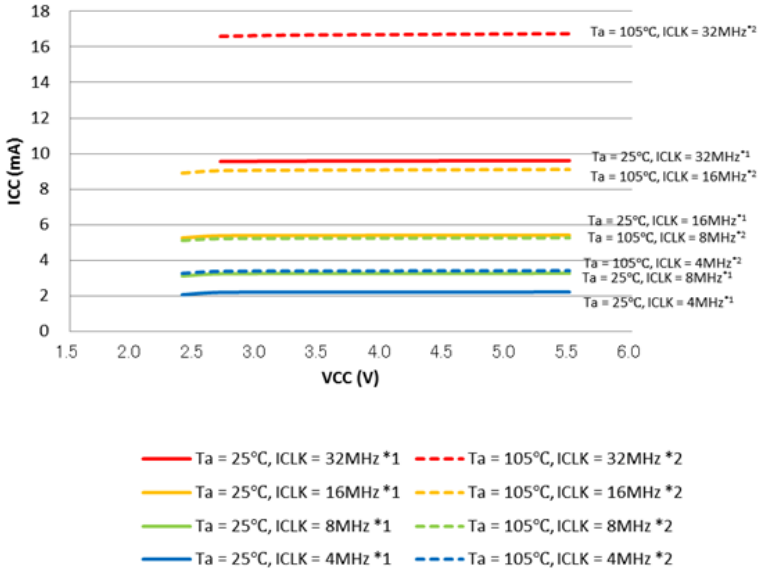


Figure 2.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

Table 2.11 Operating and standby current (1) (2 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions
Supply current*1	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.4	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		1.4	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		2.1	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		-	4.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		0.9	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		1.6	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	5.9	-	μA	*7
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		13.0	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		-	55.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		3.2	-		*7
			All peripheral clock enabled*5	ICLK = 32.768 kHz		10.0	-		*8

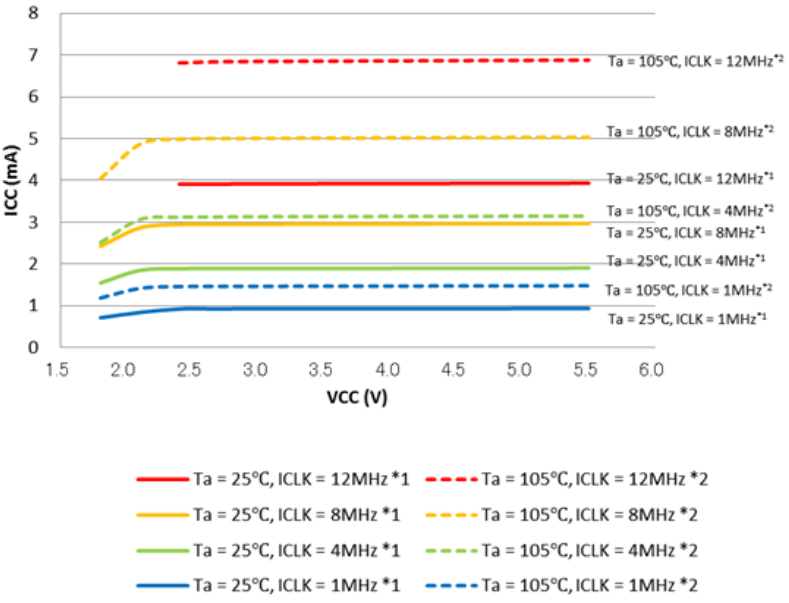
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. VCC = 3.3 V.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.17 Voltage dependency in high-speed operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.18 Voltage dependency in middle-speed operating mode (reference data)

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Peripheral module clock (PCLKB)*4	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3, *4	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.19 Operation frequency in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3, *4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see Table 2.21, Clock timing.

Table 2.20 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1, *3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2, *3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship between ICLK, PCLKB, and PCLKD frequencies.

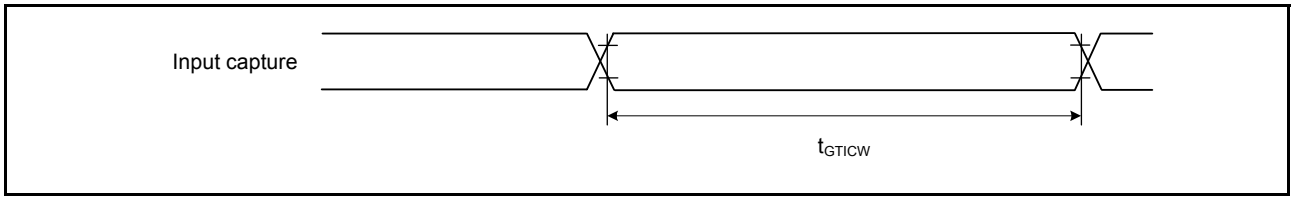


Figure 2.37 GPT input capture timing

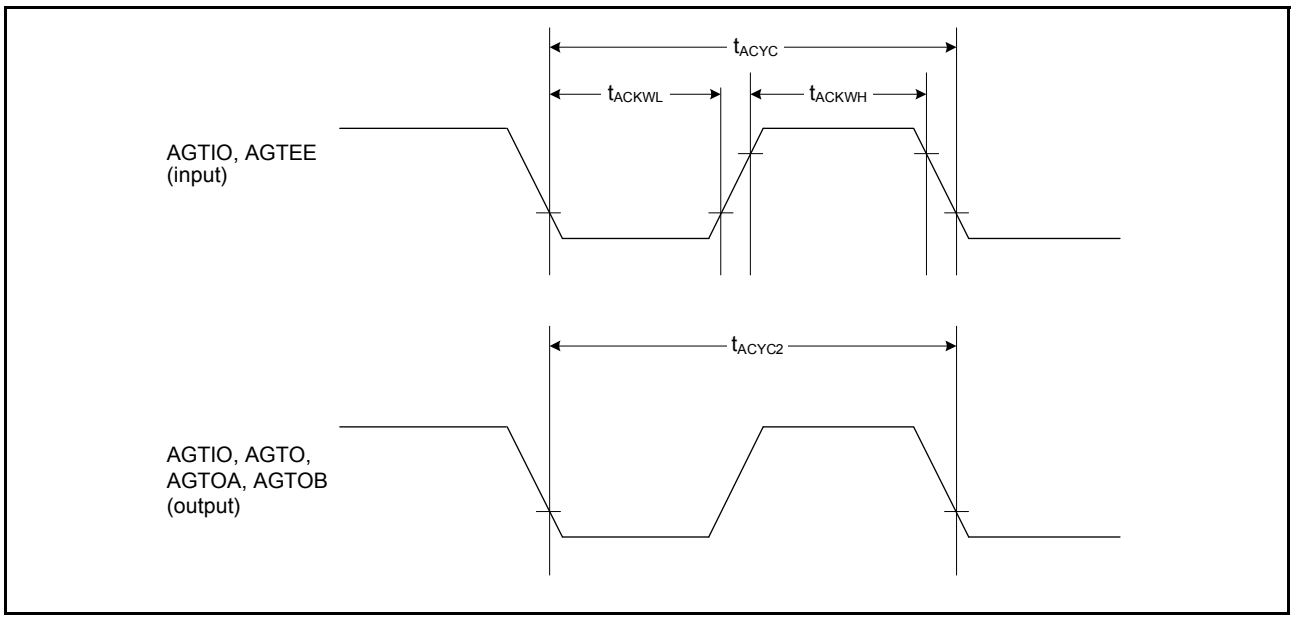


Figure 2.38 AGT I/O timing

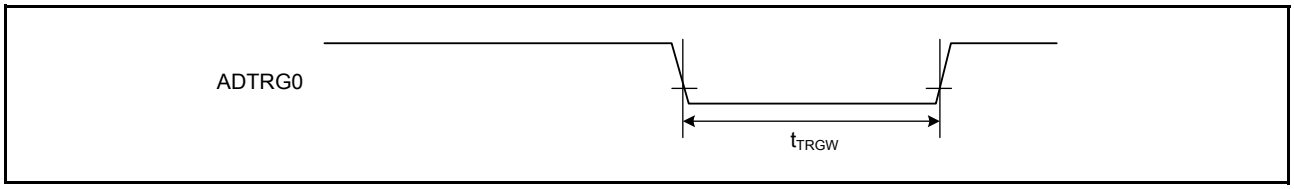


Figure 2.39 ADC14 trigger input timing

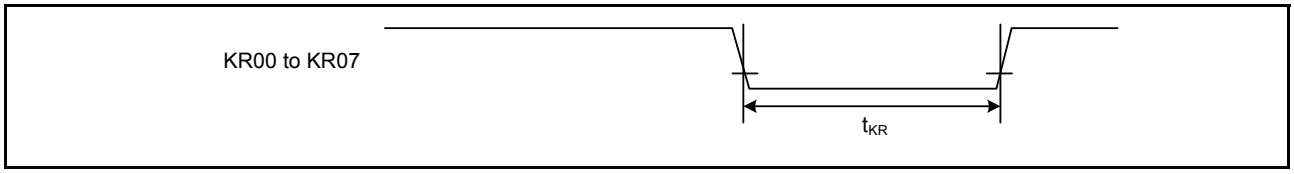


Figure 2.40 Key interrupt input timing

2.3.7 CAC Timing

Table 2.31 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

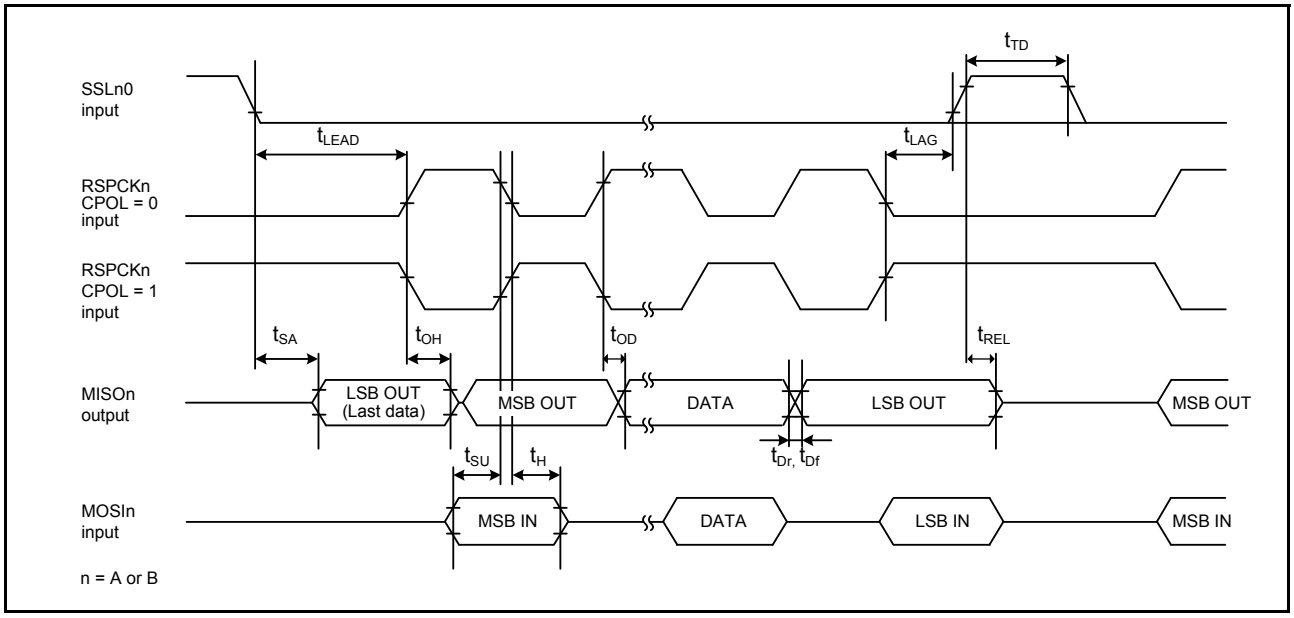


Figure 2.55 SPI timing (slave, CPHA = 1)

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.38 USB characteristics

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6V, Ta = –20 to +85°C

Parameter			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP – USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL}= 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 2.58, Figure 2.59, Figure 2.60
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery Charging Specification Ver 1.2	D + sink current		I_{DP_SINK}	25	175	µA	-
	D – sink current		I_{DM_SINK}	25	175	µA	-
	DCD source current		I_{DP_SRC}	7	13	µA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D + source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D – source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

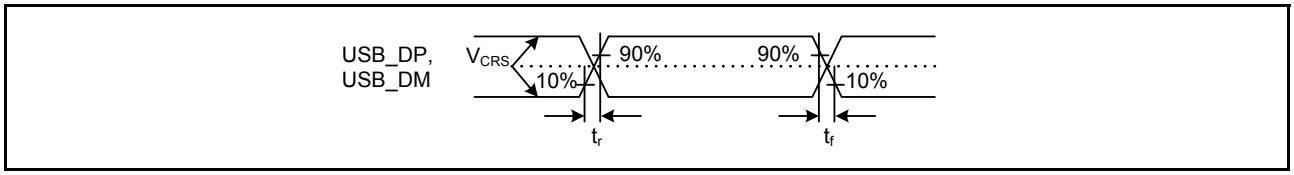


Figure 2.58 USB_DP and USB_DM output timing

Table 2.41 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.42 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	32	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above

Table 2.43 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.44 A/D conversion characteristics (5) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	16	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5*3	kΩ	High-precision channel
		-	-	6.7*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above

Table 2.45 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	7.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.88	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±12.0	±32.0	LSB	High-precision channel
				±48.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.

Table 2.46 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	4	MHz	-
Analog input capacitance*2	Cs	-	-	8*3	pF	High-precision channel
		-	-	9*3	pF	Normal-precision channel
Analog input resistance	Rs	-	-	13.1*3	kΩ	High-precision channel
		-	-	14.3*3	kΩ	Normal-precision channel

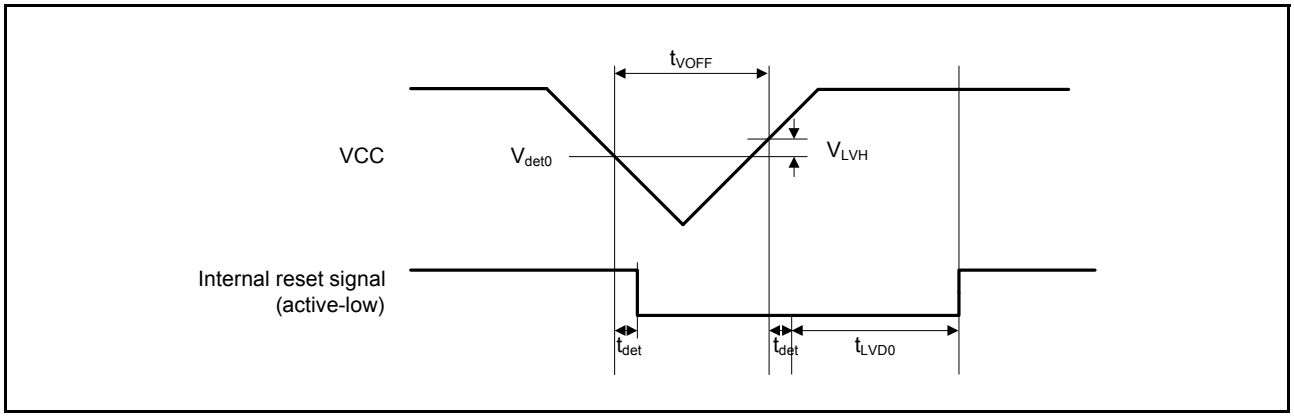


Figure 2.68 Voltage detection circuit timing (V_{det0})

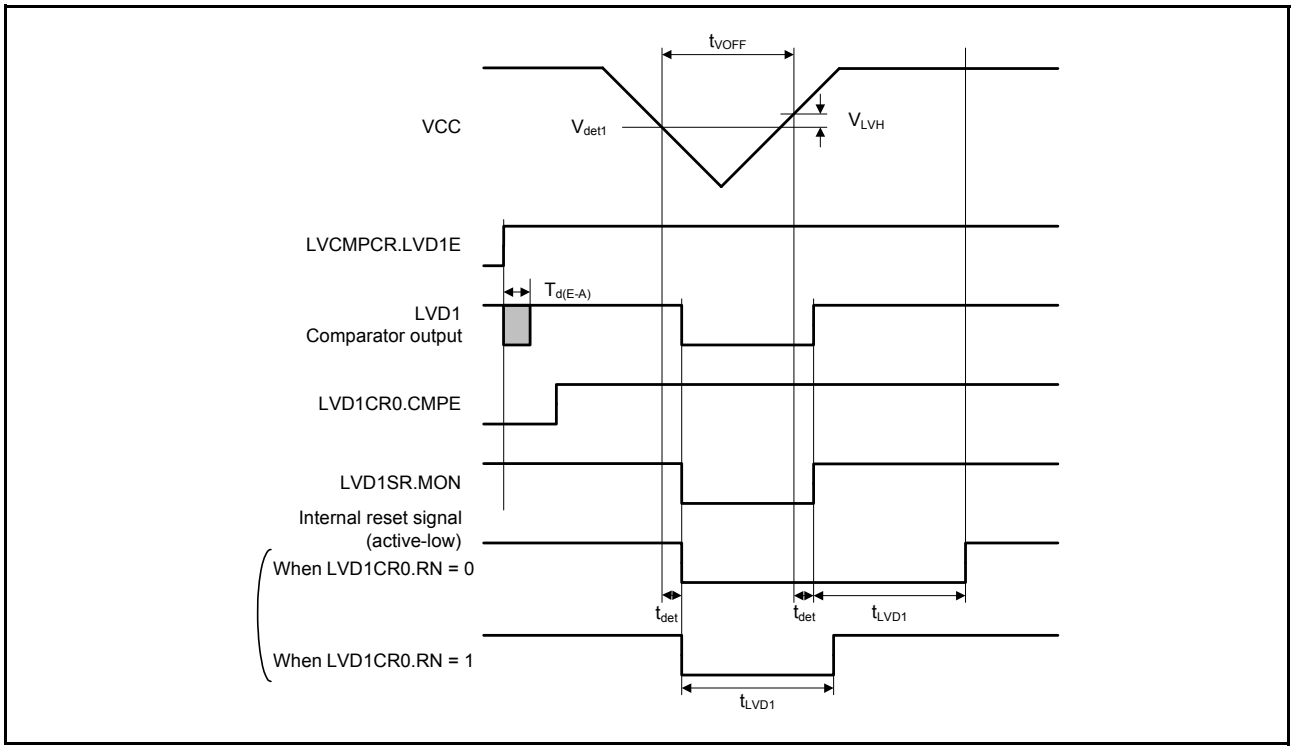


Figure 2.69 Voltage detection circuit timing (V_{det1})

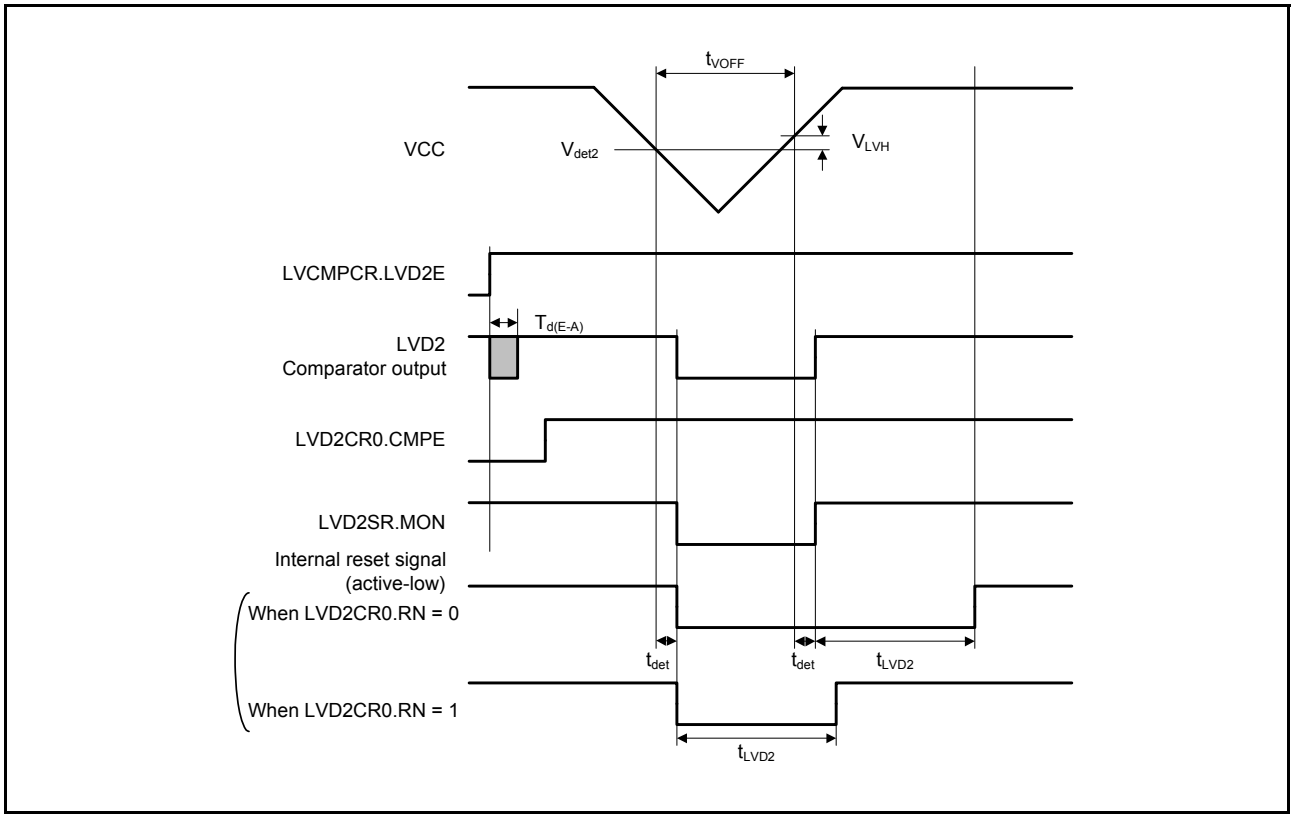


Figure 2.70 Voltage detection circuit timing (V_{det2})

2.10 CTSU Characteristics

Table 2.54 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

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R01DS0264EU0130