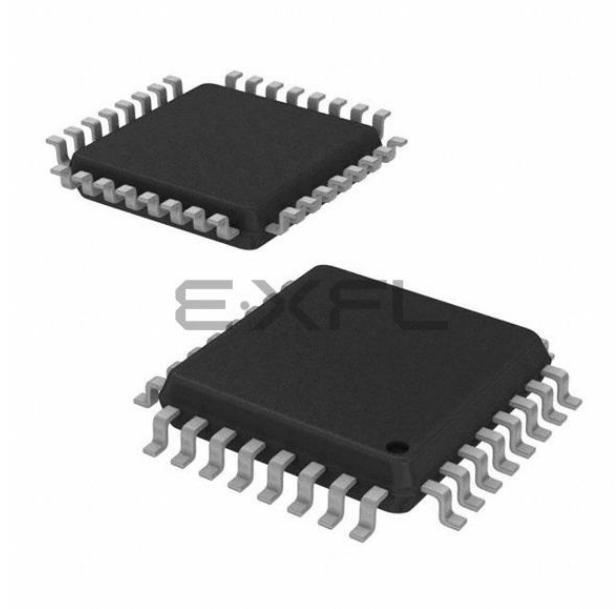

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c31b0agp20000

I2C Slave

- I2C Slave supports the slave function of I2C and wake-up function from Standby mode.

Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor that has already been constructed on the memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

A/D Converter (Max: 8 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 54 fast general-purpose I/O ports @64-pin package
- Certain ports are 5 V tolerant.
  See 4.List of Pin Functions and 5.I/O Circuit Typefor the corresponding pins.

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 12 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

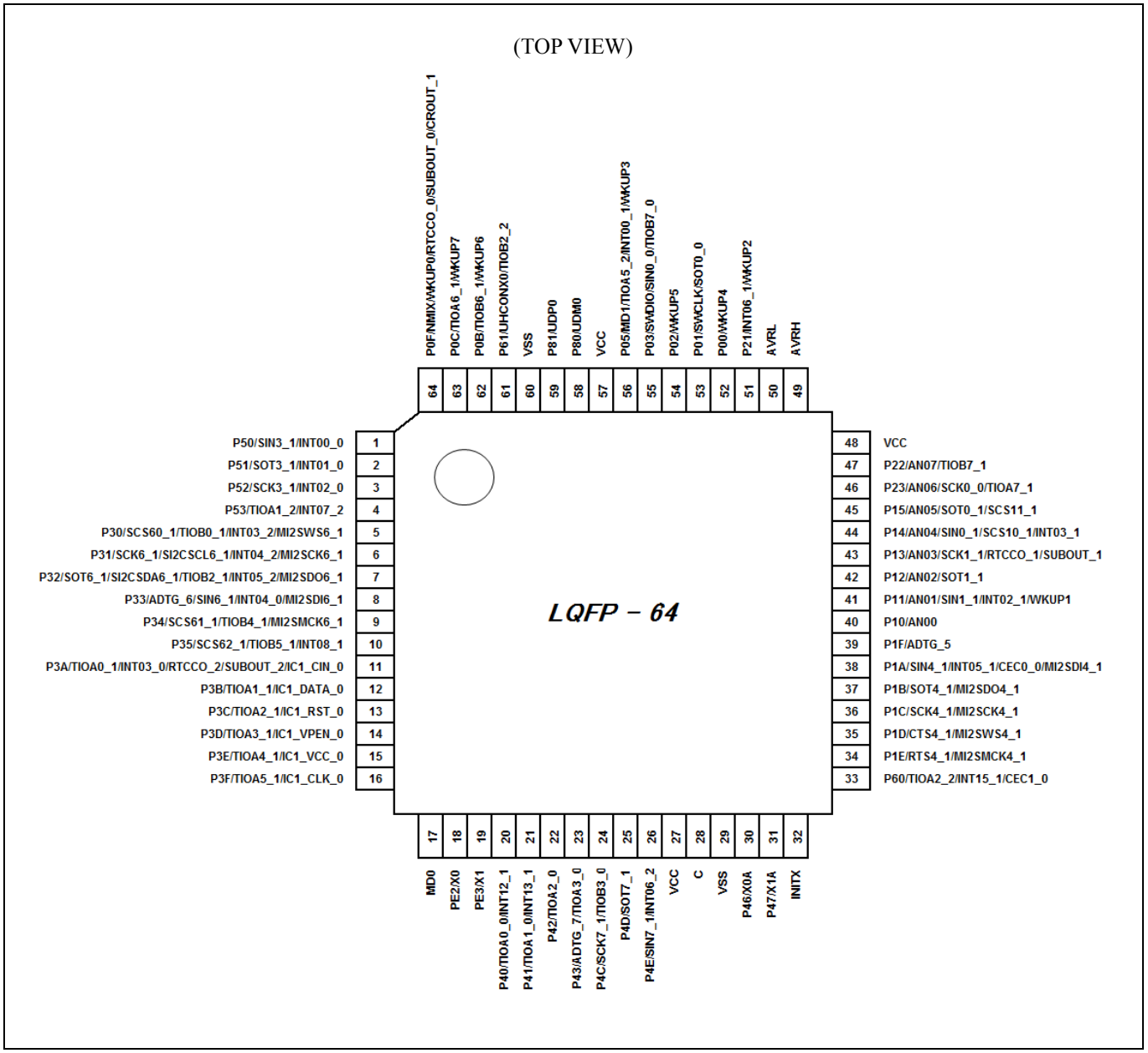
- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost

3. Pin Assignment

FPT-64P-M38



Note:

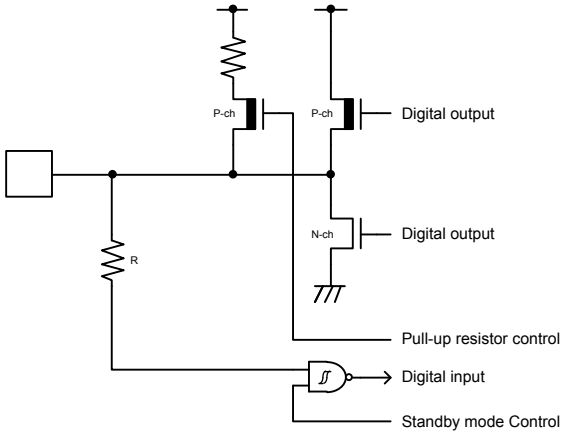
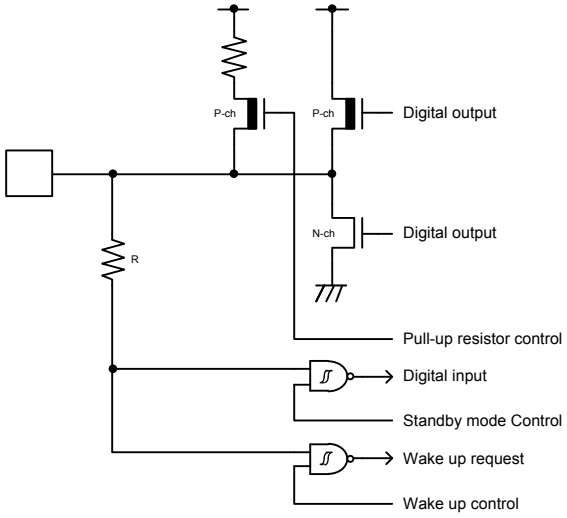
- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin no.				Pin Function	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)			
45	33	-	-	P15 AN05 SOT0_1 SCS11_1	F	J
46	34	22	-	P23 AN06 SCK0_0 TIOA7_1	F	J
47	35	23	-	P22 AN07 TIOB7_1	F	J
48	36	24	-	VCC	-	-
49	37	-	-	AVRH *	-	-
50	38	25	-	AVRL	-	-
51	39	26	-	P21 INT06_1 WKUP2	E	K
52	-	-	-	P00 WKUP4	E	K
53	40	27	-	P01 SWCLK SOT0_0	D	K
54	-	-	-	P02 WKUP5	E	K
55	41	28	-	P03 SWDIO SIN0_0 TIOB7_0	D	K
56	42	29	-	P05 MD1 TIOA5_2 INT00_1 WKUP3	E	K
57	43	-	-	VCC	-	-
58	44	30	-	P80 UDM0	J	G
59	45	31	-	P81 UDP0	J	G
60	46	32	-	VSS	-	-
61	47	-	-	P61 UHCONX0 TIOB2_2	H	K
62	-	-	-	P0B TIOB6_1 WKUP6	E	K

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
ADC	ADTG_5	A/D converter external trigger input pin	39	-	-	-
	ADTG_6		8	8	7	-
	ADTG_7		23	-	-	-
ADC	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	40	28	18	-
	AN01		41	29	19	-
	AN02		42	30	20	-
	AN03		43	31	21	-
	AN04		44	32	-	-
	AN05		45	33	-	-
	AN06		46	34	22	-
	AN07		47	35	23	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	20	-	-	-
	TIOA0_1		11	10	-	-
	TIOB0_1	Base timer ch.0 TIOB pin	5	5	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	21	-	-	-
	TIOA1_1		12	11	-	-
	TIOA1_2		4	4	-	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	22	-	-	-
	TIOA2_1		13	12	-	-
	TIOA2_2		33	25	17	-
	TIOB2_1	Base timer ch.2 TIOB pin	7	7	6	-
	TIOB2_2		61	47	-	-
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	23	-	-	-
	TIOA3_1		14	-	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	24	-	-	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	15	-	-	-
	TIOB4_1	Base timer ch.4 TIOB pin	9	-	-	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	16	-	-	-
	TIOA5_2		56	42	29	-
	TIOB5_1	Base timer ch.5 TIOB pin	10	-	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	63	-	-	-
	TIOB6_1	Base timer ch.6 TIOB pin	62	-	-	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	34	22	-
	TIOB7_0	Base timer ch.7 TIOB pin	55	41	28	-
	TIOB7_1		47	35	23	-
Debugger	SWCLK	Serial wire debug interface clock input pin	53	40	27	-
	SWDIO	Serial wire debug interface data input / output pin	55	41	28	-

Type	Circuit	Remarks
D		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off

Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Reserved
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		Reserved
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote Control Receiver
0x4003_5000	0x4003_5FFF		Low-Voltage Detection / DS mode / Vref Calibration
0x4003_6000	0x4003_6FFF		USB Clock Generator
0x4003_7000	0x4003_77FF		Reserved
0x4003_7800	0x4003_79FF		I2C Slave
0x4003_7A00	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_C8FF		Reserved
0x4003_C900	0x4003_C9FF		Smart Card Interface
0x4003_CA00	0x4003_CAFF		MFS-I2S Clock Generator
0x4003_CB00	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		DSTC
0x4006_2000	0x41FF_FFFF		Reserved

Each term in above table have the following meanings.

Type
This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1) Reset state. CPU is initialized by Power-on reset or a reset due to low Power voltage supply.

(2) Reset state. CPU is initialized by INITX input signal or system initialization after power on reset.

(3) Run mode or SLEEP mode state.

(4) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

(5) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

(6) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"

(7) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"

(8) Run mode state after returning from Deep Standby mode.
(I/O state hold function(CONTX) is fixed at 1)

Each pin status

The meaning of the symbols in the pin status table is as follows.

IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
IE	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
IP	Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
IE/IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
OE	The OSC is in operation state. However, it may be stopped in some operation mode of the CPU. For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
OS	The OSC is in stop state. (Hi-Z)
UE	USB I/O function is controlled by USB controller.
US	USB I/O function is disabled(Hi-Z)
PC	Digital output and pull up register is controlled by the register in the GPIO or peripheral function. Digital input is not shut off
CP	Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off. Digital input is not shut off.
HC	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
HS	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
GS	Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

Additional note

Additional note is described below.

*1	In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.
*2	In this type, when Digital I/O function is selected, internal oscillation function is disabled.
*3	In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.
*4	In this type, when Digital I/O function is selected, analog input function is not available.
*5	In this case, PCR register is initialized to “1”. Pull up register is on.
*6	In this type, when Digital I/O function is selected, USB I/O function is disabled. This pin does not have pull up register.
*7	In this type, when USB I/O function is selected, digital output is disabled. (Hi-Z), digital input is shut off by fixed 0.

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	Ta=25°C Vcc=3.3 V	0.58	1.85	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.56	1.83	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	0.78	6.6	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.76	6.6	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	Ta=25°C Vcc=3.3 V	1.16	2.4	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.15	2.4	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	1.37	7.2	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.35	7.2	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2

*1: All ports are fixed. LVD off.

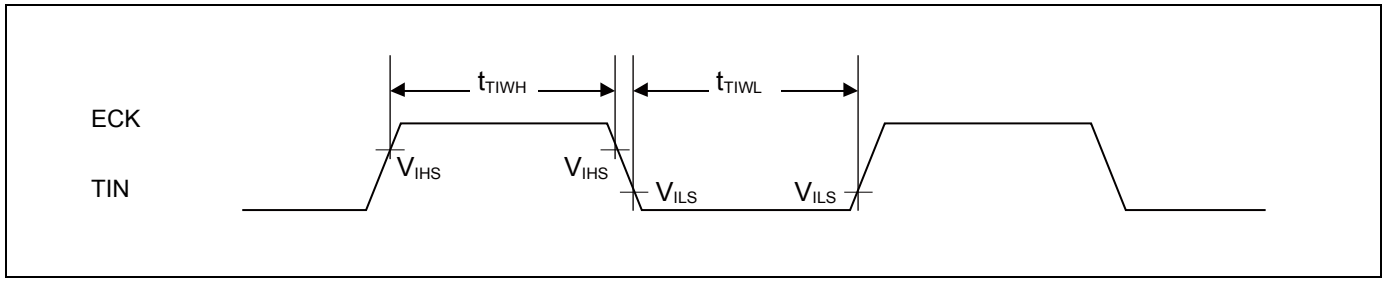
*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

11.4.8 Base Timer Input Timing

Timer Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

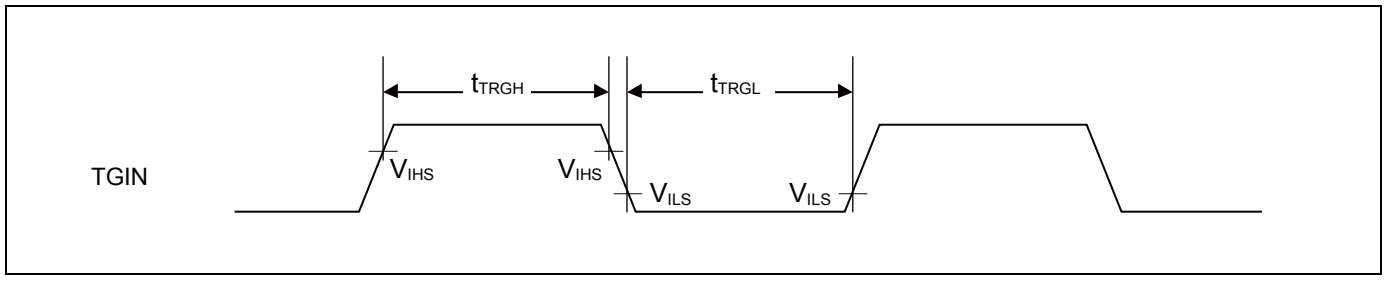
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

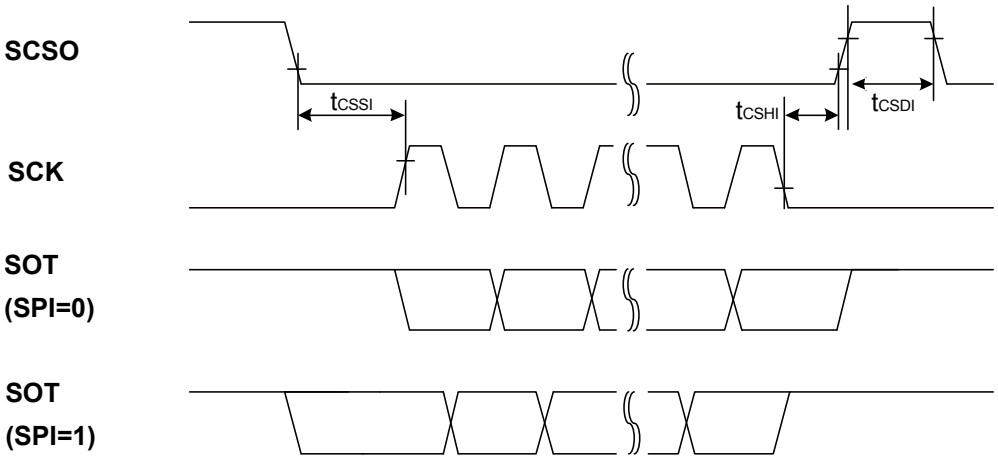
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

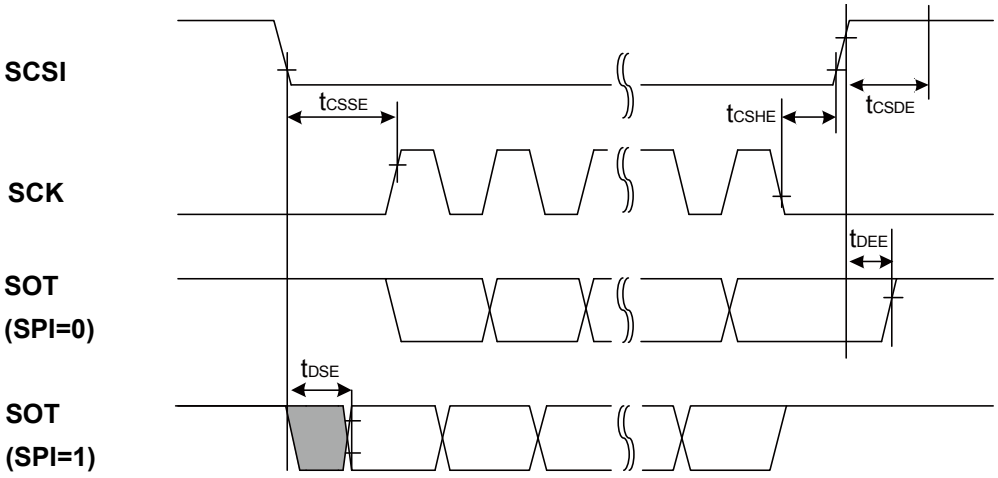
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↓ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

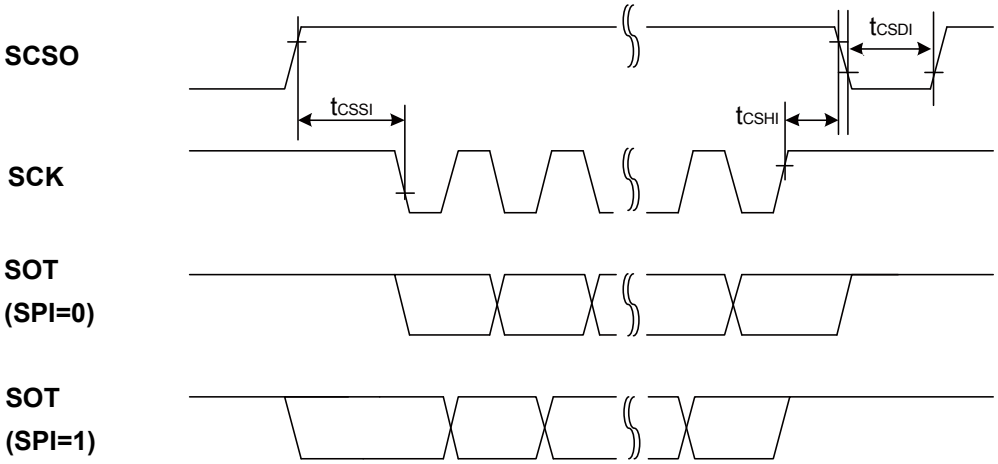
*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

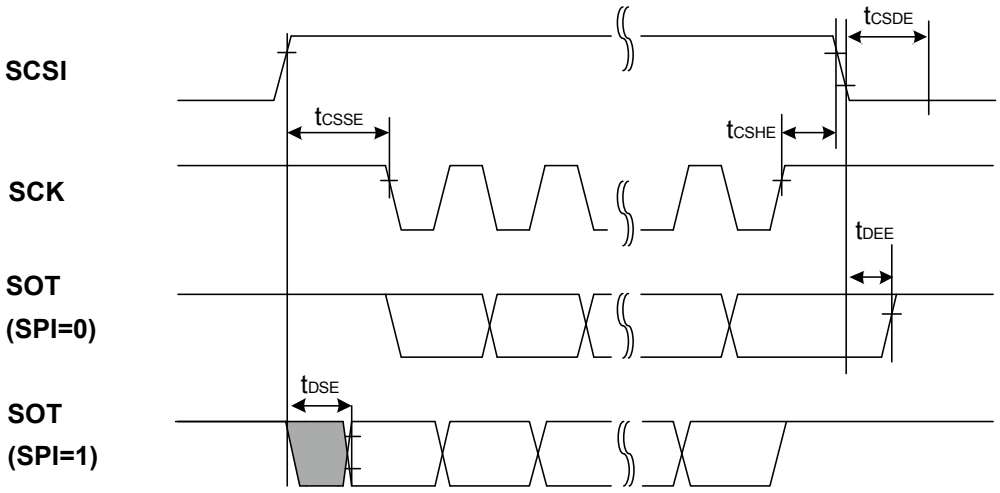
*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*



Master mode



Slave mode

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↑→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

11.4.10 External Input Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

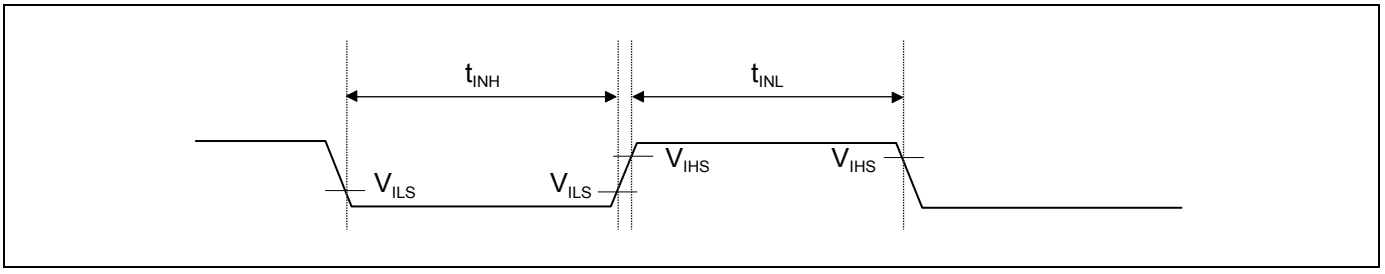
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*1	-	ns	A/D converter trigger input
		INT00 to INT08, INT12, INT13, INT15, NMIX	*2	2 t_{CYCP} +100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
		WKUPx	*4	500	-	ns	Deep standby wake up

*1: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

*2: In Run mode and Sleep mode

*3: In Timer mode, RTC mode and Stop mode

*4: In Deep Standby RTC mode and Deep Standby Stop mode



11.4.13 Smart Card Interface Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t_R	ICx_VCC, ICx_RST, ICx_CLK, ICx_DATA	C_L=30 pF	4	20	ns	
Output falling time	t_F			4	20	ns	
Output clock frequency	f_{CLK}	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

■External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx_CIN pin when it's used as smart card reader function.

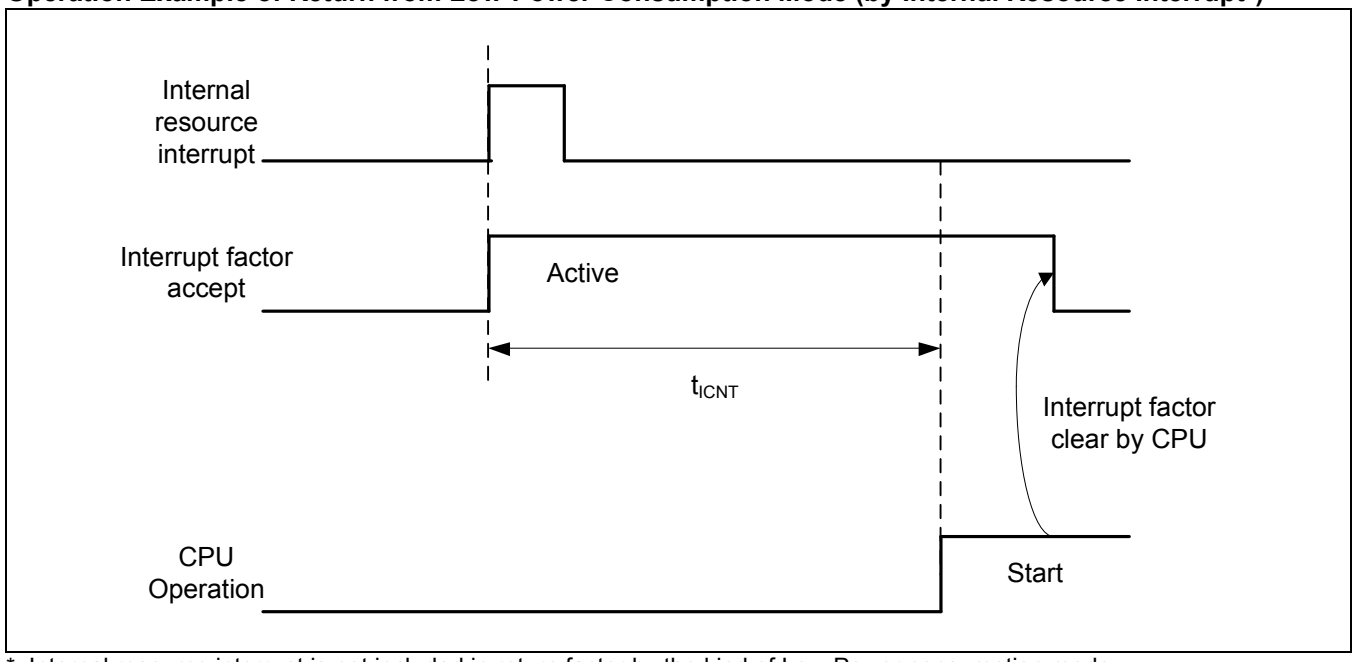
11.7.2 Low-Voltage Detection Interrupt

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} represents the APB1 bus clock cycle time.

Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*

12. Ordering Information

Part number	On-chip Flash memory [Kbyte]	On-Chip SRAM [Kbyte]	Package	Packing
S6E1C32D0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 64 pins (FPT-64P-M38)	Tray
S6E1C31D0AGV20000	64	12		
S6E1C32C0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 48 pins (FPT-48P-M49)	Tray
S6E1C31C0AGV20000	64	12		
S6E1C32B0AGP20000	128	16	Plastic • LQFP (0.80 mm pitch), 32 pins (FPT-32P-M30)	Tray
S6E1C31B0AGP20000	64	12		
S6E1C32D0AGN20000	128	16	Plastic • QFN64 (0.50 mm pitch), 64 pins (LCC-64P-M25)	Tray
S6E1C31D0AGN20000	64	12		
S6E1C32C0AGN20000	128	16	Plastic • QFN48 (0.50 mm pitch), 48 pins (LCC-48P-M74)	Tray
S6E1C31C0AGN20000	64	12		
S6E1C32B0AGN20000	128	16	Plastic • QFN32 (0.50 mm pitch), 32 pins (LCC-32P-M73)	Tray
S6E1C31B0AGN20000	64	12		
(TBD)	128	16	WLCSP (TBD)	(TBD)