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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c31c0agv20000

- Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
- Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

■ HDMI-CEC receiver
- Automatic ACK reply function available
- Line error detection function available

■ Remote control receiver
- 4 bytes reception buffer
- Repeat code detection function available

Smart Card Interface (Max 1 Channel)

■ Compliant with ISO7816-3 specification

■ Card Reader only/B class card only

■ Available protocols
- Transmitter: 8E2, 8O2, 8N2
- Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
- Inverse mode

■ TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

Clock and Reset

■ Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

Main clock:	8 MHz to 48 MHz
Sub clock:	32.768 kHz
Built-in high-speed CR clock:	8 MHz
Built-in low-speed CR clock:	100 kHz
Main PLL clock	8MHz to 16MHz (Input), 75MHz to 150MHz (Output)

■ Resets
- Reset request from the INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detection reset
- Clock supervisor reset

Clock Supervisor (CSV)

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

■ If an external clock failure (clock stop) is detected, a reset is asserted.

■ If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-Voltage Detector (LVD)

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

■ LVD1: monitor V_{CC} and error reporting via an interrupt

■ LVD2: auto-reset operation

Low Power Consumption Mode

This series has six low power consumption modes.

■ Sleep

■ Timer

■ RTC

■ Stop

■ Deep standby RTC (selectable between keeping the value of RAM and not)

■ Deep standby Stop (selectable between keeping the value of RAM and not)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

■ Serial Wire Debug Port (SW-DP)

■ Micro Trace Buffer (MTB)

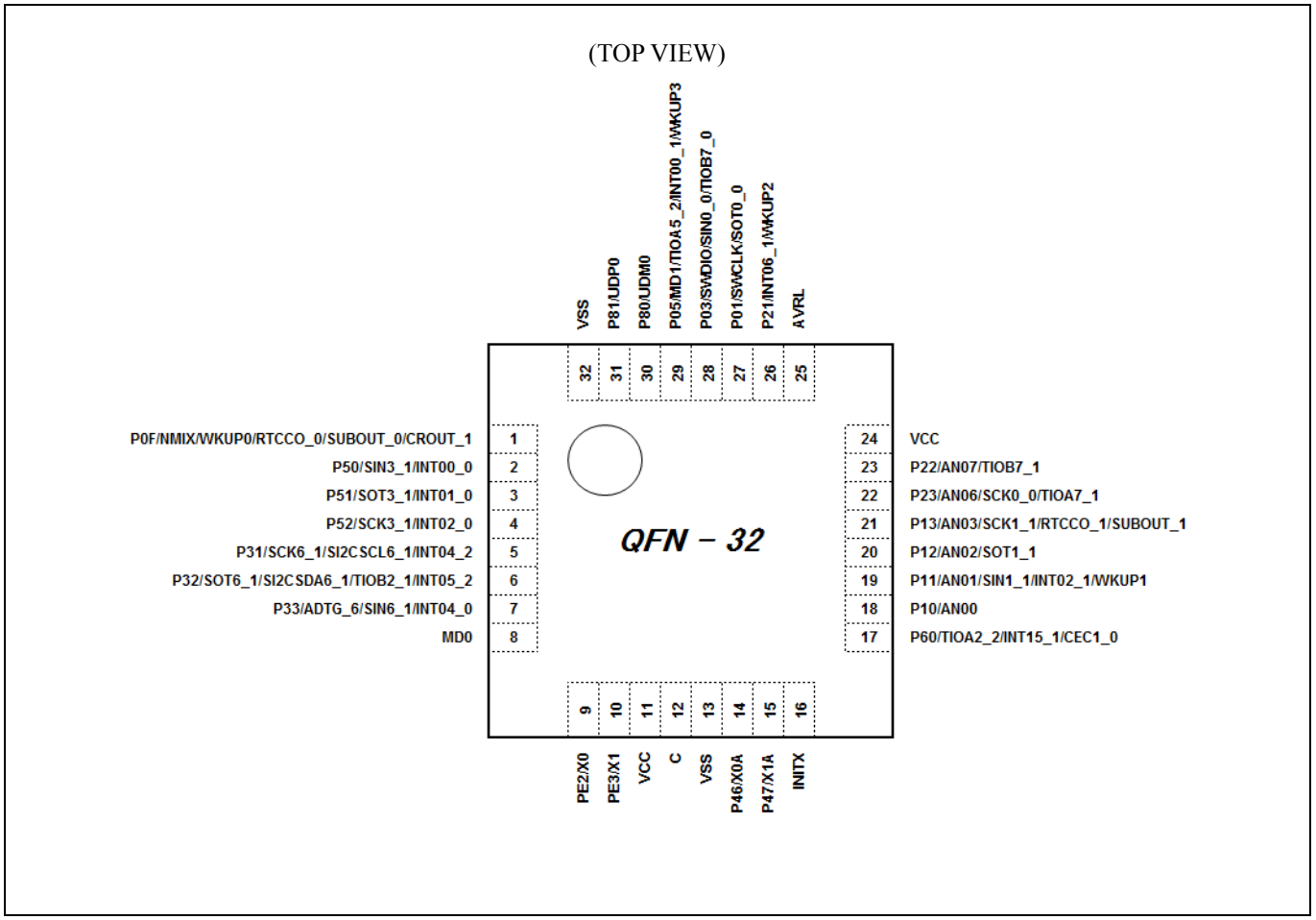
Unique ID

A 41-bit unique value of the device has been set.

Power Supply

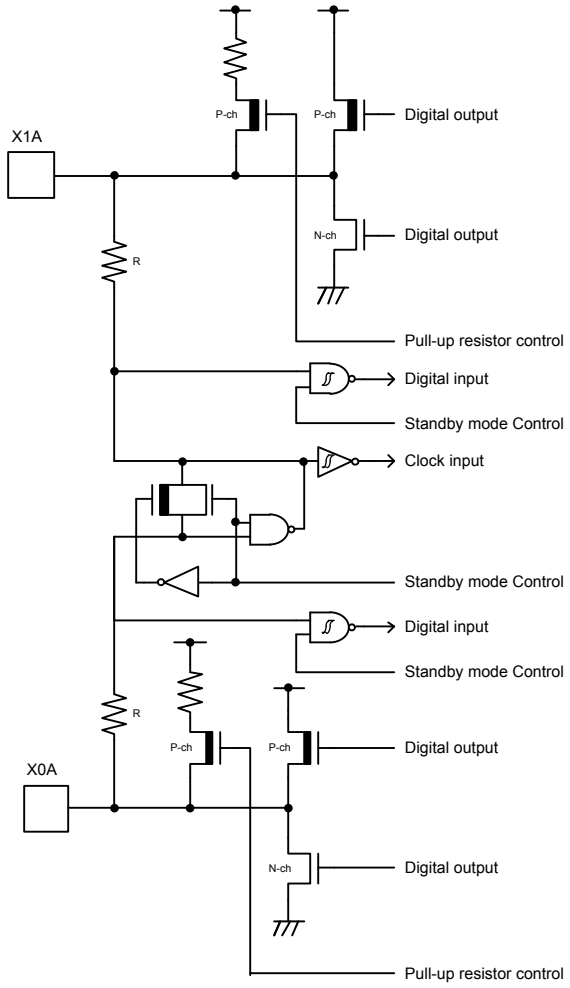
■ Wide voltage range:
VCC = 1.65V to 3.6 V
VCC = 3.0V to 3.6V (when USB is used)

LCC-32P-M73



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

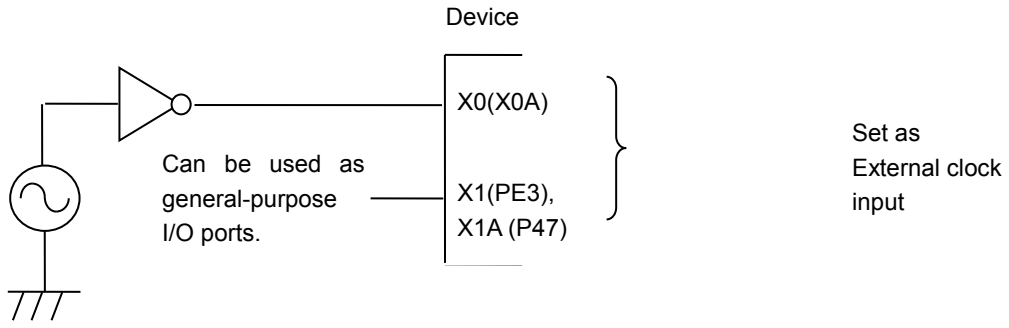
Type	Circuit	Remarks
C		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 33kΩ I_{OH}= -4mA, I_{OL}= 4mA

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

However in the Deep Standby mode, an external clock as an input of the sub clock cannot be used.

Example of Using an External Clock



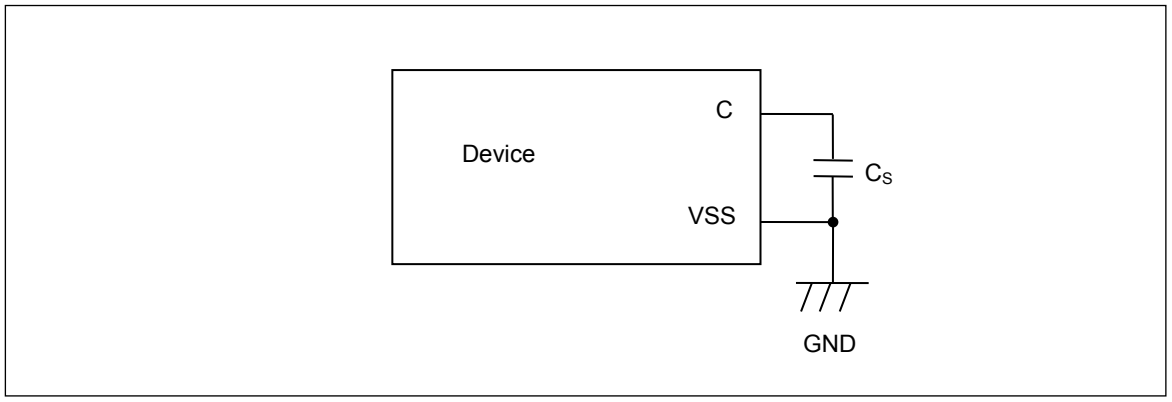
Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.

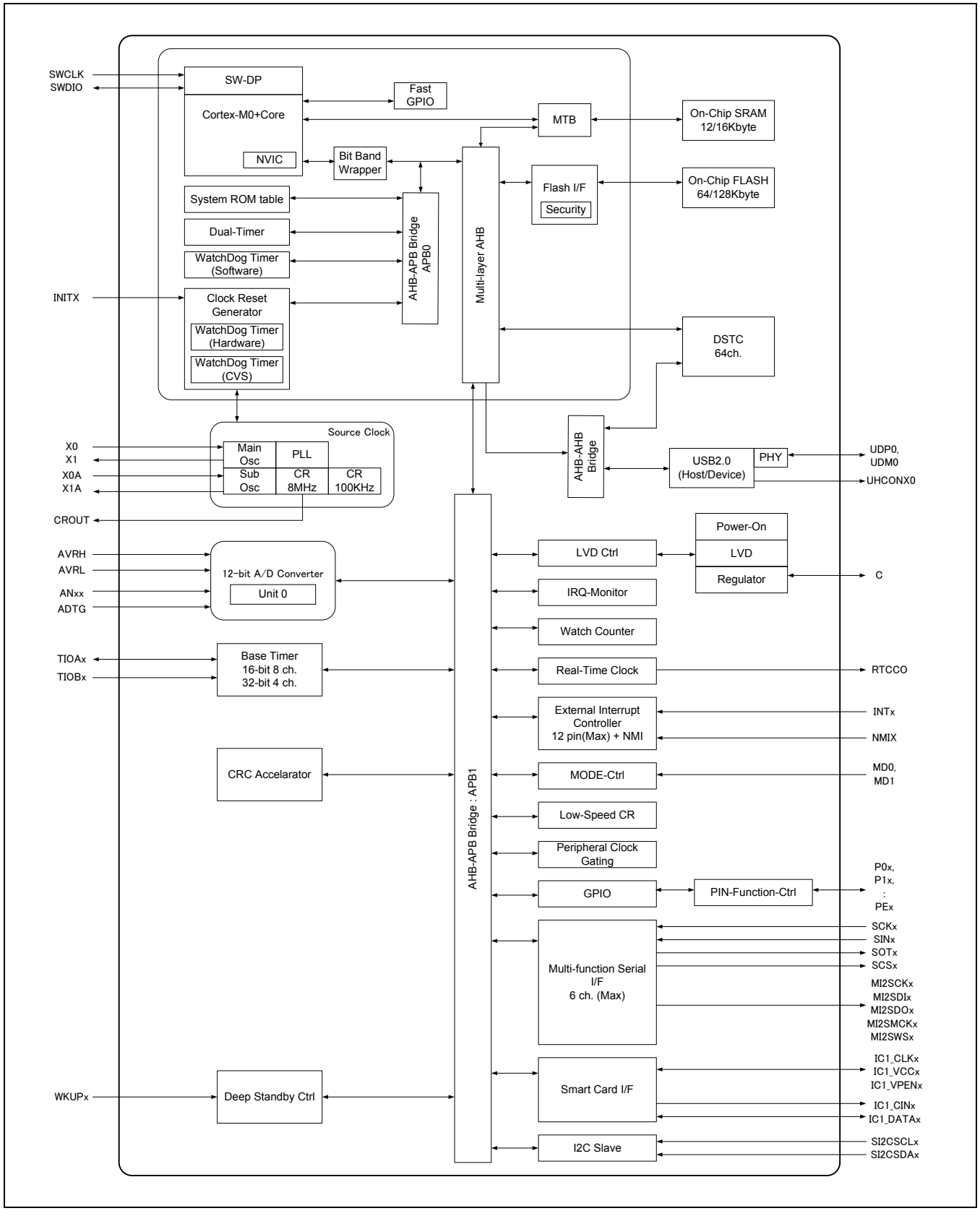
Incidentally, the C pin becomes floating in Deep standby mode.



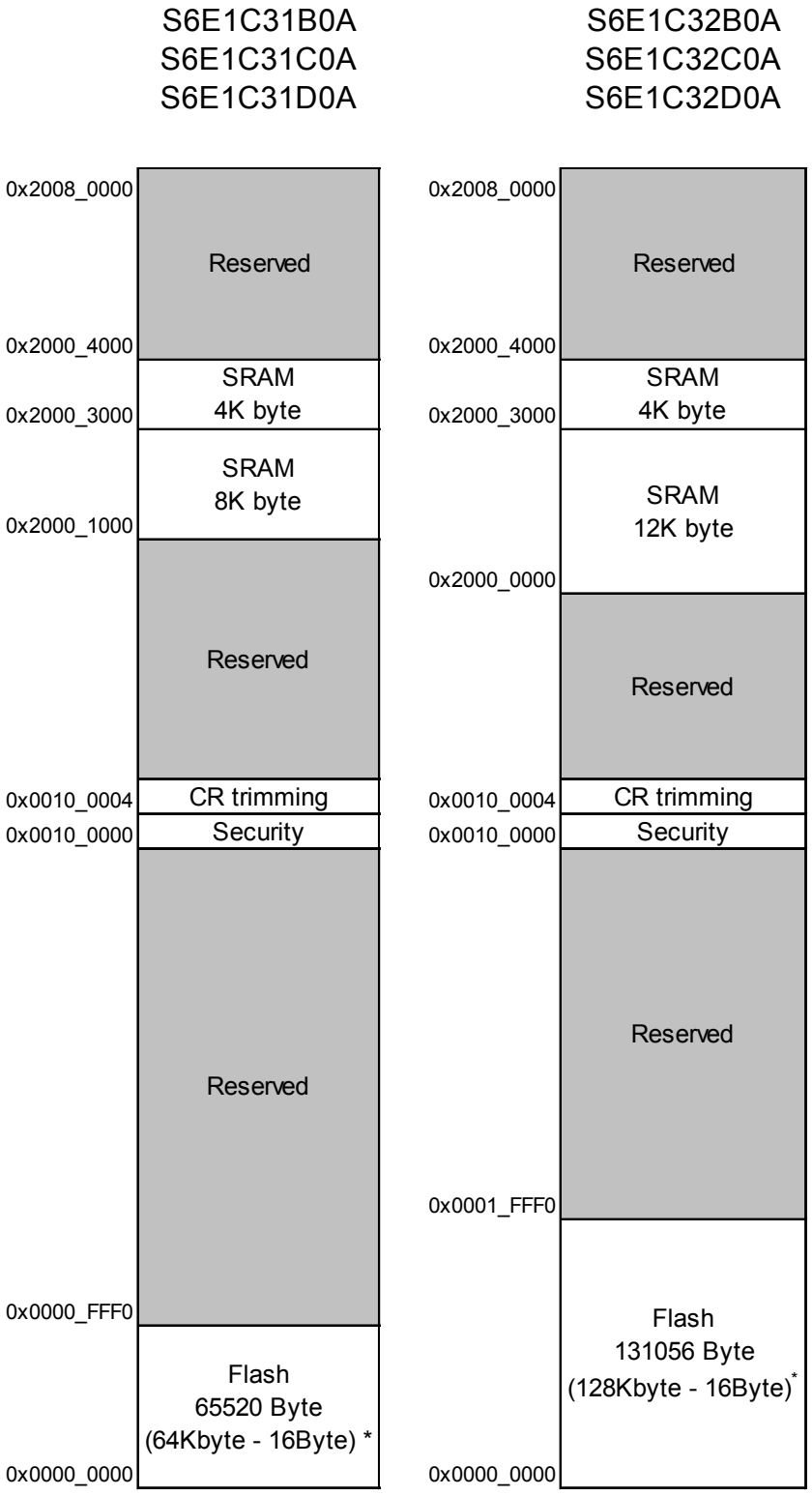
Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

8. Block Diagram



Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	Ta=25°C Vcc=3.3 V	12.4	52.4	µA	*1, *2
			Ta=25°C Vcc=1.65 V	12.0	52.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V	-	597	µA	*1, *2
	I_{CCT} (VCC)	Sub timer mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	15.6	55.6	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	15.0	55.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	601	µA	*1, *2
	I_{CCR} (VCC)	RTC mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	13.2	53.2	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	12.7	52.7	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	598	µA	*1, *2

*1: All ports are fixed. LVD off. Flash off.

*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I_{CCHD} (VCC)	Deep standby Stop mode	RAM off	Ta=25°C Vcc=3.3 V	0.58	1.85	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.56	1.83	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	0.78	6.6	µA	*1, *2
				Ta=25°C Vcc=1.65 V	0.76	6.6	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2
	I_{CCRD} (VCC)	Deep standby RTC mode	RAM off	Ta=25°C Vcc=3.3 V	1.16	2.4	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.15	2.4	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	46	µA	*1, *2
			RAM on	Ta=25°C Vcc=3.3 V	1.37	7.2	µA	*1, *2
				Ta=25°C Vcc=1.65 V	1.35	7.2	µA	*1, *2
				Ta=105°C Vcc=3.6 V	-	88	µA	*1, *2

*1: All ports are fixed. LVD off.

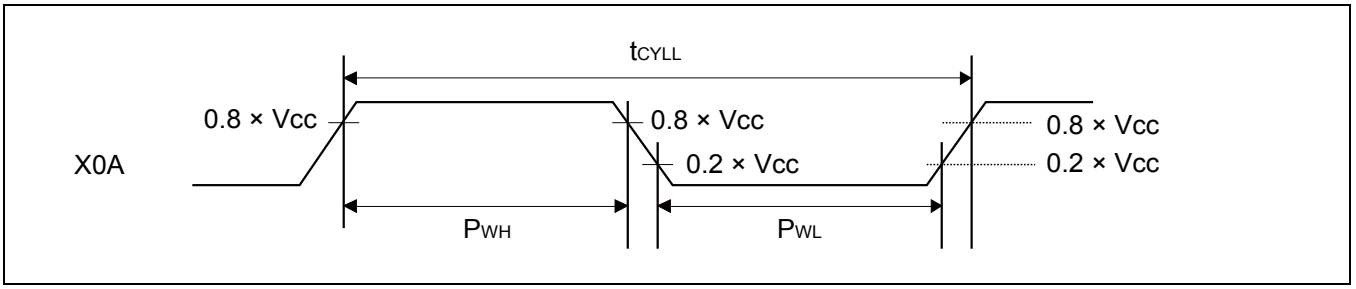
*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

11.4.2 Sub Clock Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



11.4.9 CSIO/SPI/UART Timing

CSIO (SPI=0, SCINV=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

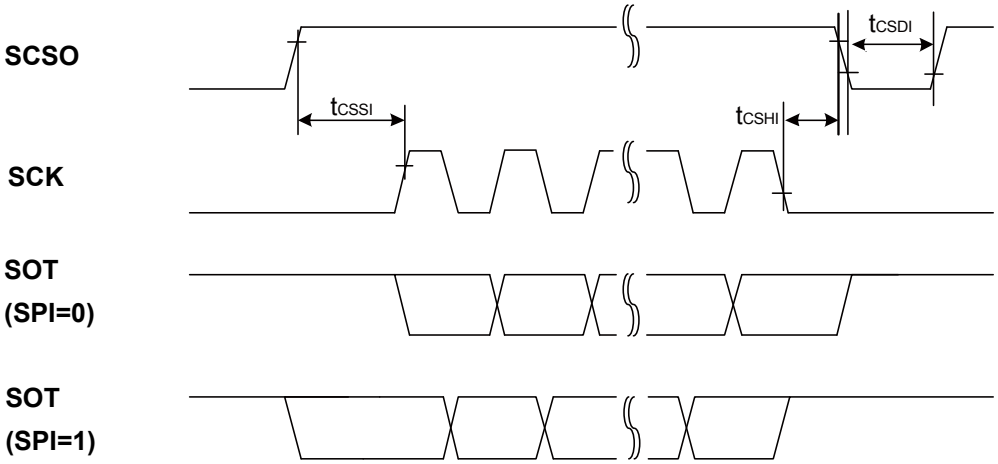
SPI (SPI=1, SCINV=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

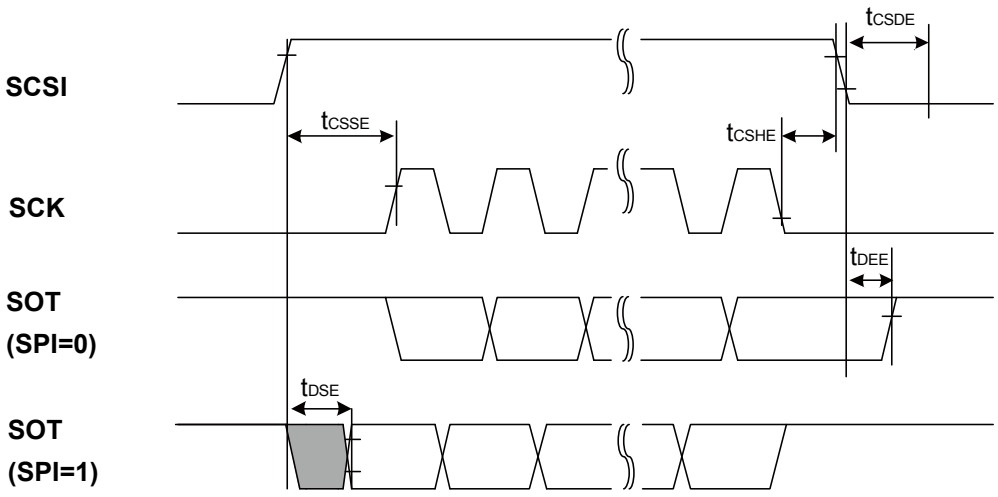
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*



Master mode



Slave mode

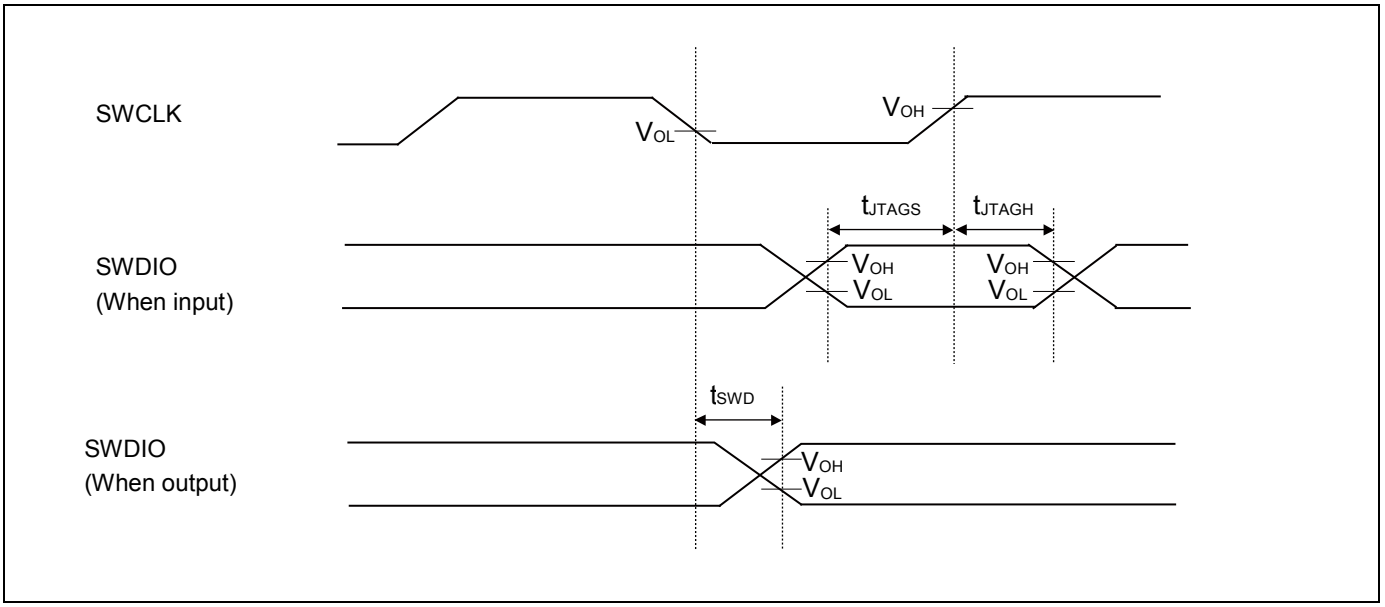
11.4.14 SW-DP Timing

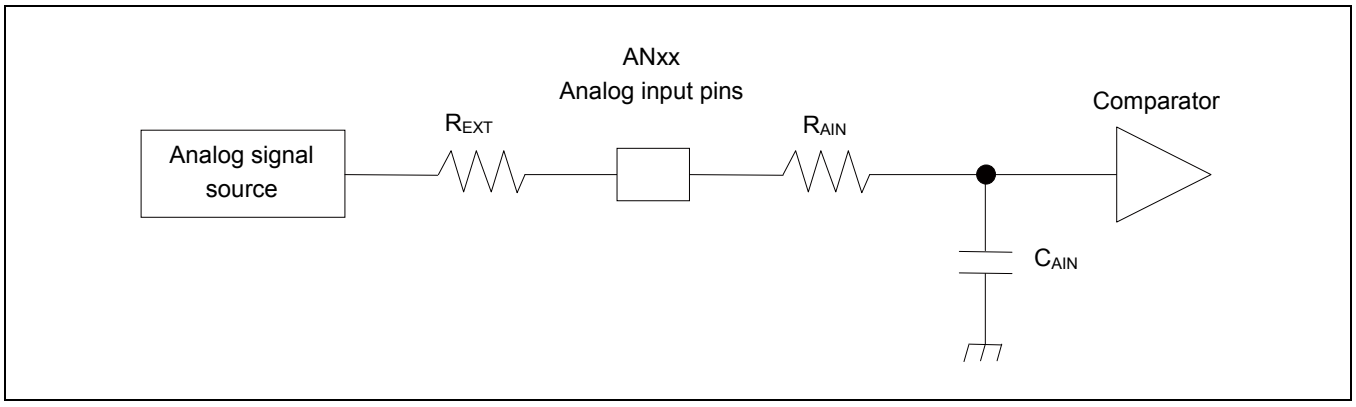
(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- *External load capacitance C_L=30 pF*





(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D Converter = 2.2 kΩ with 2.7 ≤ VCC ≤ 3.6
Input resistance of A/D Converter = 5.5 kΩ with 1.8 ≤ VCC ≤ 2.7
Input resistance of A/D Converter = 10.5 kΩ with 1.65 ≤ VCC ≤ 1.8

C_{AIN}: Input capacitance of A/D Converter = 7.5 pF with 1.65 ≤ VCC ≤ 3.6

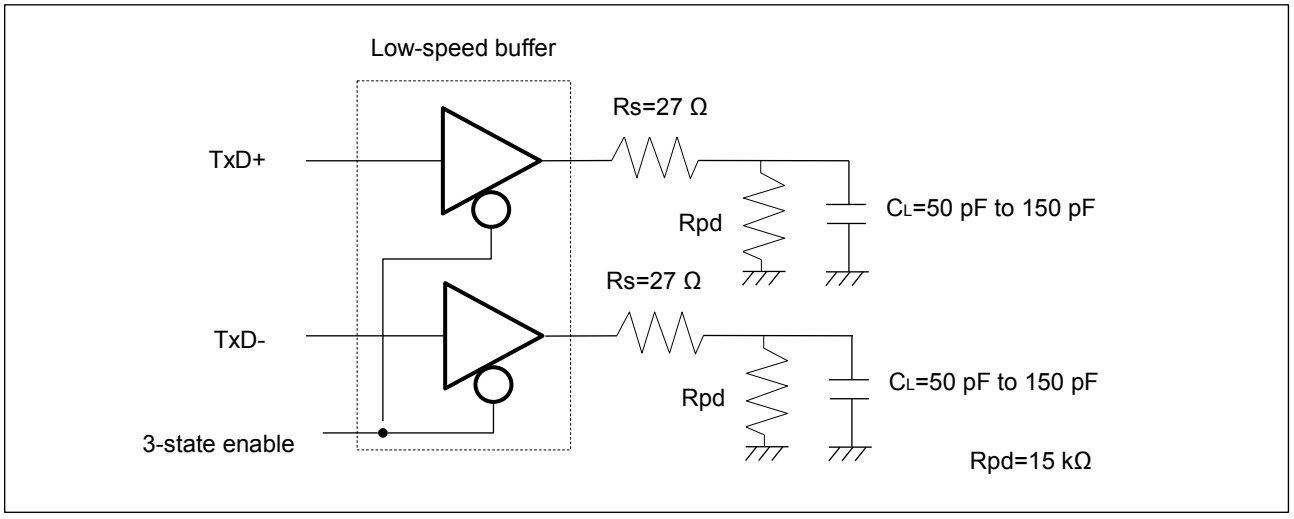
R_{EXT}: Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

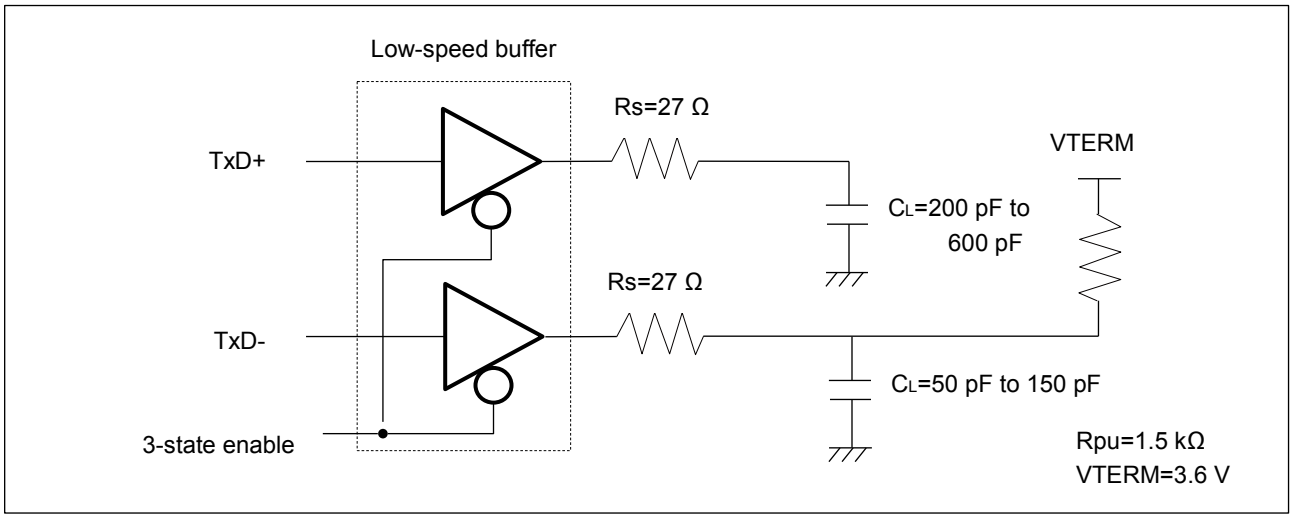
t_C: Compare time

t_{CCK} : Compare clock cycle

- Low-Speed Load (Upstream Port Load) – Reference 1



- Low-Speed Load (Downstream Port Load) – Reference 2



11.7.2 Low-Voltage Detection Interrupt

(T_A=-40°C to +105°C)

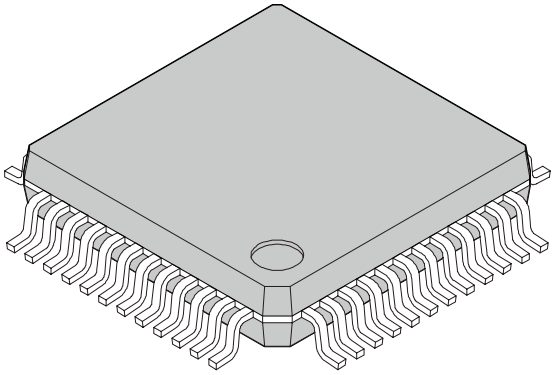
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} represents the APB1 bus clock cycle time.

12. Ordering Information

Part number	On-chip Flash memory [Kbyte]	On-Chip SRAM [Kbyte]	Package	Packing
S6E1C32D0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 64 pins (FPT-64P-M38)	Tray
S6E1C31D0AGV20000	64	12		
S6E1C32C0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 48 pins (FPT-48P-M49)	Tray
S6E1C31C0AGV20000	64	12		
S6E1C32B0AGP20000	128	16	Plastic • LQFP (0.80 mm pitch), 32 pins (FPT-32P-M30)	Tray
S6E1C31B0AGP20000	64	12		
S6E1C32D0AGN20000	128	16	Plastic • QFN64 (0.50 mm pitch), 64 pins (LCC-64P-M25)	Tray
S6E1C31D0AGN20000	64	12		
S6E1C32C0AGN20000	128	16	Plastic • QFN48 (0.50 mm pitch), 48 pins (LCC-48P-M74)	Tray
S6E1C31C0AGN20000	64	12		
S6E1C32B0AGN20000	128	16	Plastic • QFN32 (0.50 mm pitch), 32 pins (LCC-32P-M73)	Tray
S6E1C31B0AGN20000	64	12		
(TBD)	128	16	WLCSP (TBD)	(TBD)

48-pin plastic LQFP

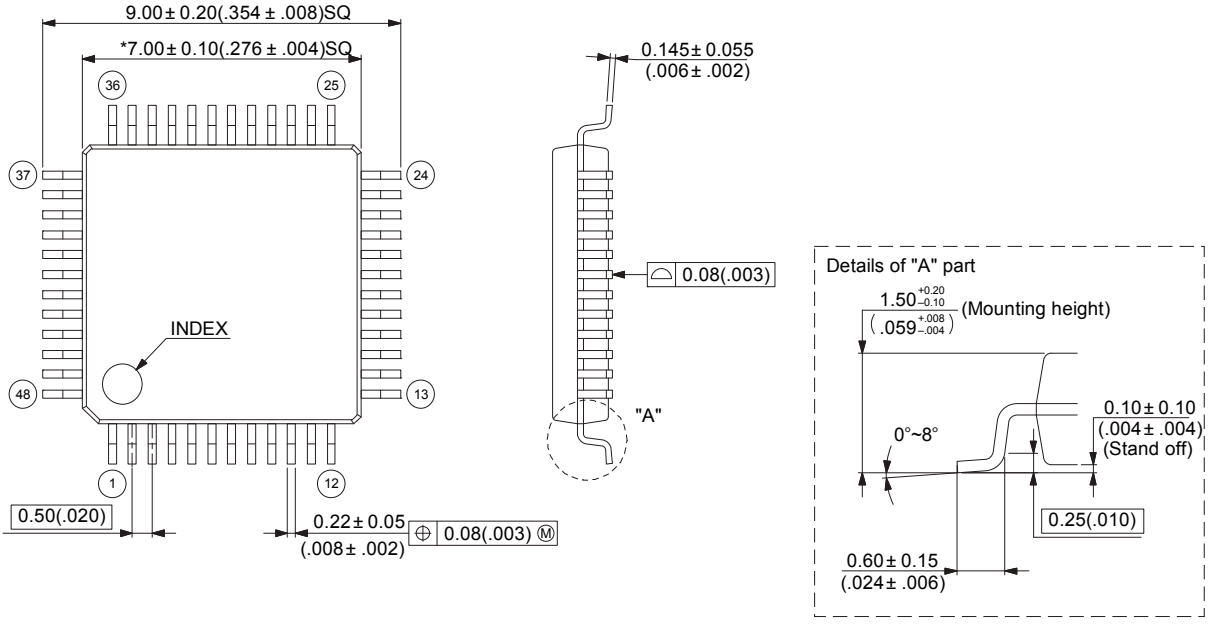


(FPT-48P-M49)

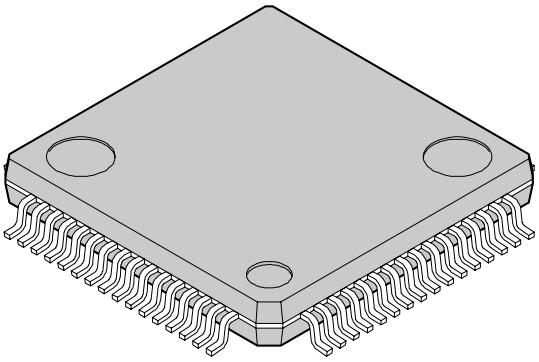
Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

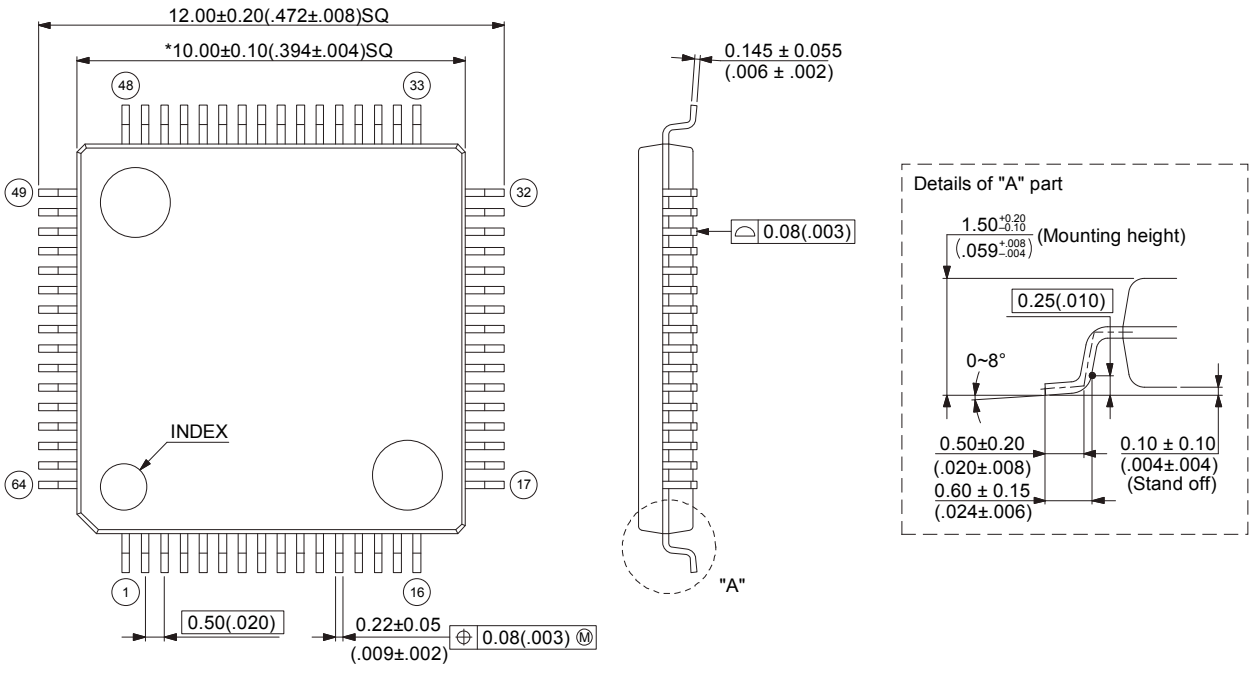


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.