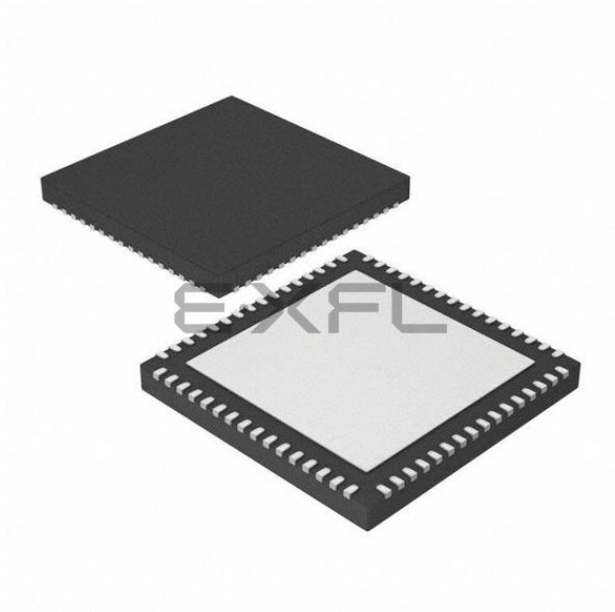


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | CSIO, I²C, LINbus, SmartCard, UART/USART, USB |
| Peripherals | I²S, LVD, POR, PWM, WDT |
| Number of I/O | 54 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 12K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-WFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c31d0agn20000 |

### I2C Slave

- I2C Slave supports the slave function of I2C and wake-up function from Standby mode.

### Descriptor System Data Transfer Controller (DSTC) (64 Channels)

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor that has already been constructed on the memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

### A/D Converter (Max: 8 Channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

### Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

### General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 54 fast general-purpose I/O ports @64-pin package
- Certain ports are 5 V tolerant.
  See 4.List of Pin Functions and 5.I/O Circuit Typefor the corresponding pins.

### Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

### Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

### Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

### External Interrupt Controller Unit

- Up to 12 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

### Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

### CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

### HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost

# 1. Product Lineup

### Memory Size

| Product name | S6E1C31B0A/ S6E1C31C0A/ S6E1C31D0A | S6E1C32B0A/ S6E1C32C0A/ S6E1C32D0A |
|---|---|---|
| On-chip Flash memory | 64 Kbytes | 128 Kbytes |
| On-chip SRAM | 12 Kbytes | 16 Kbytes |

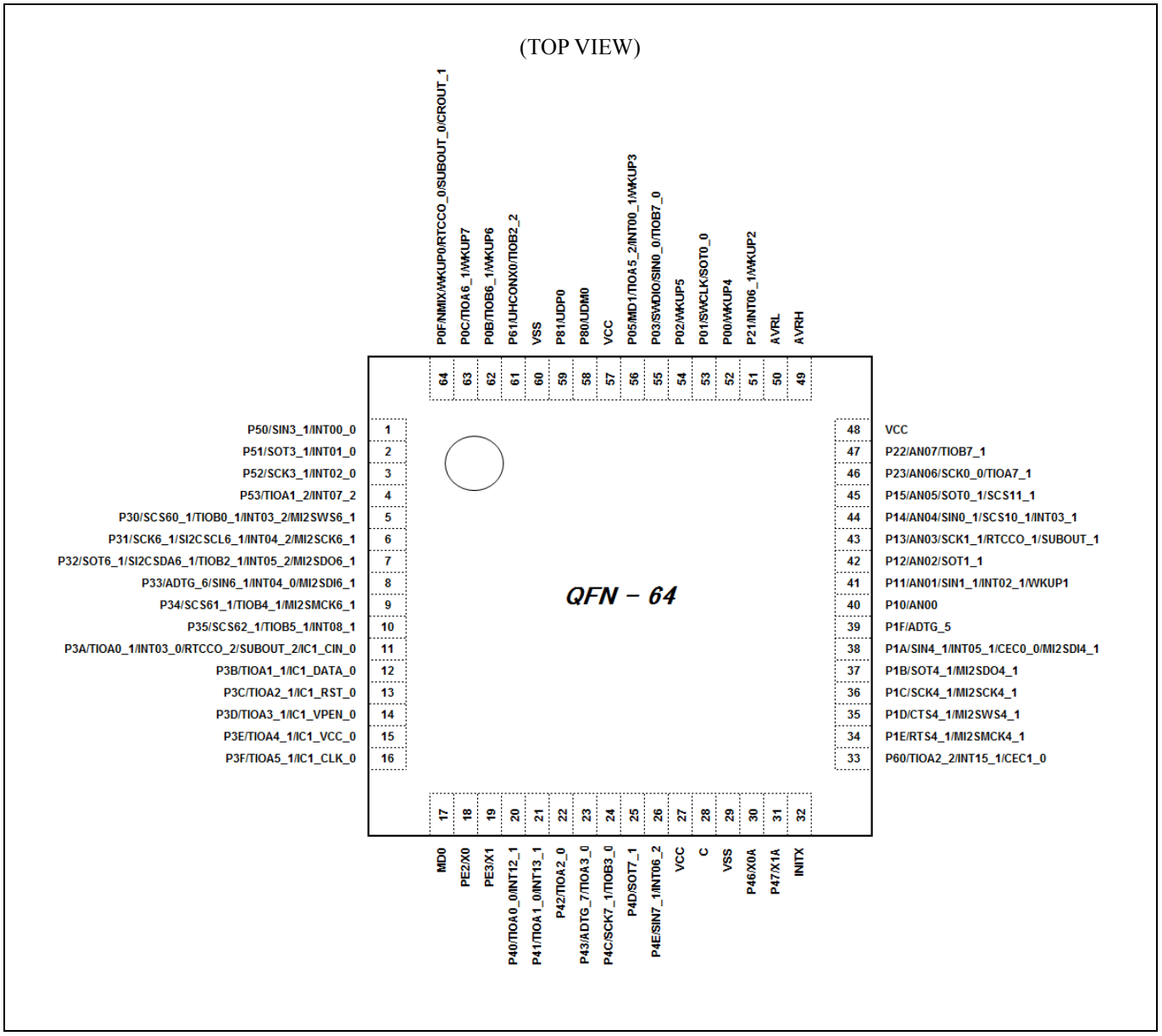
### Function

| Product name | | S6E1C32B0A (WLCSP) | S6E1C32B0A/ S6E1C31B0A | S6E1C32C0A/ S6E1C32C0A | S6E1C31D0A/ S6E1C32D0A |
|---|---|---|---|---|---|
| Pin count | | TBD | 32 | 48 | 64 |
| CPU | | Cortex-M0+ | | | |
| | Frequency | 40.8 MHz | | | |
| Power supply voltage range | | 1.65 V to 3.6 V | | | |
| USB2.0 (Device/Host) | | 1 unit | | | |
| DSTC | | 64 ch. | | | |
| Multi-function Serial Interface (UART/CSIO/I$^2$C/I2S) | | 2 ch. (Max) Ch.0/3 without FIFO | 4 ch. (Max) Ch.0/1/3 without FIFO Ch. 6 with FIFO | 6 ch. (Max) Ch.0/1/3 without FIFO Ch.4/6/7 with FIFO | 6 ch. (Max) Ch.0/1/3 without FIFO Ch.4/6/7 with FIFO |
| | | I2S : No | | I2S : 1 ch (Max) Ch. 6 with FIFO | I2S : 2 ch (Max) Ch. 4/6 with FIFO |
| Base Timer (PWC/Reload timer/PWM/PPG) | | 8 ch. (Max) | | | |
| Dual Timer | | 1 unit | | | |
| HDMI-CEC/ Remote Control Receiver | | 1 ch.(Max) Ch.1 | | 2 ch (Max) Ch.0/1 | |
| I2C Slave | | No | 1 ch (Max) | | |
| Smart Card Interface | | No | | | 1 ch (Max) |
| Real-time Clock | | 1 unit | | | |
| Watch Counter | | 1 unit | | | |
| CRC Accelerator | | Yes | | | |
| Watchdog timer | | 1 ch. (SW) + 1 ch. (HW) | | | |
| External Interrupt | | 5 pins (Max), NMI × 1 | 7 pins (Max), NMI x 1 | 9 pins (Max), NMI x 1 | 12 pins (Max), NMI x 1 |
| I/O port | | 20 pins (Max) | 24 pins (Max) | 38 pins (Max) | 54 pins (Max) |
| 12-bit A/D converter | | 4 ch (1 unit) | 6 ch. (1 unit) | 8 ch. (1 unit) | 8 ch. (1 unit) |
| CSV (Clock Supervisor) | | Yes | | | |
| LVD (Low-voltage Detection) | | 2 ch. | | | |
| Built-in CR | High-speed | 8 MHz (Typ) | | | |
| | Low-speed | 100 kHz (Typ) | | | |
| Debug Function | | SW-DP | | | |
| Unique ID | | Yes | | | |

***Note:***

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
  *See "11. Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.*

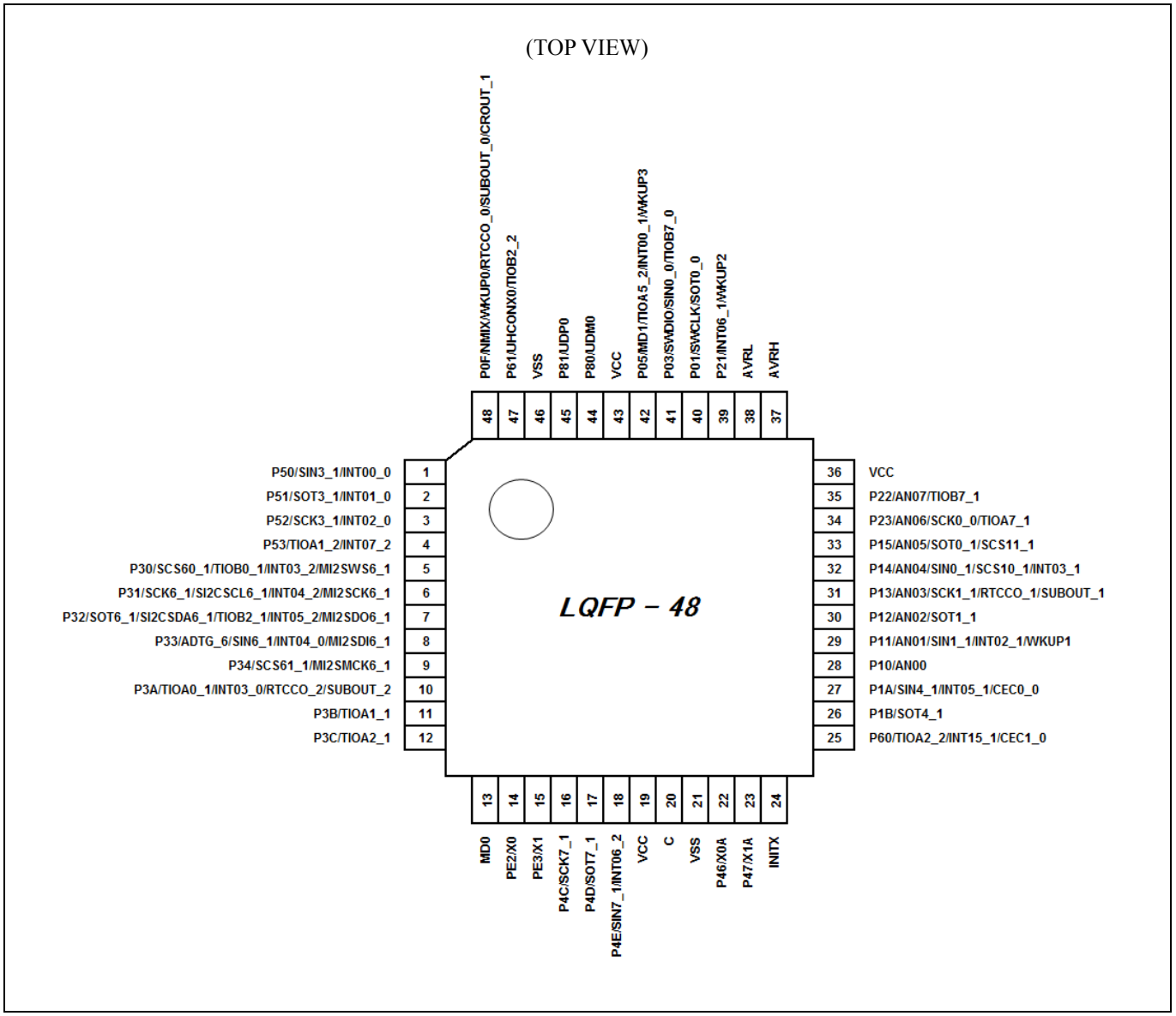
**LCC-64P-M25**




***Note:***

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

**FPT-48P-M49**




***Note:***

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) |
| I2S(MFS) | MI2SDI4_1 | I2S Serial Data Input pin (operation mode 2). | 38 | - | - | - |
| | MI2SDO4_1 | I2S Serial Data Output pin (operation mode 2). | 37 | - | - | - |
| | MI2SCK4_1 | I2S Serial Clock Output pin (operation mode 2). | 36 | - | - | - |
| | MI2SWS4_1 | I2S Word Select Output pin (operation mode 2). | 35 | - | - | - |
| | MI2SMCK4_1 | I2S Master Clock Input/output pin (operation mode 2). | 34 | - | - | - |
| | MI2SDI6_1 | I2S Serial Data Input pin (operation mode 2). | 8 | 8 | - | - |
| | MI2SDO6_1 | I2S Serial Data Output pin (operation mode 2). | 7 | 7 | - | - |
| | MI2SCK6_1 | I2S Serial Clock Output pin (operation mode 2). | 6 | 6 | - | - |
| | MI2SWS6_1 | I2S Word Select Output pin (operation mode 2). | 5 | 5 | - | - |
| | MI2SMCK6_1 | I2S Master Clock Input/output pin (operation mode 2). | 9 | 9 | - | - |
| Smart Card Interface | IC1_CIN_0 | Smart Card insert detection output pin | 11 | - | - | - |
| | IC1_CLK_0 | Smart Card serial interface clock output pin | 16 | - | - | - |
| | IC1_DATA_0 | Smart Card serial interface data input pin | 12 | - | - | - |
| | IC1_RST_0 | Smart Card reset output pin | 13 | - | - | - |
| | IC1_VCC_0 | Smart Card power enable output pin | 15 | - | - | - |
| | IC1_VPEN_0 | Smart Card programming output pin | 14 | - | - | - |
| USB | UDM0 | USB function/host D – pin | 58 | 44 | 30 | - |
| | UDP0 | USB function/host D + pin | 59 | 45 | 31 | - |
| | UHCONX0 | USB external pull-up control pin | 61 | 47 | - | - |
| Real-time Clock | RTCCO_0 | 0.5 seconds pulse output pin of real-time clock | 64 | 48 | 1 | - |
| | RTCCO_1 | | 43 | 31 | 21 | - |
| | RTCCO_2 | | 11 | 10 | - | - |
| | SUBOUT_0 | Sub clock output pin | 64 | 48 | 1 | - |
| | SUBOUT_1 | | 43 | 31 | 21 | - |
| | SUBOUT_2 | | 11 | 10 | - | - |
| HDMI-CEC/Remote Control Reception | CEC0_0 | HDMI-CEC/Remote Control Reception ch.0 input/output pin | 38 | 27 | - | - |
| | CEC1_0 | HDMI-CEC/Remote Control Reception ch.1 input/output pin | 33 | 25 | 17 | - |

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) |
| Low Power Consumption Mode | WKUP0 | Deep Standby mode return signal input pin 0 | 64 | 48 | 1 | - |
| | WKUP1 | Deep Standby mode return signal input pin 1 | 41 | 29 | 19 | - |
| | WKUP2 | Deep Standby mode return signal input pin 2 | 51 | 39 | 26 | - |
| | WKUP3 | Deep Standby mode return signal input pin 3 | 56 | 42 | 29 | - |
| | WKUP4 | Deep Standby mode return signal input pin 4 | 52 | - | - | - |
| | WKUP5 | Deep Standby mode return signal input pin 5 | 54 | - | - | - |
| | WKUP6 | Deep Standby mode return signal input pin 6 | 62 | - | - | - |
| | WKUP7 | Deep Standby mode return signal input pin 7 | 63 | - | - | - |
| I2C Slave | SI2CSCL6_1 | I2C Clock Pin | 6 | 6 | 5 | - |
| | SI2CSDA6_1 | I2C Data Pin | 7 | 7 | 6 | - |
| RESET | INITX | External Reset Input pin.<br>A reset is valid when INITX="L". | 32 | 24 | 16 | - |
| MODE | MD0 | Mode 0 pin.<br>During normal operation, input MD0="L".<br>During serial programming to Flash memory, input MD0="H". | 17 | 13 | 8 | - |
| | MD1 | Mode 1 pin.<br>During normal operation, input is not needed.<br>During serial programming to Flash memory, MD1 = "L" must be input. | 56 | 42 | 29 | - |
| CLOCK | X0 | Main clock (oscillation) input pin | 18 | 14 | 9 | - |
| | X0A | Sub clock (oscillation) input pin | 30 | 22 | 14 | - |
| | X1 | Main clock (oscillation) I/O pin | 19 | 15 | 10 | - |
| | X1A | Sub clock (oscillation) I/O pin | 31 | 23 | 15 | - |
| | CROUT_1 | Built-in high-speed CR oscillation clock output port | 64 | 48 | 1 | - |
| POWER | VCC | Power supply pin | 27 | 19 | 11 | - |
| | VCC | | 48 | 36 | 24 | - |
| | VCC | | 57 | 43 | - | - |
| GND | VSS | GND pin | 29 | 21 | 13 | - |
| | VSS | | 60 | 46 | 32 | - |
| Analog Reference | AVRH * | A/D converter analog reference voltage input pin | 49 | 37 | - | - |
| | AVRL | A/D converter analog reference voltage input pin | 50 | 38 | 25 | - |
| C pin | C | Power supply stabilization capacitance pin | 28 | 20 | 12 | - |

*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

# 7. Handling Devices

### Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVRH pin and AVRL pin near this device.

### Stabilizing Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

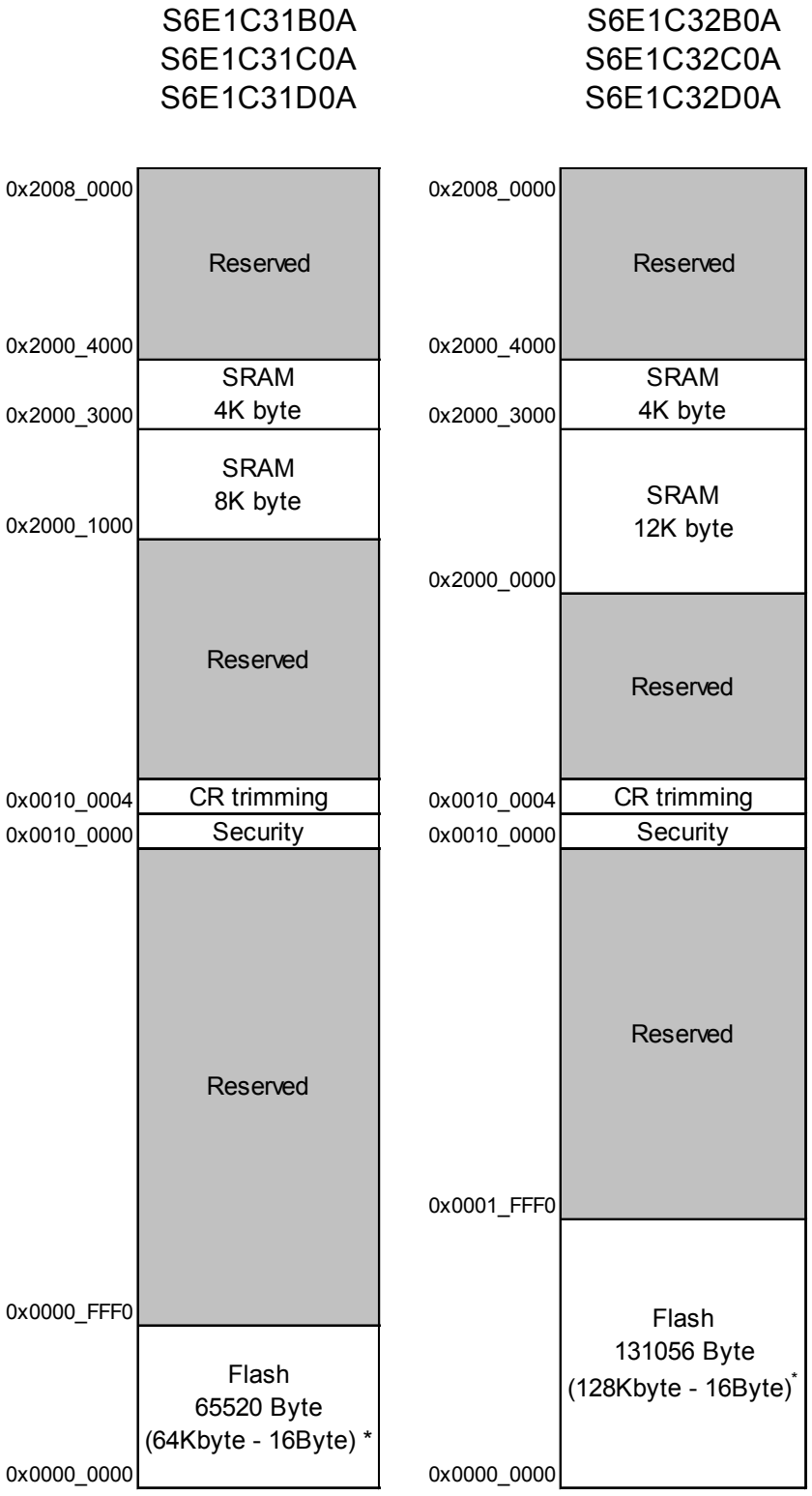
Size: More than 3.2 mm × 1.5 mm

Load capacitance: Approximately 6 pF to 7 pF

■Lead type

Load capacitance: Approximately 6 pF to 7 pF

**Memory Map (2)**




*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

| Parameter | Symbol (Pin Name) | Conditions | | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | | |
| Power supply current | $I_{CCH}$ (VCC) | Stop mode | Ta=25°C Vcc=3.3 V | 12.4 | 52.4 | µA | *1, *2 |
| | | | Ta=25°C Vcc=1.65 V | 12.0 | 52.0 | µA | *1, *2 |
| | | | Ta=105°C Vcc=3.6 V | - | 597 | µA | *1, *2 |
| | $I_{CCT}$ (VCC) | Sub timer mode | Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation | 15.6 | 55.6 | µA | *1, *2 |
| | | | Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation | 15.0 | 55.0 | µA | *1, *2 |
| | | | Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation | - | 601 | µA | *1, *2 |
| | $I_{CCR}$ (VCC) | RTC mode | Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation | 13.2 | 53.2 | µA | *1, *2 |
| | | | Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation | 12.7 | 52.7 | µA | *1, *2 |
| | | | Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation | - | 598 | µA | *1, *2 |

*1: All ports are fixed. LVD off. Flash off.

*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

### *11.4.3 Built-in CR Oscillation Characteristics*

#### Built-in High-Speed CR

($V_{CC}$= 1.65 V to 3.6 V, $V_{SS}$ = 0 V, $T_A$=- 40°C to +105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $F_{CRH}$ | Ta = - 40°C to + 105°C, | 7.84 | 8 | 8.16 | MHz | After trimming *1 |
| Frequency stabilization time | $t_{CRWT}$ | - | - | - | 300 | µs | *2 |

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

#### Built-in Low-Speed CR

($V_{CC}$= 1.65 V to 3.6 V, $V_{SS}$= 0 V, $T_A$=- 40°C to +105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_{CRL}$ | - | 50 | 100 | 150 | kHz | |

### *11.4.9 CSIO/SPI/UART Timing*

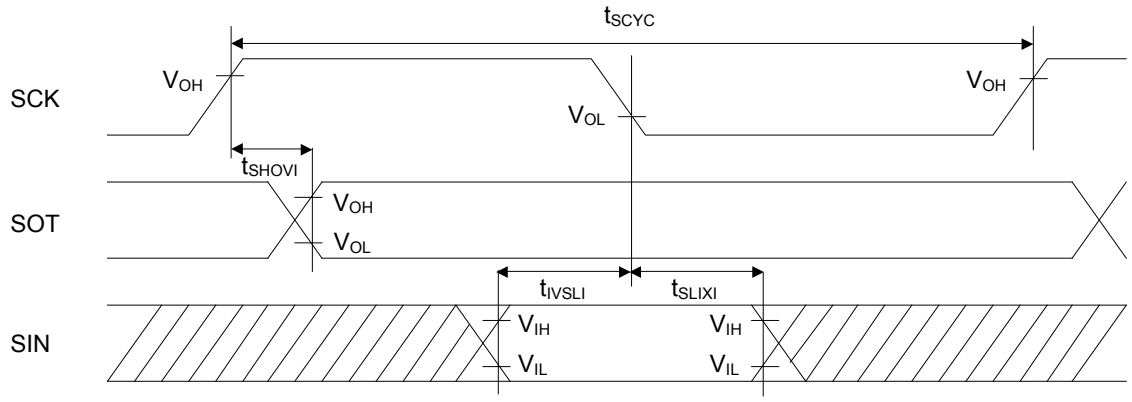
**CSIO (SPI=0, SCINV=0)**

($V_{CC}$= 1.65 V to 3.6 V, $V_{SS}$= 0 V, $T_A$=- 40°C to +105°C)

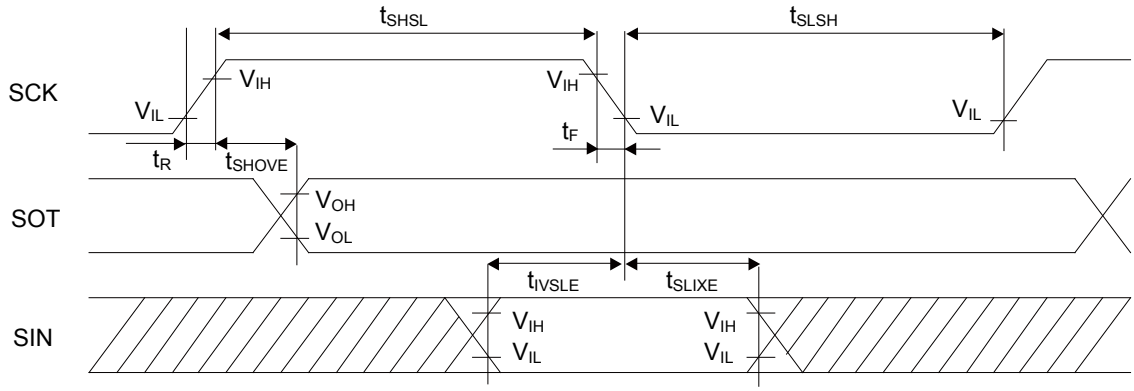
| Parameter | Symbol | Pin name | Conditions | $V_{CC}$ < 2.7 V | | $V_{CC}$ ≥ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCKx | Master mode | 4 $t_{CYCP}$ | - | 4 $t_{CYCP}$ | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCKx, SOTx | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCKx, SINx | | 50 | - | 36 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXI}$ | SCKx, SINx | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCKx | Slave mode | 2 $t_{CYCP}$ - 10 | - | 2 $t_{CYCP}$ - 10 | - | ns |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCKx | | $t_{CYCP}$ + 10 | - | $t_{CYCP}$ + 10 | - | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCKx, SOTx | | - | 50 | - | 30 | ns |
| SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCKx, SINx | | 10 | - | 10 | - | ns |
| SCK ↑ → SIN hold time | $t_{SHIXE}$ | SCKx, SINx | | 20 | - | 20 | - | ns |
| SCK falling time | tF | SCKx | | - | 5 | - | 5 | ns |
| SCK rising time | tR | SCKx | | - | 5 | - | 5 | ns |

***Notes:***

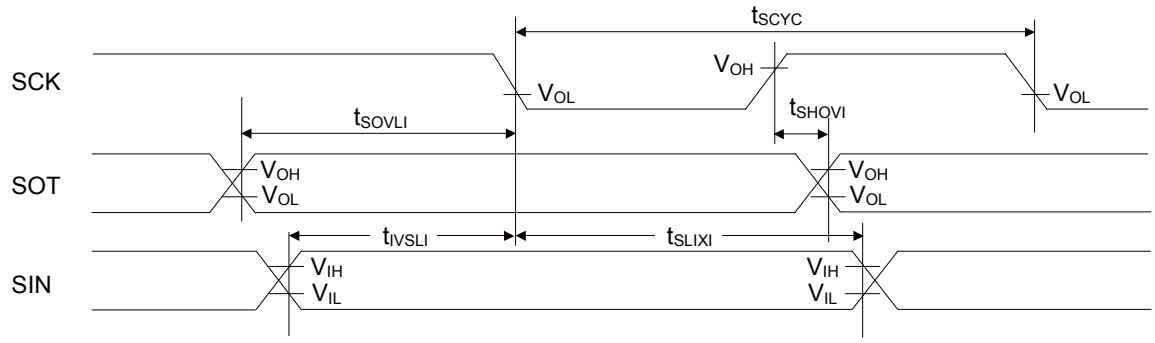
- *The above AC characteristics are for clock synchronous mode.*
- *$t_{CYCP}$ represents the APB bus clock cycle time.*
  *For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".*
- *The characteristics are only applicable when the relocate port numbers are the same.*
  *For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.*
- *External load capacitance $C_L$=30 pF*



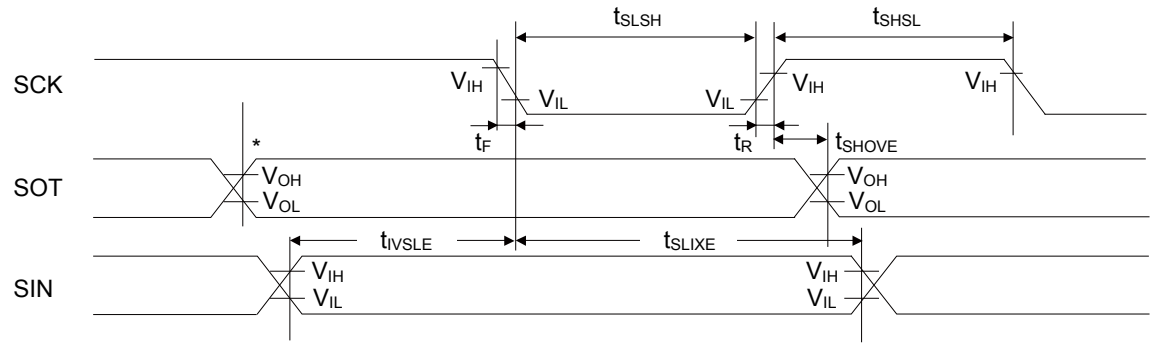

Master mode




Slave mode




Master mode



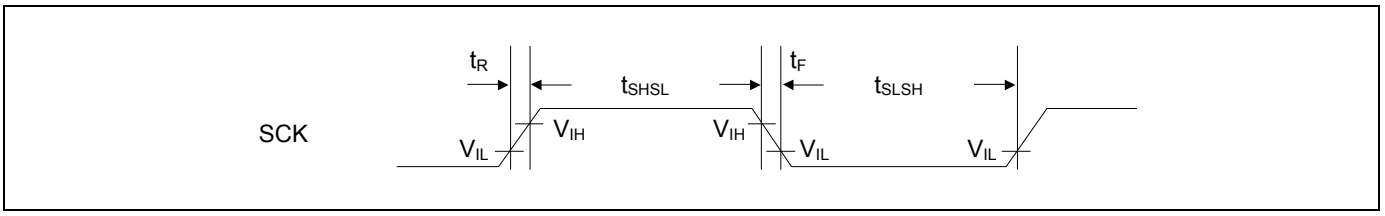

Slave mode

*: Changes when writing to TDR register

### UART external clock input (EXT=1)

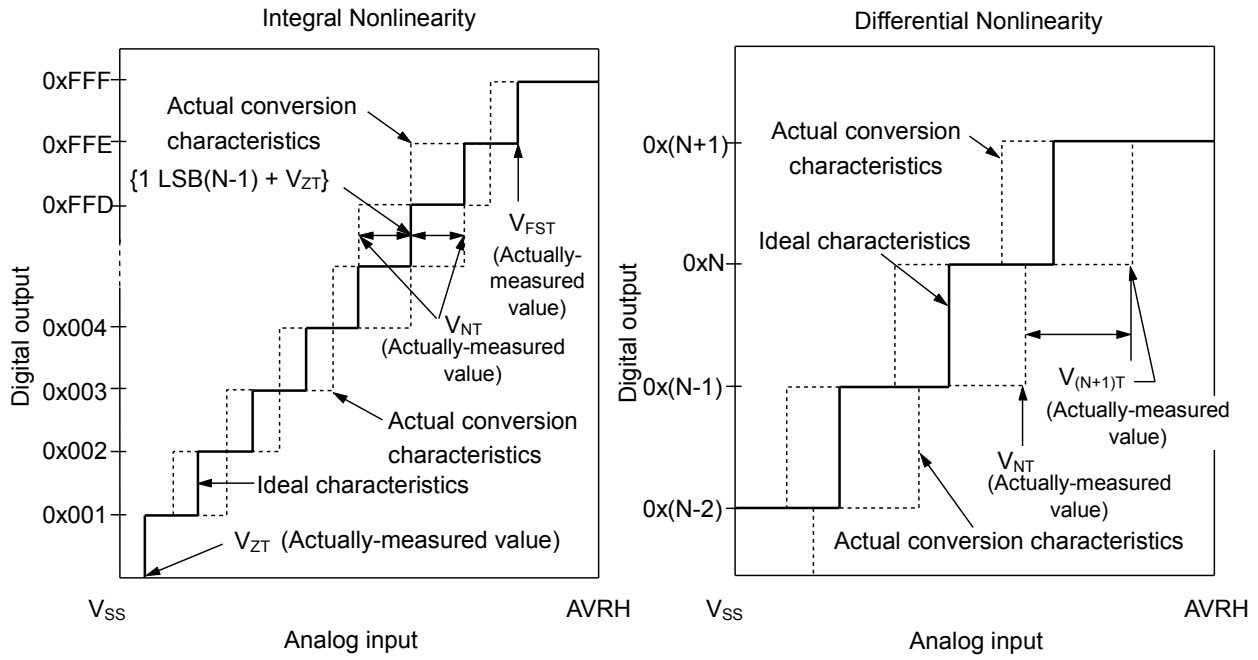
($V_{CC}$= 1.65 V to 3.6 V, $V_{SS}$= 0 V, $T_A$=- 40°C to +105°C)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Serial clock L pulse width | $t_{SLSH}$ | $C_L$=30 pF | $t_{CYCP}$ +10 | - | ns | |
| Serial clock H pulse width | $t_{SHSL}$ | | $t_{CYCP}$ +10 | - | ns | |
| SCK falling time | $t_F$ | | - | 5 | ns | |
| SCK rising time | $t_R$ | | - | 5 | ns | |



### Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.




$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
$V_{ZT}$ : Voltage at which the digital output changes from 0x000 to 0x001.
$V_{FST}$ : Voltage at which the digital output changes from 0xFFE to 0xFFF.
$V_{NT}$ : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

## 11.9 Return Time from Low-Power Consumption Mode

### *11.9.1 Return Factor: Interrupt/WKUP*

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

### Return Count Time

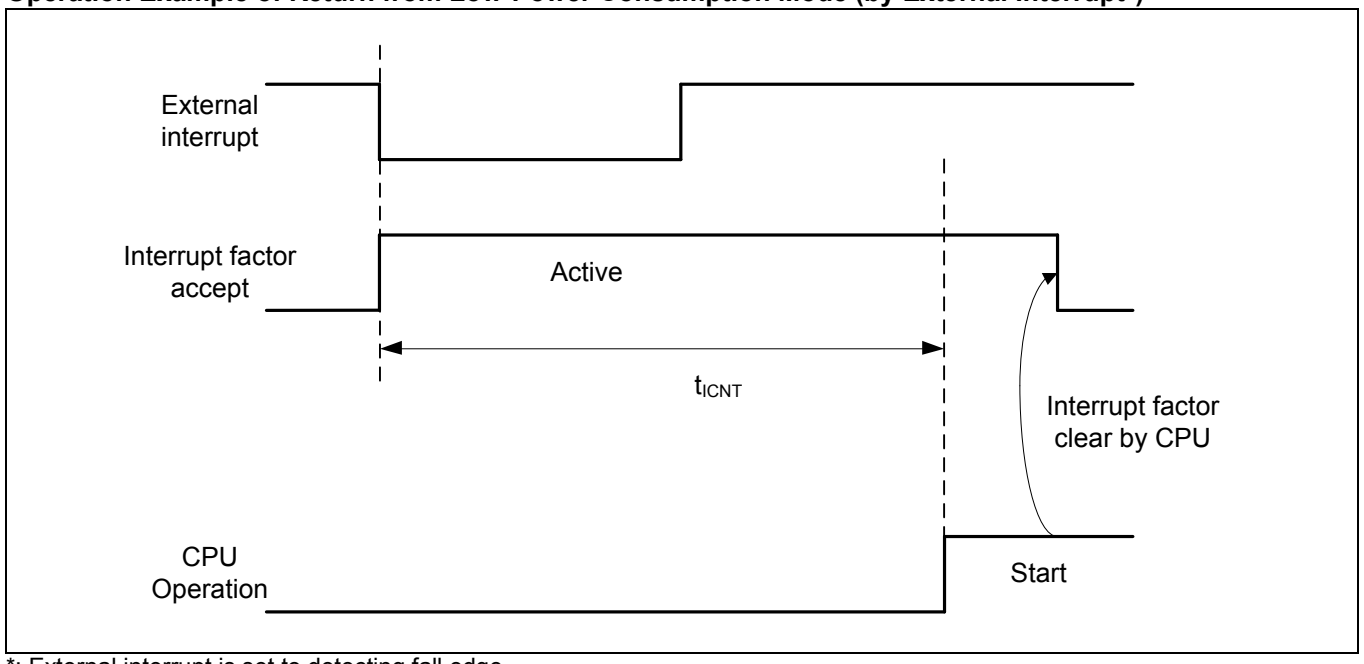
($V_{CC}$=1.65 V to 3.6 V, $T_A$=-40°C to +105°C)

| Parameter | | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| Current Mode | Mode to return | | Typ | Max *1 | | |
| Sleep mode | each Run Modes | $t_{ICNT}$ | 4*HCLK | | µs | When High-speed CR is enabled |
| Timer mode | High-speed CR Run mode<br>Main Run mode<br>PLL Run mode | | 12*HCLK | 13*HCLK | µs | When High-speed CR is enabled |
| | Low-speed CR Run mode<br>Sub Run mode | | 34+12*HCLK | 72+13*HCLK | µs | |
| Stop Mode | High-speed CR Run mode<br>Low-speed CR Run mode | | 34+12*HCLK | 72+13*HCLK | µs | |
| | Main Run mode<br>Sub Run mode<br>PLL Run mode | | 34+12*HCLK<br>+$t_{OSCWT}$ | 72+13*HCLK<br>+$t_{OSCWT}$ | µs | *2 |
| RTC mode | High-speed CR Run mode<br>Low-speed CR Run mode<br>Sub Run mode | | 34+12*HCLK | 72+13*HCLK | µs | |
| | Main Run mode<br>PLL Run mode | | 34+12*HCLK<br>+$t_{OSCWT}$ | 72+13*HCLK<br>+$t_{OSCWT}$ | µs | *2 |
| Deep Standby RTC mode<br>Deep Standby Stop mode | High-speed CR Run mode | | 43 | 281 | µs | |

*1: The maximum value depends on the condition of environment.

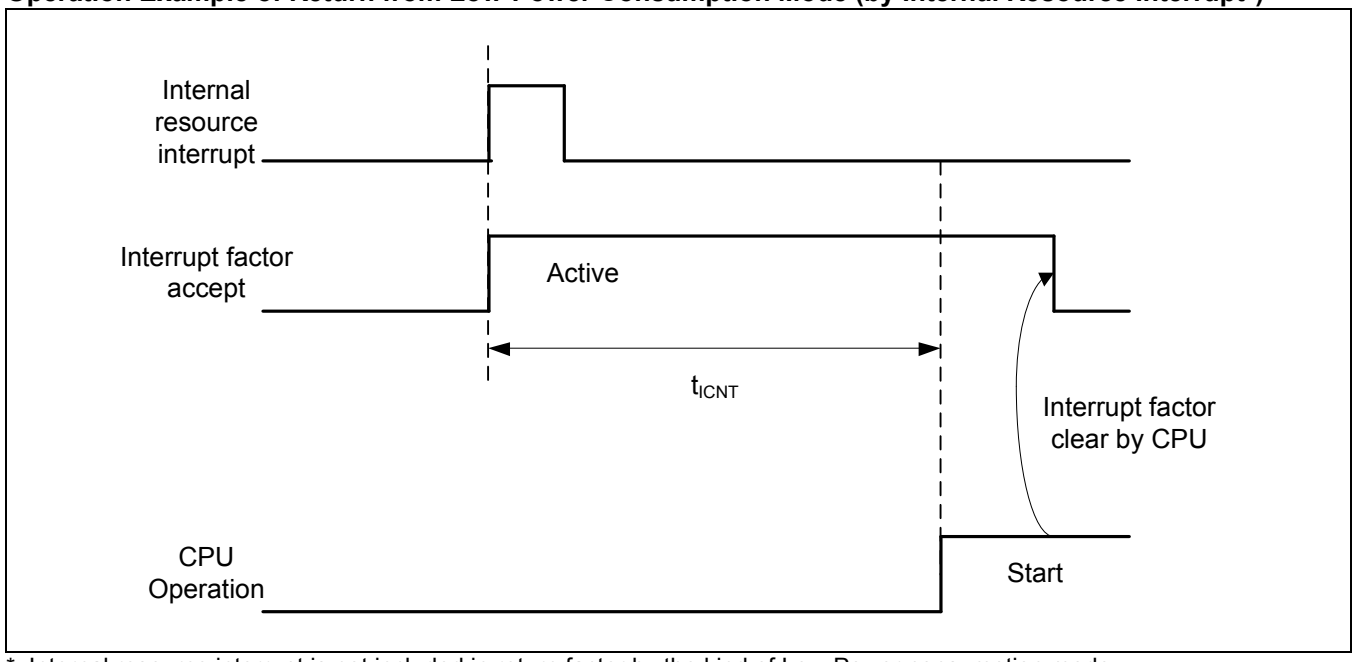
*2: $t_{OSCWT}$ : Oscillator stabilization time.

### Operation Example of Return from Low-Power Consumption Mode (by External Interrupt*)




*: External interrupt is set to detecting fall edge.

**Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt*)**

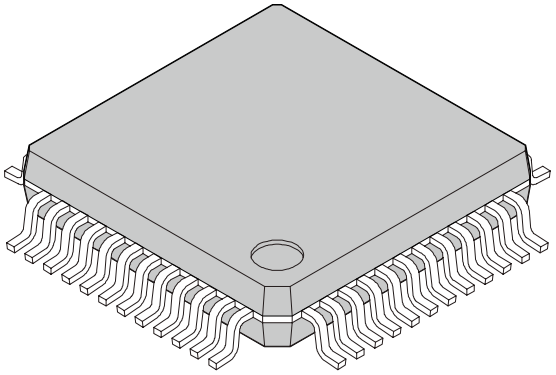



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

***Notes:***

- *The return factor is different in each Low-Power consumption modes.*
  *See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.*
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".*

48-pin plastic LQFP

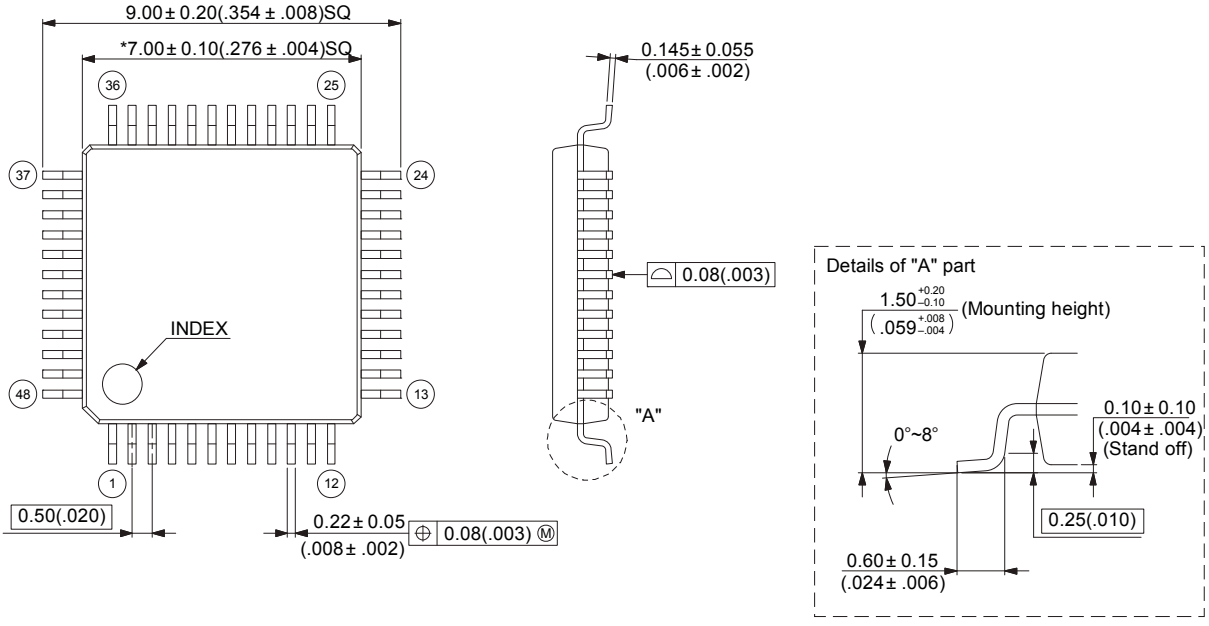


(FPT-48P-M49)

| | |
|---|---|
| Lead pitch | 0.50 mm |
| Package width × package length | 7.00 mm × 7.00 mm |
| Lead shape | Gullwing |
| Lead bend direction | Normal bend |
| Sealing method | Plastic mold |
| Mounting height | 1.70 mm MAX |
| Weight | 0.17 g |

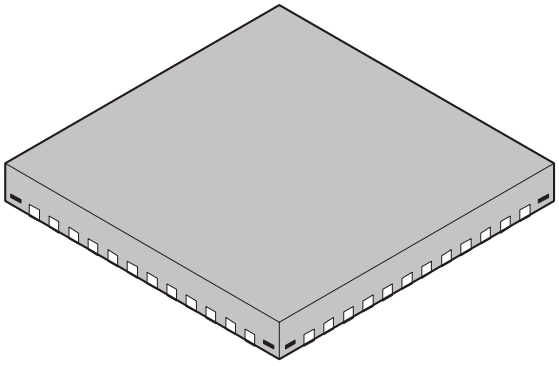
48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

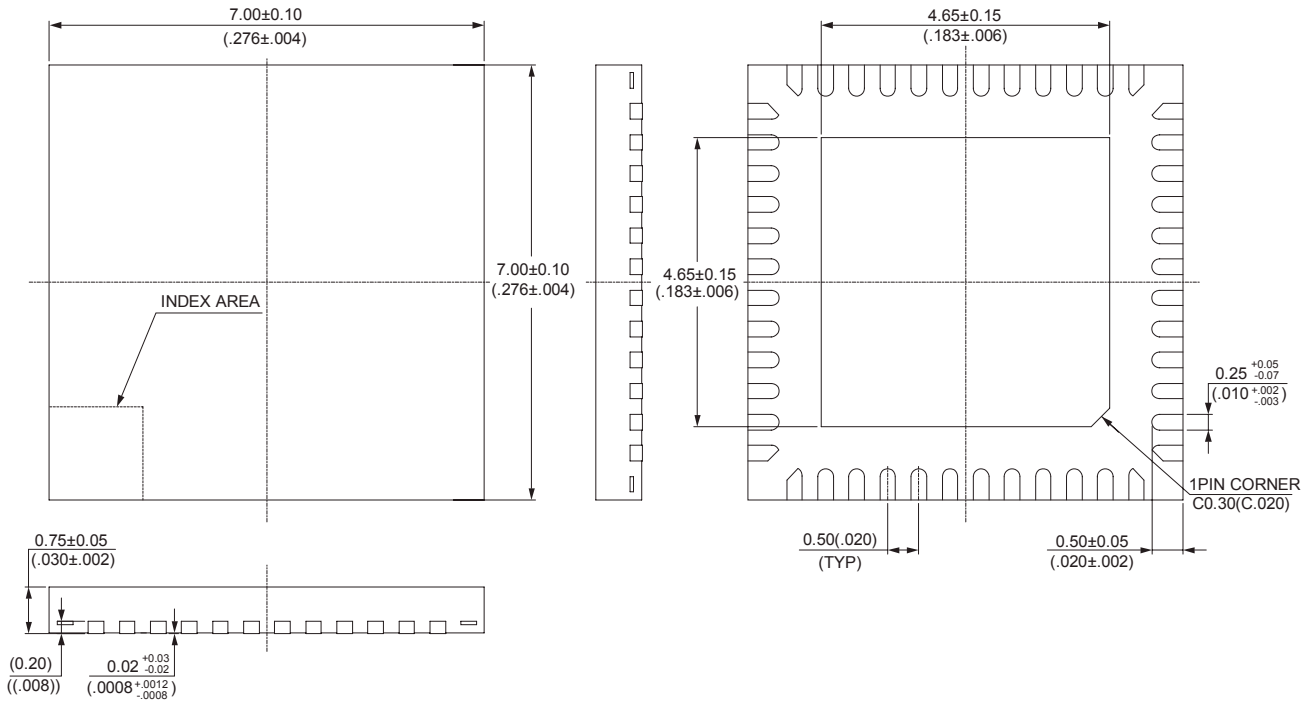





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

| 48-pin plastic QFN | | |
|---|---|---|
|  | Lead pitch | 0.50 mm |
| | Package width× package length | 7.00 mm × 7.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.80 mm MAX |
| | Weight | 0.12 g |
| | | |
| (LCC-48P-M74) | | |

48-pin plastic QFN
(LCC-48P-M74)






Dimensions in mm (inches).
Note: The values in parentheses are reference values.