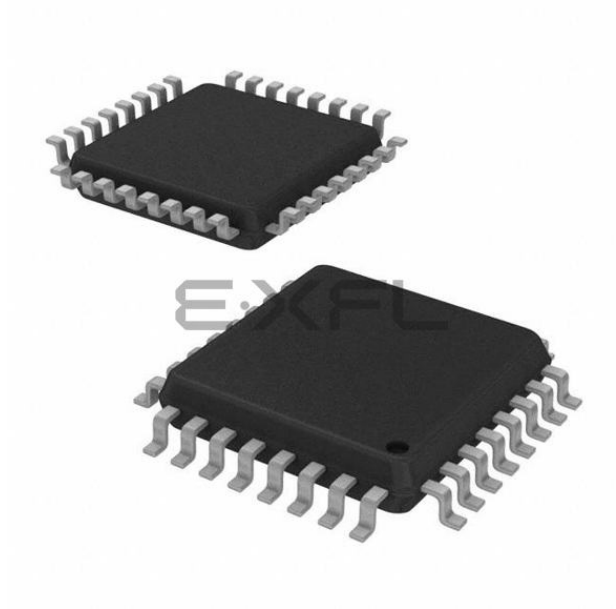

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

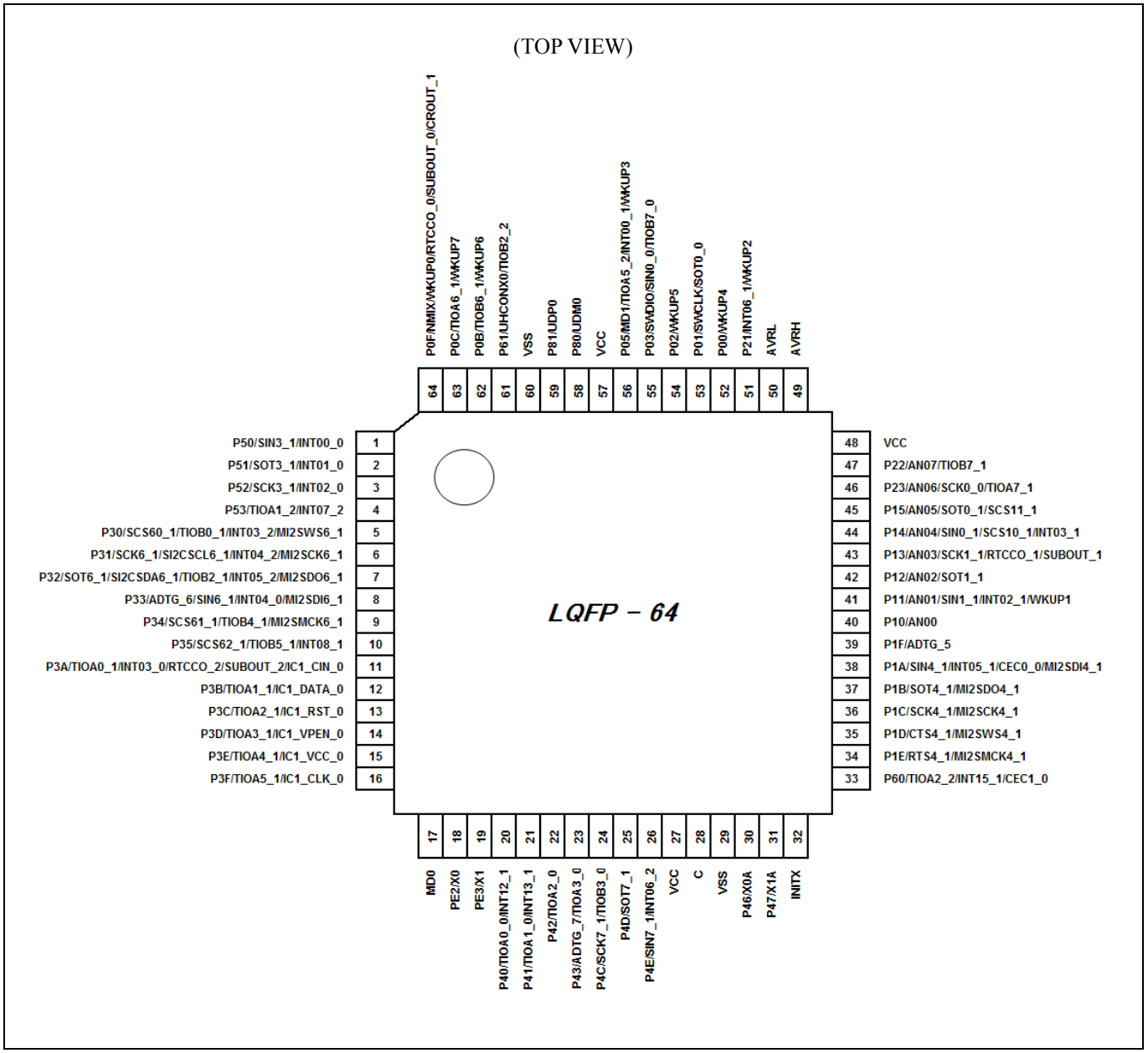
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c32b0agp20000

Sales, Solutions, and Legal Information..... 107

3. Pin Assignment

FPT-64P-M38

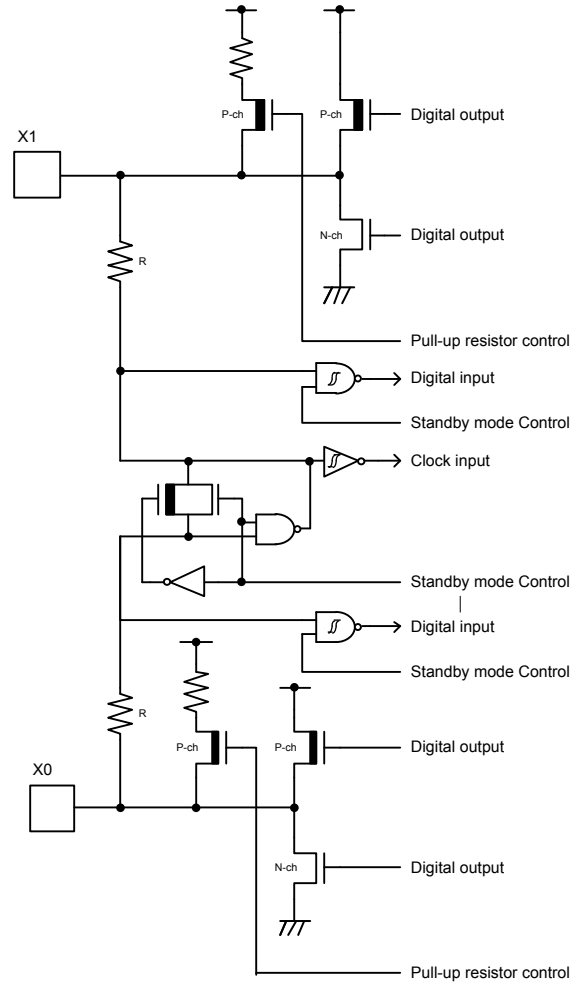
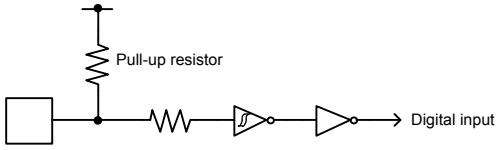


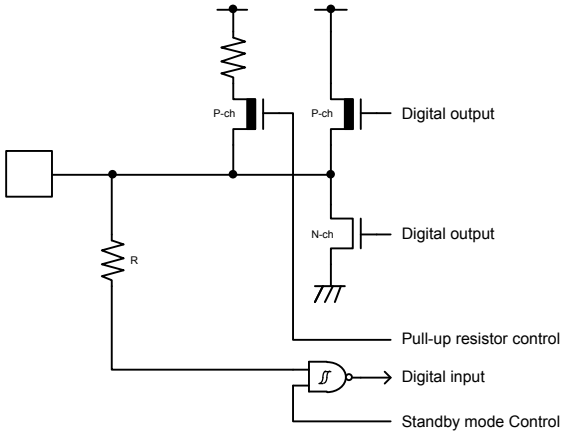
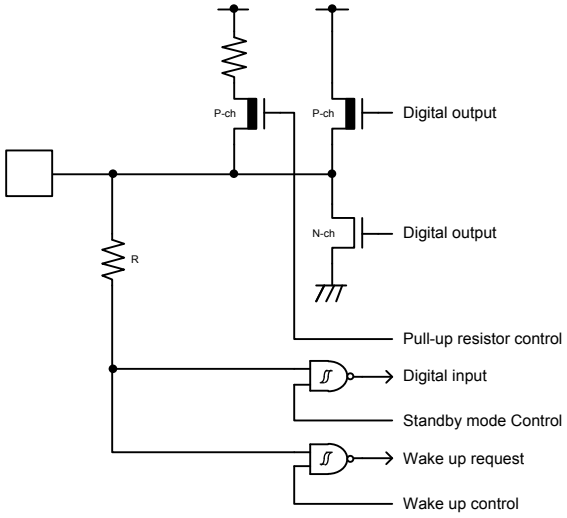
Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
I2S(MFS)	MI2SDI4_1	I2S Serial Data Input pin (operation mode 2).	38	-	-	-
	MI2SDO4_1	I2S Serial Data Output pin (operation mode 2).	37	-	-	-
	MI2SCK4_1	I2S Serial Clock Output pin (operation mode 2).	36	-	-	-
	MI2SWS4_1	I2S Word Select Output pin (operation mode 2).	35	-	-	-
	MI2SMCK4_1	I2S Master Clock Input/output pin (operation mode 2).	34	-	-	-
	MI2SDI6_1	I2S Serial Data Input pin (operation mode 2).	8	8	-	-
	MI2SDO6_1	I2S Serial Data Output pin (operation mode 2).	7	7	-	-
	MI2SCK6_1	I2S Serial Clock Output pin (operation mode 2).	6	6	-	-
	MI2SWS6_1	I2S Word Select Output pin (operation mode 2).	5	5	-	-
	MI2SMCK6_1	I2S Master Clock Input/output pin (operation mode 2).	9	9	-	-
Smart Card Interface	IC1_CIN_0	Smart Card insert detection output pin	11	-	-	-
	IC1_CLK_0	Smart Card serial interface clock output pin	16	-	-	-
	IC1_DATA_0	Smart Card serial interface data input pin	12	-	-	-
	IC1_RST_0	Smart Card reset output pin	13	-	-	-
	IC1_VCC_0	Smart Card power enable output pin	15	-	-	-
	IC1_VPEN_0	Smart Card programming output pin	14	-	-	-
USB	UDM0	USB function/host D – pin	58	44	30	-
	UDP0	USB function/host D + pin	59	45	31	-
	UHCONX0	USB external pull-up control pin	61	47	-	-
Real-time Clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	64	48	1	-
	RTCCO_1		43	31	21	-
	RTCCO_2		11	10	-	-
	SUBOUT_0	Sub clock output pin	64	48	1	-
	SUBOUT_1		43	31	21	-
	SUBOUT_2		11	10	-	-
HDMI-CEC/Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	38	27	-	-
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	33	25	17	-

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ・Oscillation feedback resistor : Approximately 1MΩ ・With standby mode control When the GPIO is selected. ・CMOS level output. ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA
B		CMOS level hysteresis input Pull-up resistor : Approximately 33kΩ

Type	Circuit	Remarks
D		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・IOH= -4mA, IOL= 4mA ・When this pin is used as an I2C pin, the digital output P-ch transistor is always off

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VCC →AVRH
Turning off : AVRH →VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

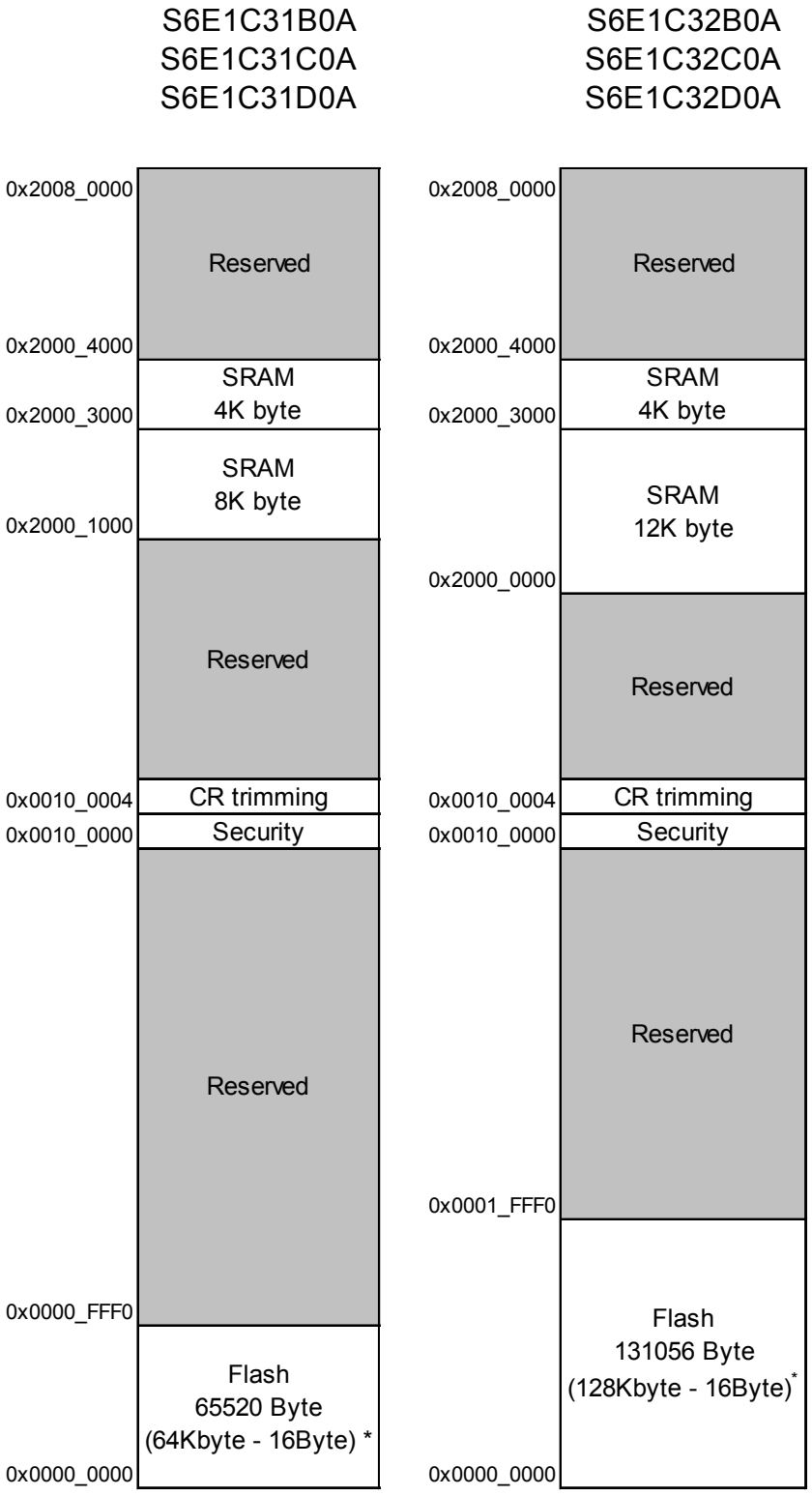
Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

Memory Map (2)



*: See "S6E1C1/C3 Series Flash Programming Manual" to check details of the Flash memory.

Each term in above table have the following meanings.

Type
This indicates a pin status type that is shown in “pin list table” in “4. List of Pin Functions”

Selected Pin function
This indicates a pin function that is selected by user program.

CPU state
This indicates a state of the CPU that is shown below.

(1) Reset state. CPU is initialized by Power-on reset or a reset due to low Power voltage supply.

(2) Reset state. CPU is initialized by INITX input signal or system initialization after power on reset.

(3) Run mode or SLEEP mode state.

(4) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

(5) Timer mode, RTC mode or STOP mode state.
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

(6) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0"

(7) Deep standby STOP mode or Deep standby RTC mode state,
The standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1"

(8) Run mode state after returning from Deep Standby mode.
(I/O state hold function(CONTX) is fixed at 1)

11.2 Recommended Operating Conditions

(V_{SS}= 0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65 *3	3.6	V	
			3.0	3.6	V	*1
Analog reference voltage	AVRH	-	2.7	V_{CC}	V	V_{CC} ≥ 2.7 V
			V_{CC}	V_{CC}	V	V_{CC} < 2.7 V
	AVRL	-	VSS	VSS	V	
Smoothing capacitor	C_S	-	1	10	µF	For regulator*2
Operating temperature	Ta	-	- 40	+ 105	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

*3: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

LVD Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.15	0.3	µA	For occurrence of reset
				0.10	0.3	µA	For occurrence of interrupt

Bipolar Vref Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Bipolar Vref Current	I_{CCBGR}	VCC	At operation	100	200	µA	

Flash Memory Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	4.4	5.6	mA	

A/D converter Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

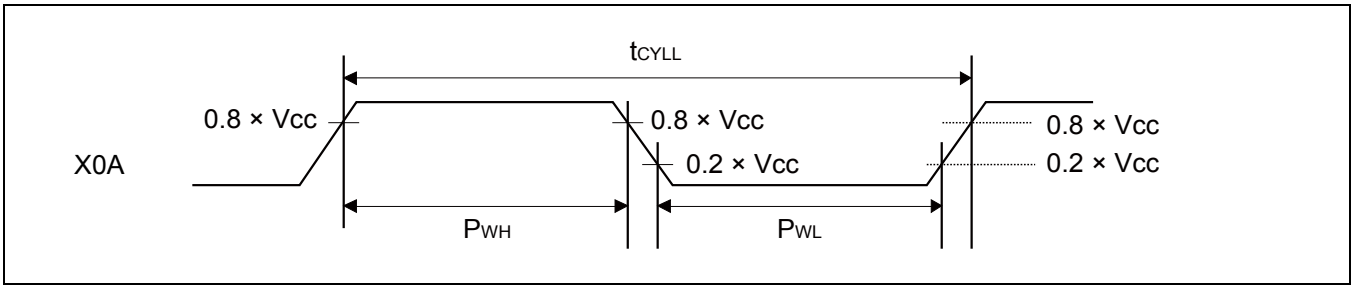
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	VCC	At operation	0.5	0.75	mA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	0.69	1.3	mA	AVRH=3.6 V
			At stop	0.1	1.3	µA	

11.4.2 Sub Clock Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	f_{CL}	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.



11.4.3 Built-in CR Oscillation Characteristics

Built-in High-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS} = 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = - 40°C to + 105°C,	7.84	8	8.16	MHz	After trimming *1
Frequency stabilization time	t_{CRWT}	-	-	-	300	µs	*2

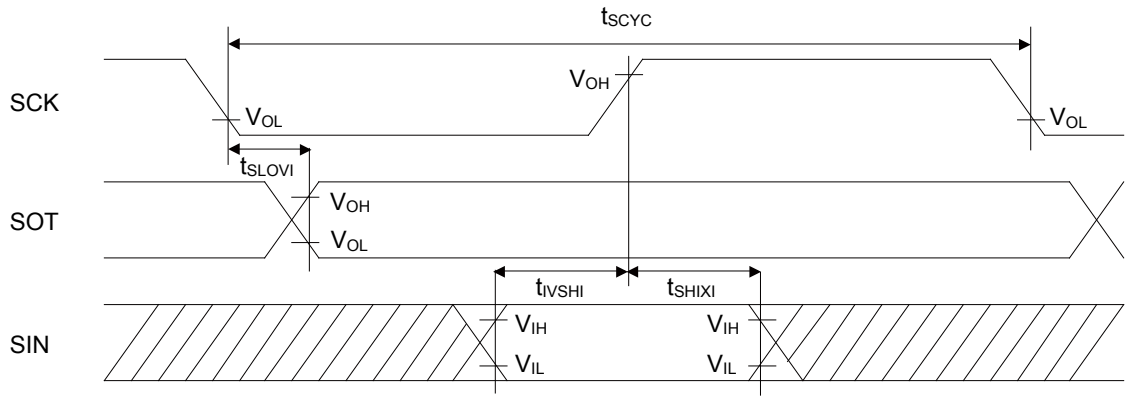
*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

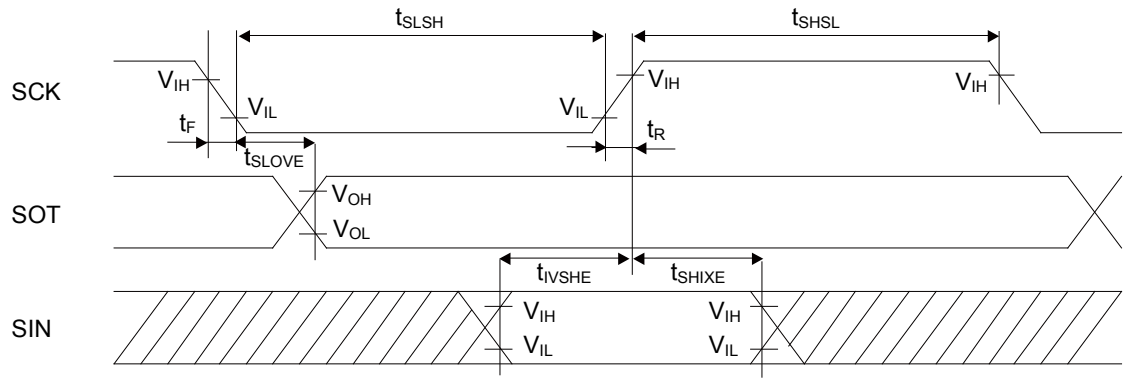
Built-in Low-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	



Master mode



Slave mode

SPI (SPI=1, SCINV=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS↓→SCK↑ setup time	t_{CSSE}	Slave mode	$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		$3t_{CYCP}$+30	-	$3t_{CYCP}$+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	55	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

*1: CSSU bit value × serial chip select timing operating clock cycle.

*2: CSHD bit value × serial chip select timing operating clock cycle.

*3: CSDS bit value × serial chip select timing operating clock cycle.
Irrespective of CSDS bit setting, $5t_{CYCP}$ or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- *For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".*
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SCSIx_1 is not guaranteed.
- *When the external load capacitance C_L=30 pF.*

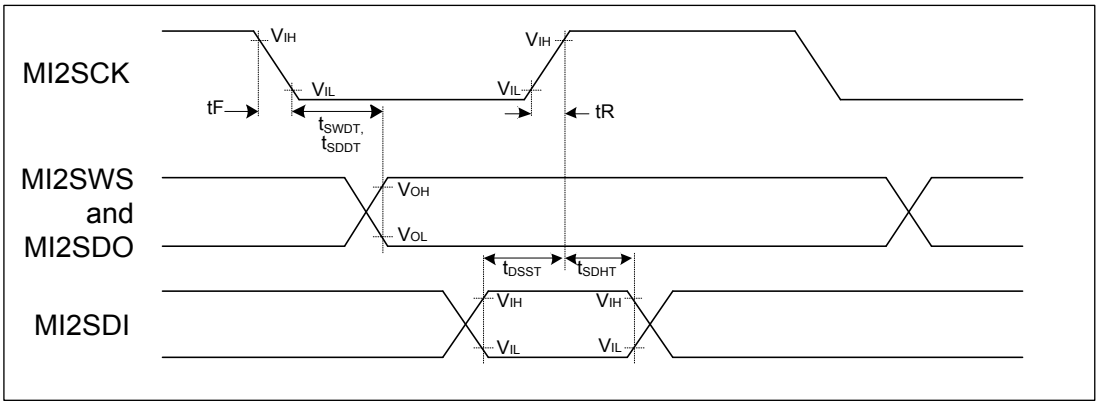
11.4.12 I^2S Timing (MFS-I2S Timing)

Master Mode Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

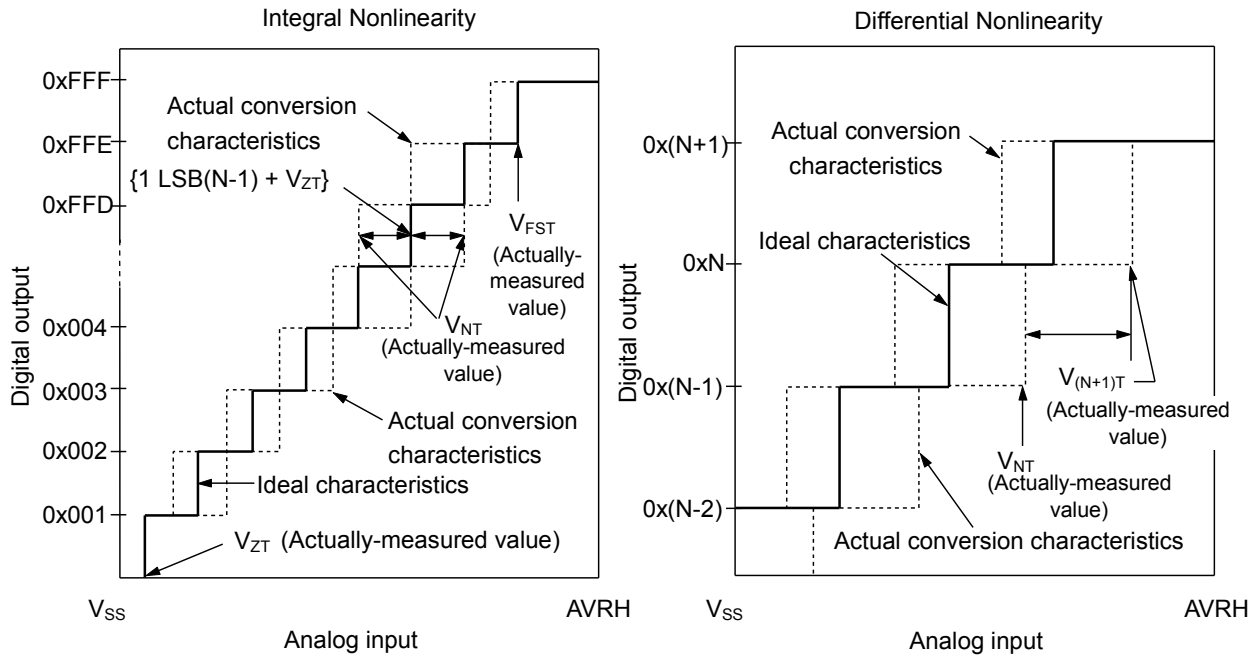
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency (*1)	F_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I^2S clock cycle time (*1)	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I^2S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	tF	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	tR	MI2SCKx		-	5	-	5	ns

*1: I^2S clock should meet the multiple of PCLK(t_{ICYC}) and the frequency less than F_{MI2SCK} meantime. The detail information please refer to Chapter I^2S of Communication Macro Part of Peripheral Manual.



Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



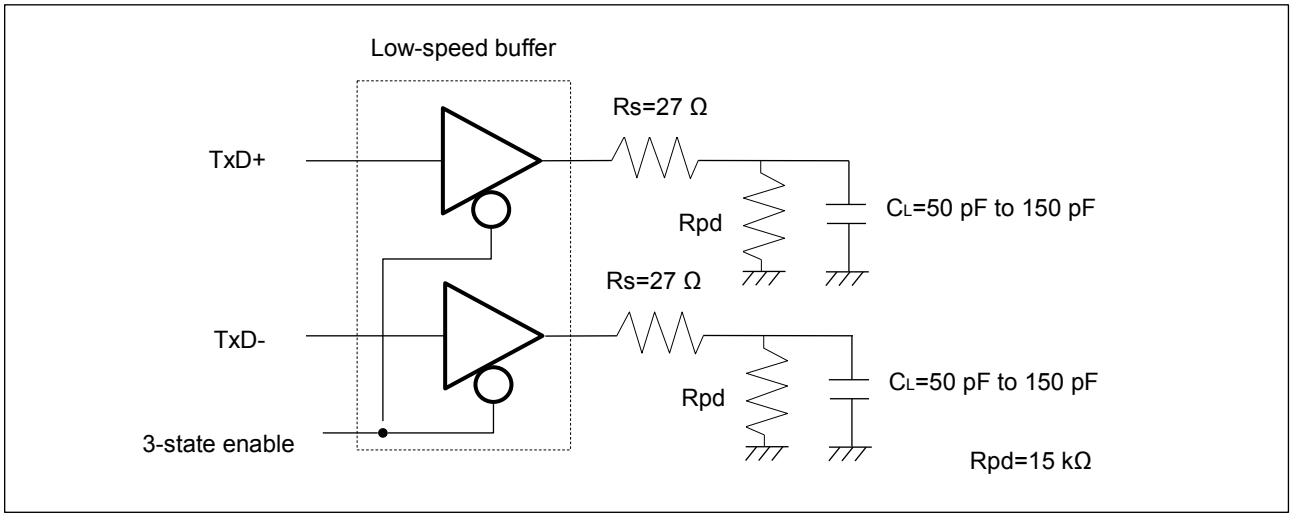
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

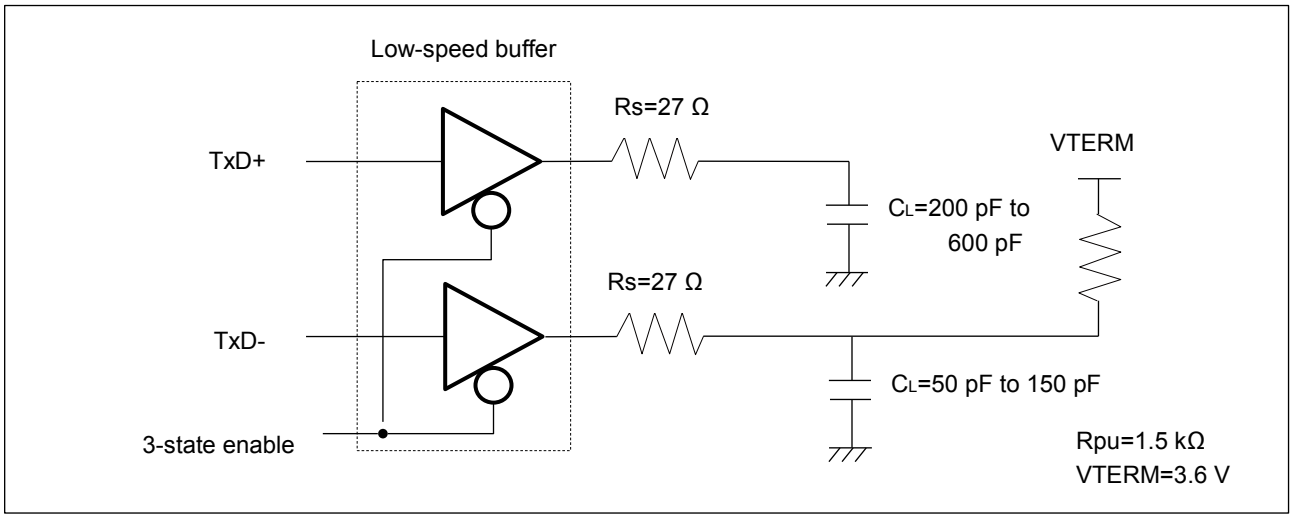
$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

- Low-Speed Load (Upstream Port Load) – Reference 1



- Low-Speed Load (Downstream Port Load) – Reference 2



11.7 Low-Voltage Detection Characteristics

11.7.1 Low-Voltage Detection Reset

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	Fixed*1	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}*2	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: The value of low voltage detection reset is always fixed.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

11.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

Return Count Time

(V_{CC}=1.65 V to 3.6 V, T_A=-40°C to +105°C)

Parameter		Symbol	Value		Unit	Remarks
Current Mode	Mode to return		Typ	Max*		
High-speed CR Sleep mode Main Sleep mode PLL Sleep mode	High-speed CR Run mode	t_{RCNT}	20	22	µs	When High-speed CR is enabled
Low-speed CR Sleep mode			50	106	µs	When High-speed CR is enabled
Sub Sleep mode			112	137	µs	When High-speed CR is enabled
High-speed CR Timer mode Main Timer mode PLL Timer mode			20	22	µs	When High-speed CR is enabled
Low-speed CR Timer mode			87	159	µs	
Sub Timer mode			148	209	µs	
Stop mode RTC mode			45	68	µs	
Deep Standby RTC mode Deep Standby Stop mode			43	281	µs	

*: The maximum value depends on the accuracy of built-in CR.

Operation Example of Return from Low-Power Consumption Mode (by INITX)