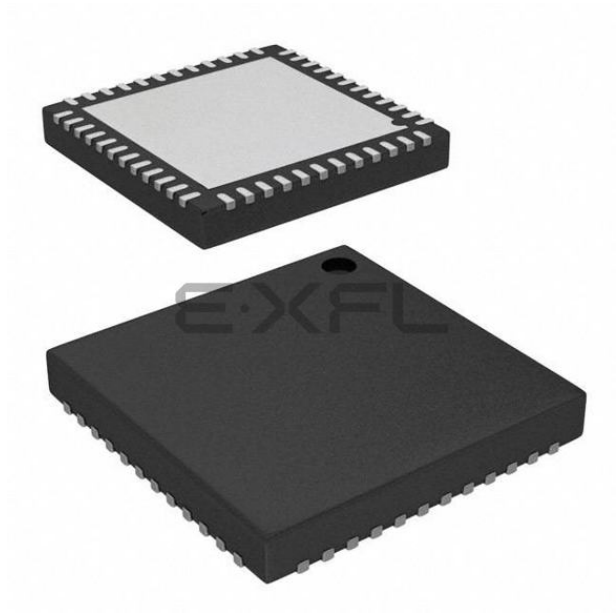


Welcome to E-XFL.COM

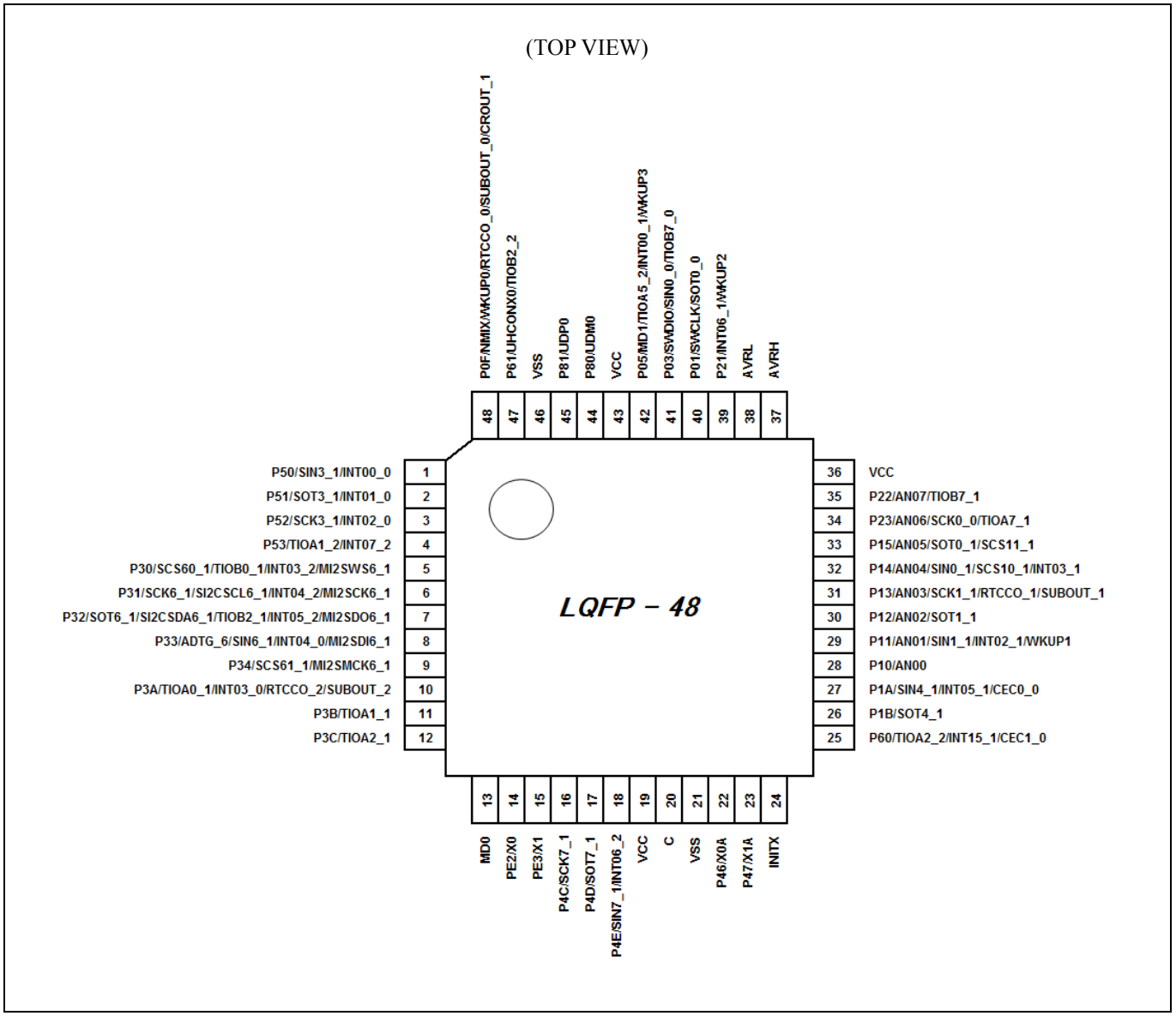
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c32c0agn20000

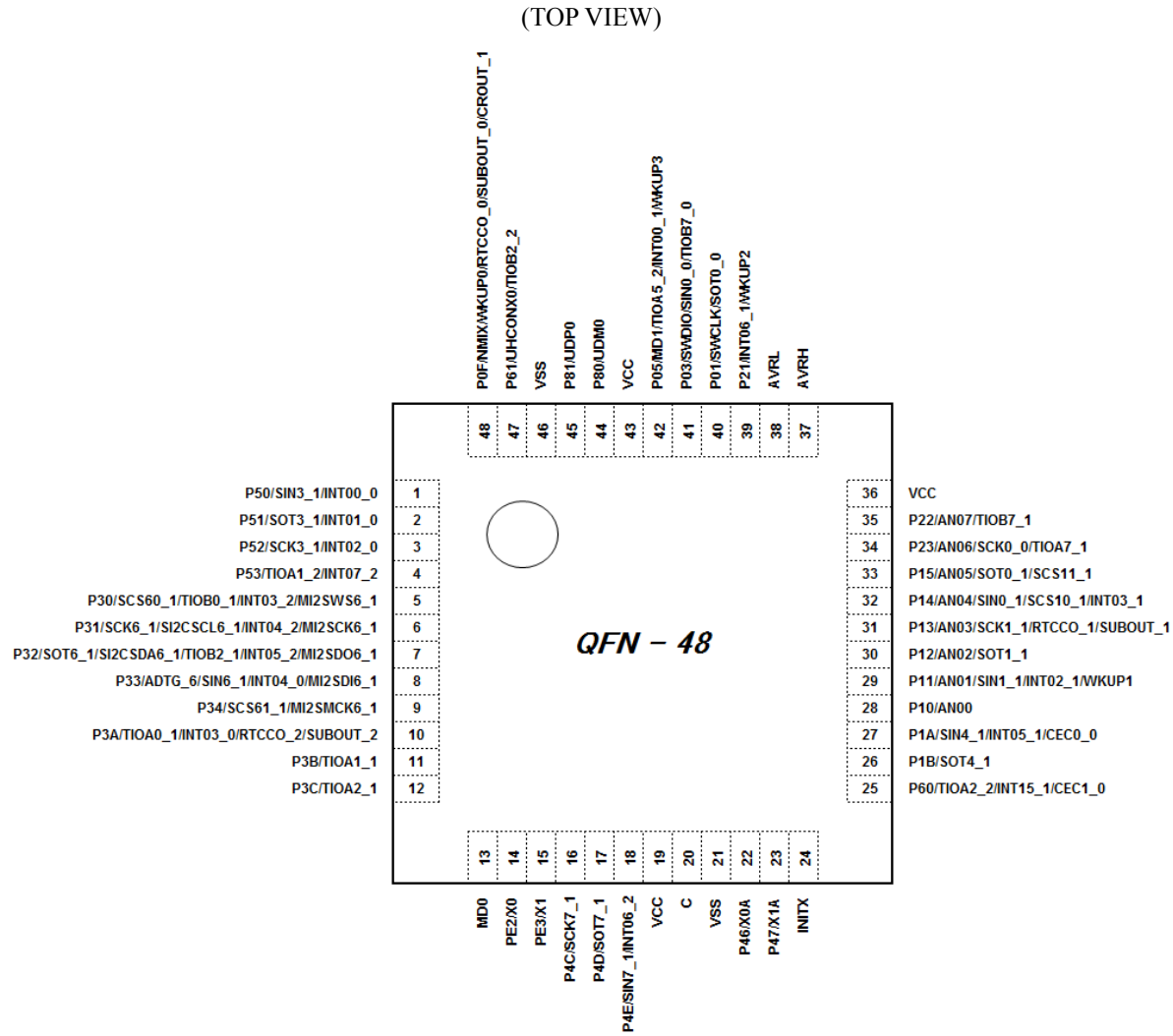
FPT-48P-M49



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

LCC-48P-M74



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

WLCSP

TBD

Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	41	29	19	-
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I2C pin (operation mode 4).	42	30	20	-
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I2C pin (operation mode 4).	43	31	21	-
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 input/output pin.	44	32	-	-
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	45	33	-	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	1	1	2	-
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I2C pin (operation mode 4).	2	2	3	-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I2C pin (operation mode 4).	3	3	4	-
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I2C pin (operation mode 4).	37	26	-	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I2C pin (operation mode 4).	36	-	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-	-

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

Notes on Power-on

Turn power on/off in the following order or at the same time.

Turning on : VCC →AVRH
Turning off : AVRH →VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Handling when Using Debug Pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

Each pin status

The meaning of the symbols in the pin status table is as follows.

IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off by fixed 0.
IE	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is not shut off.
IP	Digital output is disabled. (Hi-Z) Pull up register is defined by the value of the PCR register. Digital input is not shut off.
IE/IS	Digital output is disabled. (Hi-Z) Pull up register is off. Digital input is shut off in case of the OSC stop. Digital input is not shut off in case of the OSC operation.
OE	The OSC is in operation state. However, it may be stopped in some operation mode of the CPU. For detail, see chapter “Low Power Consumption Mode” in peripheral manual.
OS	The OSC is in stop state. (Hi-Z)
UE	USB I/O function is controlled by USB controller.
US	USB I/O function is disabled(Hi-Z)
PC	Digital output and pull up register is controlled by the register in the GPIO or peripheral function. Digital input is not shut off
CP	Digital output is controlled by the register in the GPIO or peripheral function. Pull up register is off. Digital input is not shut off.
HC	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is not shut off
HS	Digital output and pull up register is maintained the status that is immediately prior to entering the current CPU state. Digital input is shut off
GS	Digital output and pull up register is copied the GPIO status that is immediately prior to entering the current CPU state and the status is maintained. Digital input is shut off

Additional note

Additional note is described below.

*1	In this type, when internal oscillation function is selected, digital output is disabled. (Hi-Z) pull up register is off, digital input is shut off by fixed 0.
*2	In this type, when Digital I/O function is selected, internal oscillation function is disabled.
*3	In this type, when analog input function is selected, digital output is disabled, (Hi-Z). pull up register is off, digital input is shut off by fixed 0.
*4	In this type, when Digital I/O function is selected, analog input function is not available.
*5	In this case, PCR register is initialized to “1”. Pull up register is on.
*6	In this type, when Digital I/O function is selected, USB I/O function is disabled. This pin does not have pull up register.
*7	In this type, when USB I/O function is selected, digital output is disabled. (Hi-Z), digital input is shut off by fixed 0.

Parameter	Symbol (Pin Name)	Conditions		Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCH} (VCC)	Stop mode	Ta=25°C Vcc=3.3 V	12.4	52.4	µA	*1, *2
			Ta=25°C Vcc=1.65 V	12.0	52.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V	-	597	µA	*1, *2
	I_{CCT} (VCC)	Sub timer mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	15.6	55.6	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	15.0	55.0	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	601	µA	*1, *2
	I_{CCR} (VCC)	RTC mode	Ta=25°C Vcc=3.3 V 32 kHz Crystal oscillation	13.2	53.2	µA	*1, *2
			Ta=25°C Vcc=1.65 V 32 kHz Crystal oscillation	12.7	52.7	µA	*1, *2
			Ta=105°C Vcc=3.6 V 32 kHz Crystal oscillation	-	598	µA	*1, *2

*1: All ports are fixed. LVD off. Flash off.

*2: When CALDONE bit(CAL_CTL:CALDONE) is “1”. In case of “0”, Bipolar Vref current is added.

LVD Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.15	0.3	µA	For occurrence of reset
				0.10	0.3	µA	For occurrence of interrupt

Bipolar Vref Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Bipolar Vref Current	I_{CCBGR}	VCC	At operation	100	200	µA	

Flash Memory Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	4.4	5.6	mA	

A/D converter Current

(V_{CC}=1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	VCC	At operation	0.5	0.75	mA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	0.69	1.3	mA	AVRH=3.6 V
			At stop	0.1	1.3	µA	

11.4.3 Built-in CR Oscillation Characteristics

Built-in High-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS} = 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = - 40°C to + 105°C,	7.84	8	8.16	MHz	After trimming *1
Frequency stabilization time	t_{CRWT}	-	-	-	300	µs	*2

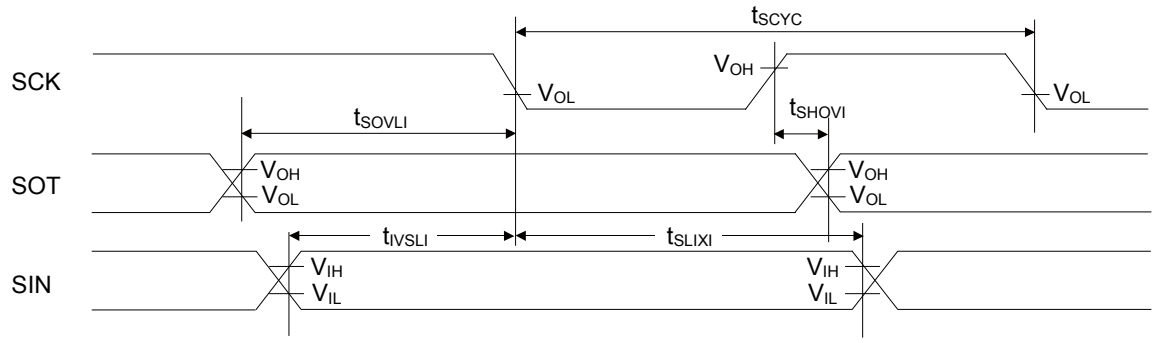
*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

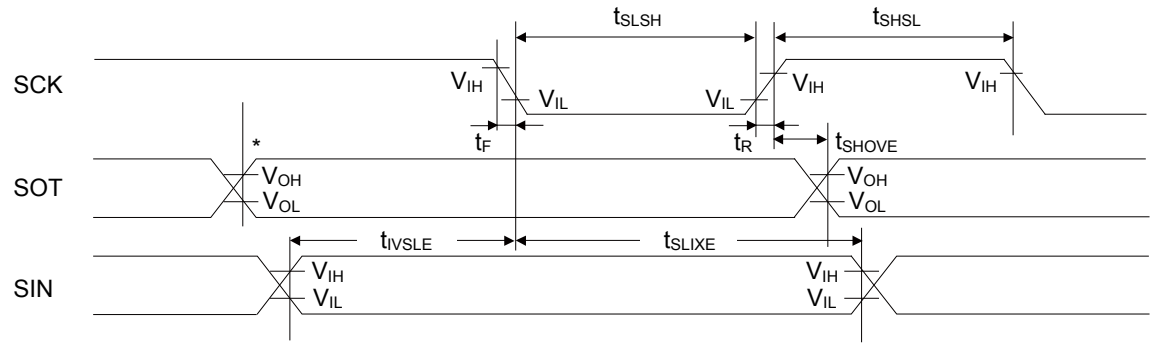
Built-in Low-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

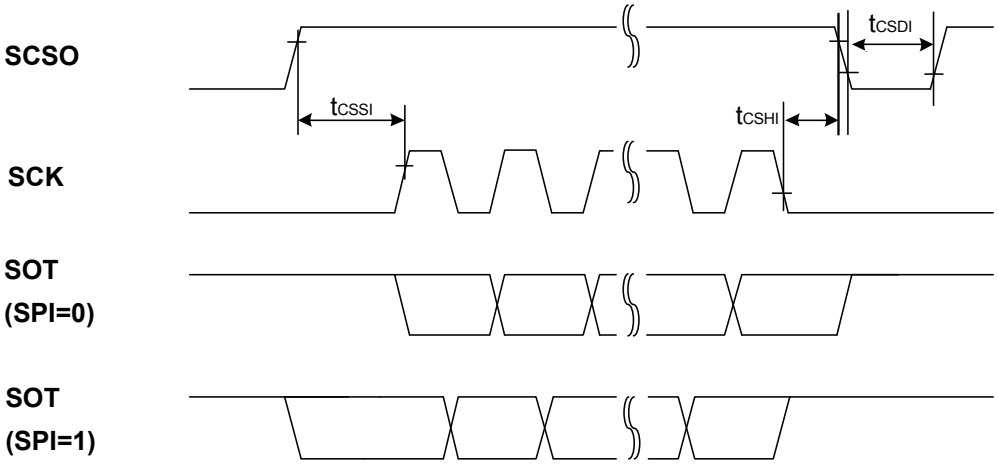


Master mode

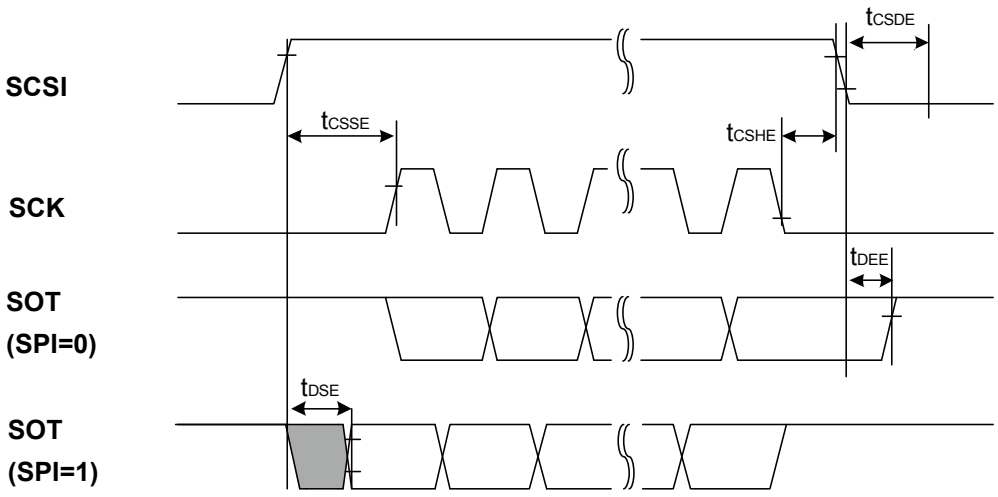


Slave mode

*: Changes when writing to TDR register



Master mode

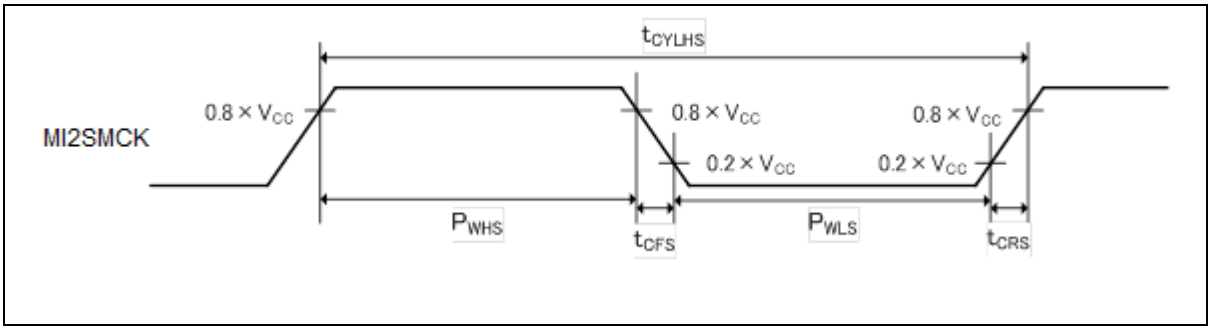


Slave mode

MI2SMCK Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	MI2SMCK	-	-	12.288	MHz	
Input clock cycle	t_{CYLHS}	-	-	81.3	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



MI2SMCK Output Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	MI2SMCK	-	-	25	MHz	$V_{CC} \geq 2.7$ V
				-	20	MHz	$V_{CC} < 2.7$ V

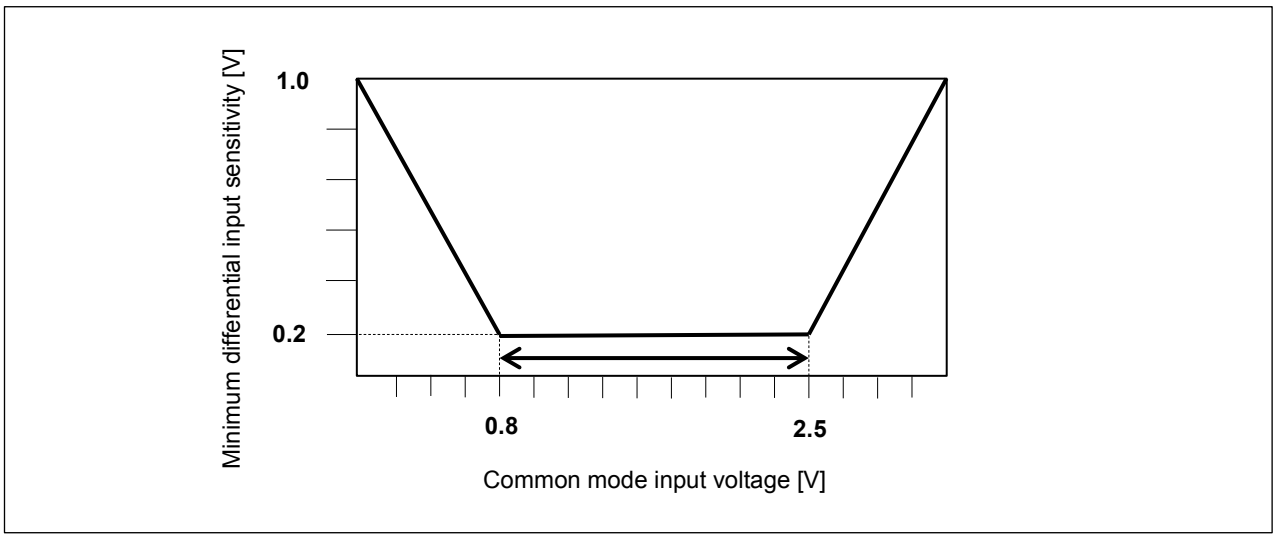
11.6 USB Characteristics

(V_{CC}=3.0 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} – 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Differential common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristic	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-speed	4	20	ns	*5
	Falling time	t_{FF}		Full-speed	4	20	ns	*5
	Rising/Falling time matching	t_{FRFM}		Full-speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-speed	75	300	ns	*7
	Falling time	t_{LF}		Low-speed	75	300	ns	*7
	Rising/Falling time matching	t_{LRFM}		Low-speed	80	125	%	*7

*1 : The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V_{IL}(Max)=0.8 V, VIH(Min)=2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2 : Use differential-receiver to receive USB differential data signal.
Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.



*3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above

11.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

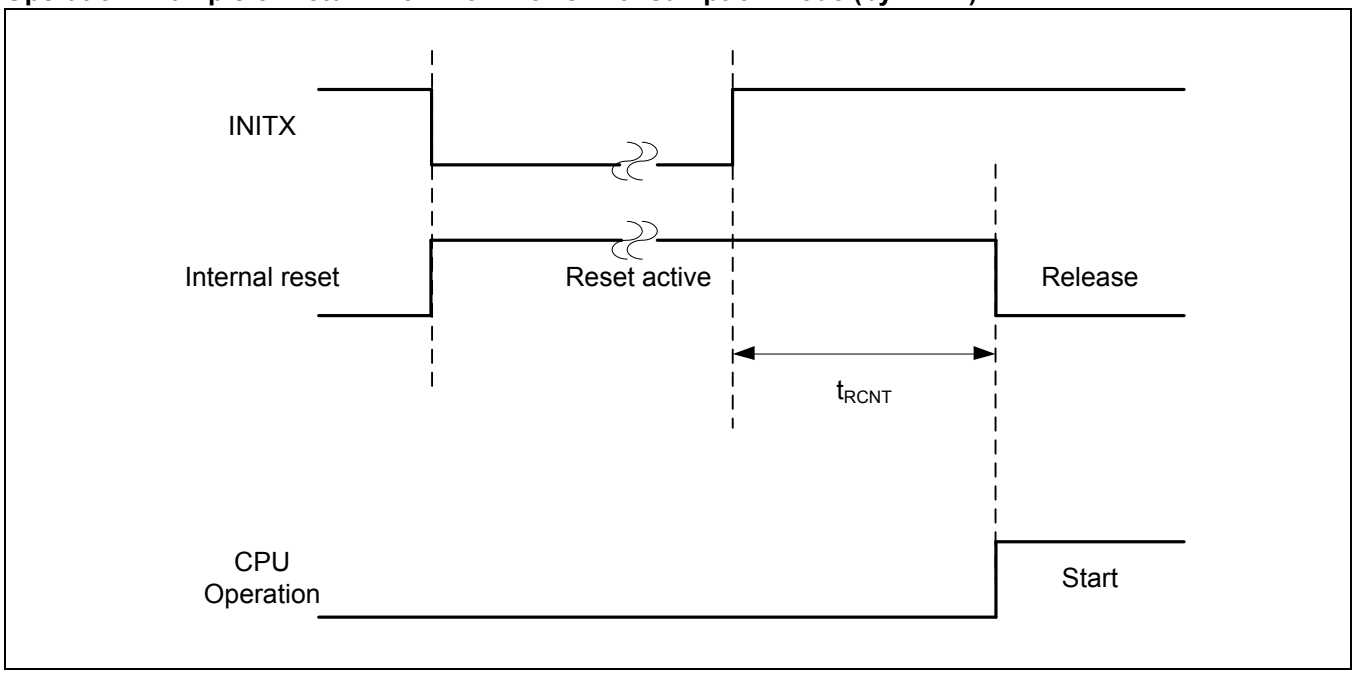
Return Count Time

(V_{CC}=1.65 V to 3.6 V, T_A=-40°C to +105°C)

Parameter		Symbol	Value		Unit	Remarks
Current Mode	Mode to return		Typ	Max*		
High-speed CR Sleep mode Main Sleep mode PLL Sleep mode	High-speed CR Run mode	t_{RCNT}	20	22	µs	When High-speed CR is enabled
Low-speed CR Sleep mode			50	106	µs	When High-speed CR is enabled
Sub Sleep mode			112	137	µs	When High-speed CR is enabled
High-speed CR Timer mode Main Timer mode PLL Timer mode			20	22	µs	When High-speed CR is enabled
Low-speed CR Timer mode			87	159	µs	
Sub Timer mode			148	209	µs	
Stop mode RTC mode			45	68	µs	
Deep Standby RTC mode Deep Standby Stop mode			43	281	µs	

*: The maximum value depends on the accuracy of built-in CR.

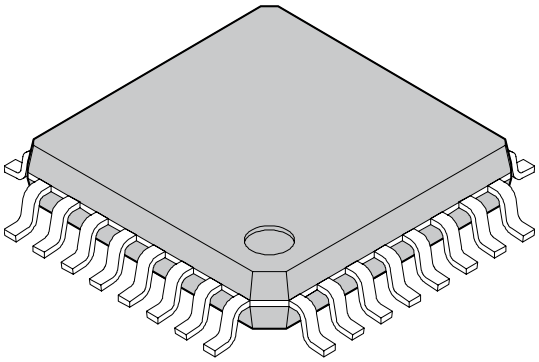
Operation Example of Return from Low-Power Consumption Mode (by INITX)



12. Ordering Information

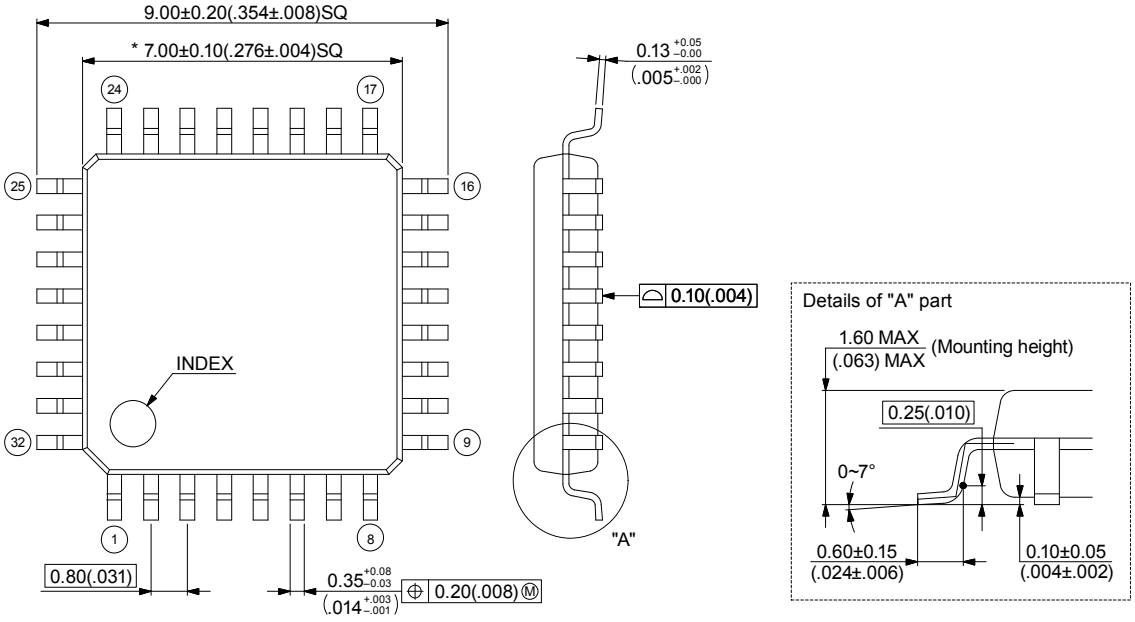
Part number	On-chip Flash memory [Kbyte]	On-Chip SRAM [Kbyte]	Package	Packing
S6E1C32D0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 64 pins (FPT-64P-M38)	Tray
S6E1C31D0AGV20000	64	12		
S6E1C32C0AGV20000	128	16	Plastic • LQFP (0.50 mm pitch), 48 pins (FPT-48P-M49)	Tray
S6E1C31C0AGV20000	64	12		
S6E1C32B0AGP20000	128	16	Plastic • LQFP (0.80 mm pitch), 32 pins (FPT-32P-M30)	Tray
S6E1C31B0AGP20000	64	12		
S6E1C32D0AGN20000	128	16	Plastic • QFN64 (0.50 mm pitch), 64 pins (LCC-64P-M25)	Tray
S6E1C31D0AGN20000	64	12		
S6E1C32C0AGN20000	128	16	Plastic • QFN48 (0.50 mm pitch), 48 pins (LCC-48P-M74)	Tray
S6E1C31C0AGN20000	64	12		
S6E1C32B0AGN20000	128	16	Plastic • QFN32 (0.50 mm pitch), 32 pins (LCC-32P-M73)	Tray
S6E1C31B0AGN20000	64	12		
(TBD)	128	16	WLCSP (TBD)	(TBD)

13. Package Dimensions

32-pin plastic LQFP		
	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX
(FPT-32P-M30)		

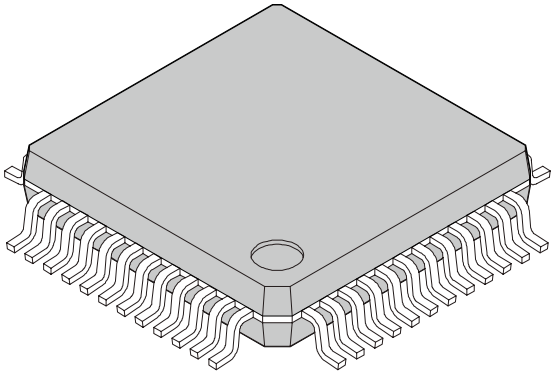
32-pin plastic LQFP
(FPT-32P-M30)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

48-pin plastic LQFP

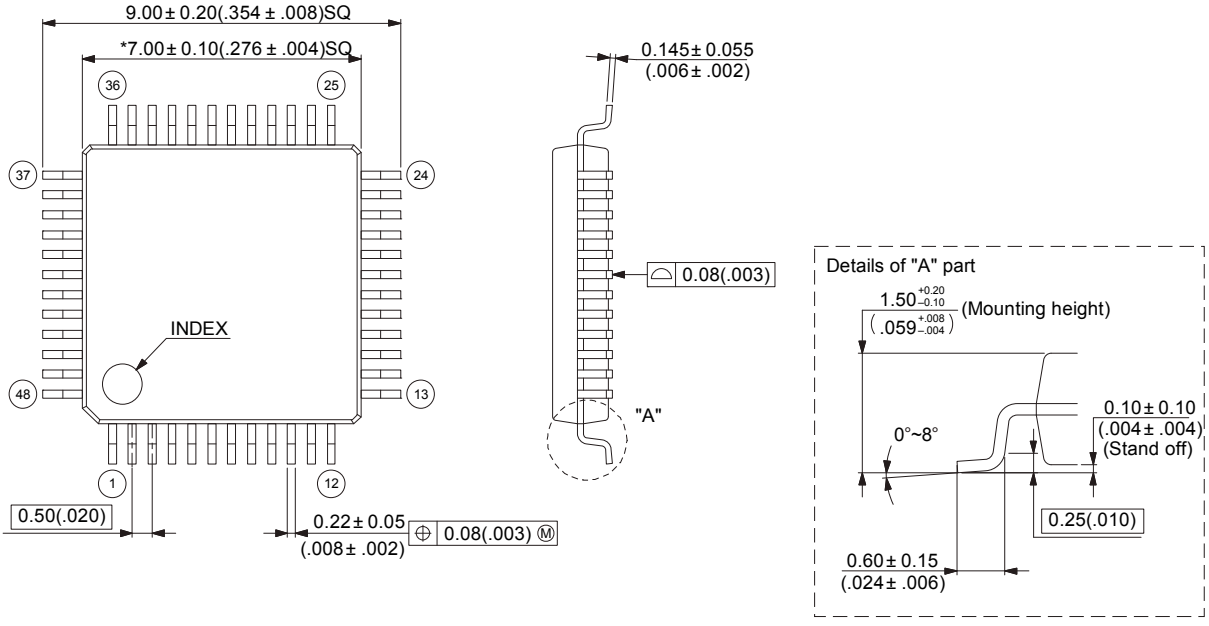


(FPT-48P-M49)

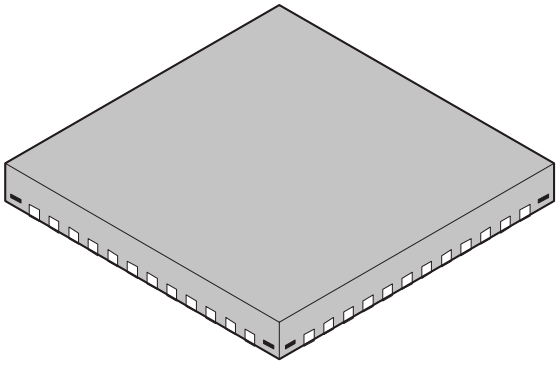
Lead pitch	0.50 mm
Package width × package length	7.00 mm × 7.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

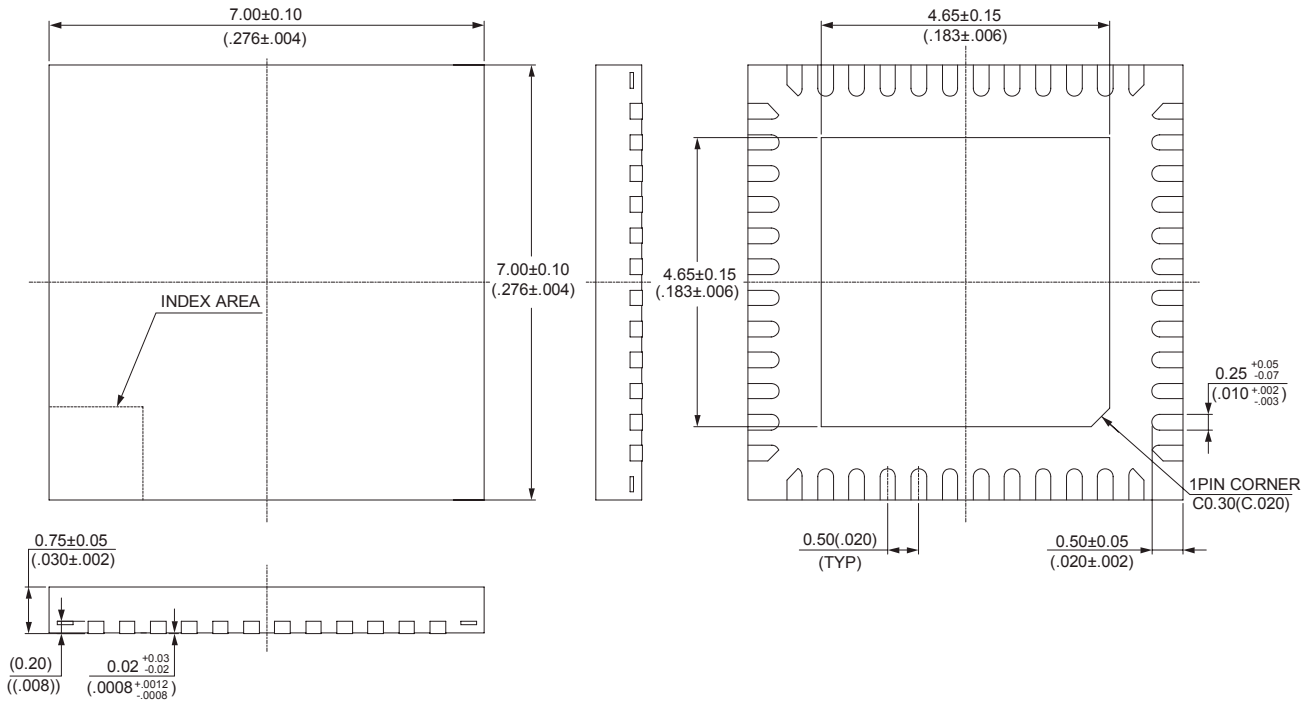
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



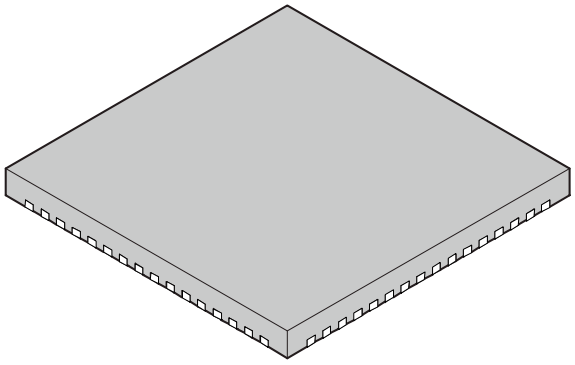
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

48-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width× package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.12 g
(LCC-48P-M74)		

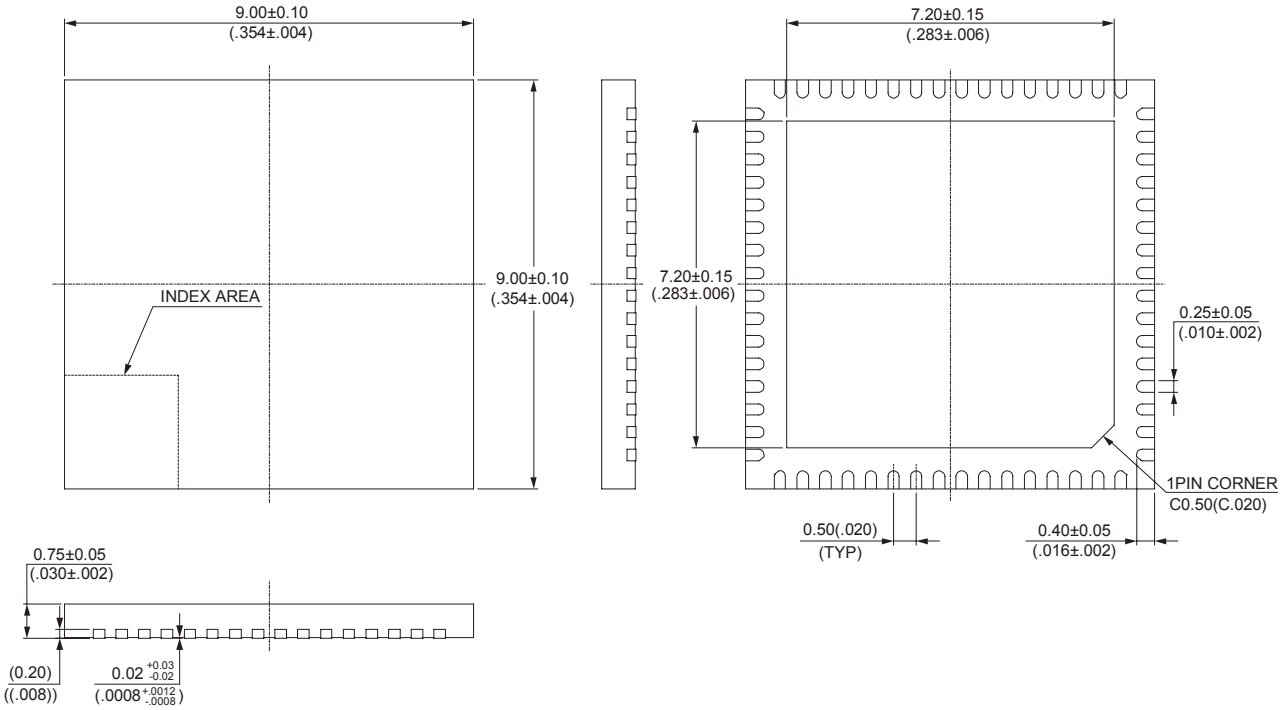
48-pin plastic QFN
(LCC-48P-M74)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.21 g
(LCC-64P-M25)		

64-pin plastic QFN
(LCC-64P-M25)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.