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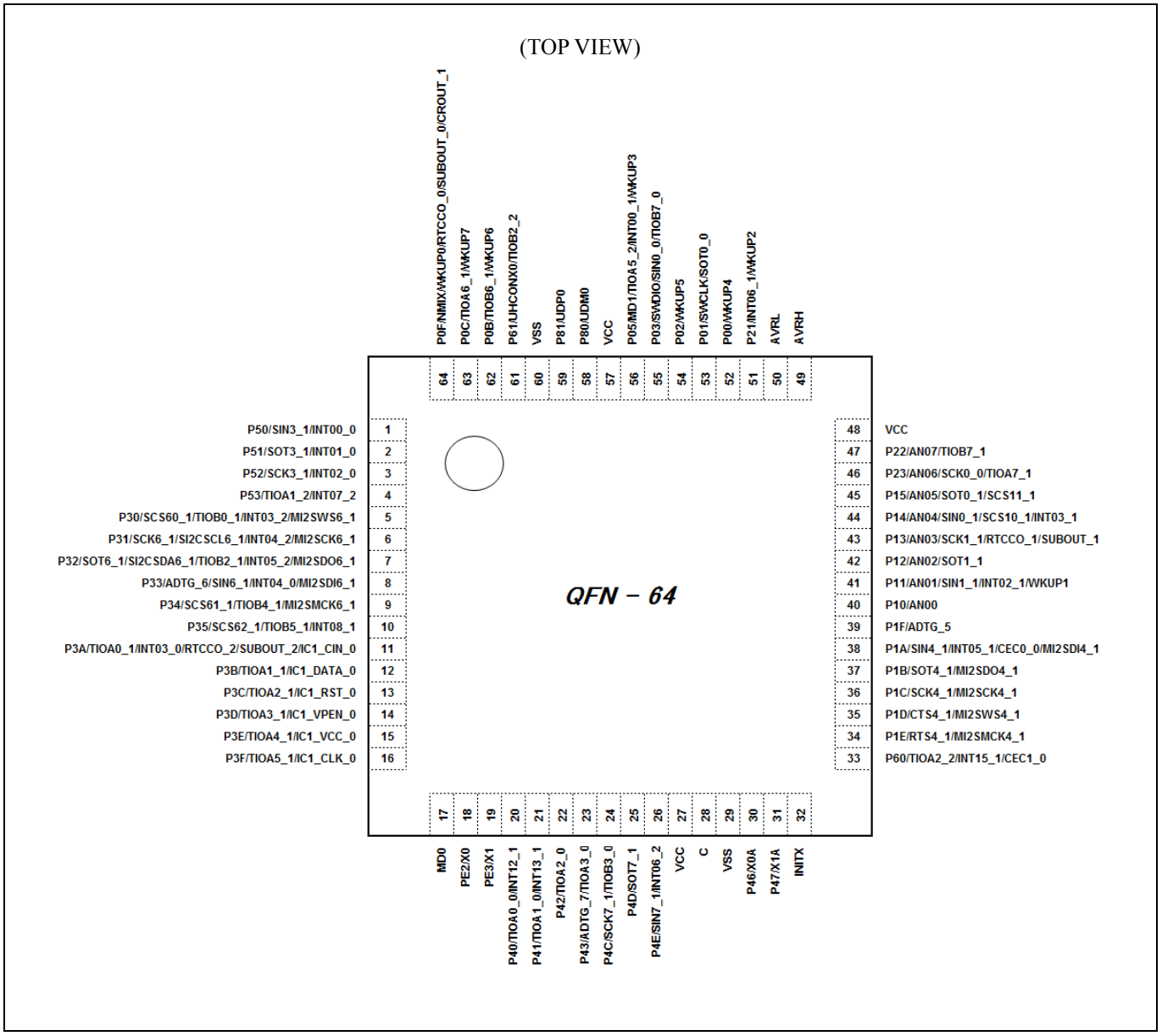
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CSIO, I²C, LINbus, SmartCard, UART/USART, USB
Peripherals	I²S, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e1c32d0agv20000

LCC-64P-M25



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
ADC	ADTG_5	A/D converter external trigger input pin	39	-	-	-
	ADTG_6		8	8	7	-
	ADTG_7		23	-	-	-
ADC	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	40	28	18	-
	AN01		41	29	19	-
	AN02		42	30	20	-
	AN03		43	31	21	-
	AN04		44	32	-	-
	AN05		45	33	-	-
	AN06		46	34	22	-
	AN07		47	35	23	-
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	20	-	-	-
	TIOA0_1		11	10	-	-
	TIOB0_1	Base timer ch.0 TIOB pin	5	5	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	21	-	-	-
	TIOA1_1		12	11	-	-
	TIOA1_2		4	4	-	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	22	-	-	-
	TIOA2_1		13	12	-	-
	TIOA2_2		33	25	17	-
	TIOB2_1	Base timer ch.2 TIOB pin	7	7	6	-
	TIOB2_2		61	47	-	-
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	23	-	-	-
	TIOA3_1		14	-	-	-
	TIOB3_0	Base timer ch.3 TIOB pin	24	-	-	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	15	-	-	-
	TIOB4_1	Base timer ch.4 TIOB pin	9	-	-	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	16	-	-	-
	TIOA5_2		56	42	29	-
	TIOB5_1	Base timer ch.5 TIOB pin	10	-	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	63	-	-	-
	TIOB6_1	Base timer ch.6 TIOB pin	62	-	-	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	34	22	-
	TIOB7_0	Base timer ch.7 TIOB pin	55	41	28	-
	TIOB7_1		47	35	23	-
Debugger	SWCLK	Serial wire debug interface clock input pin	53	40	27	-
	SWDIO	Serial wire debug interface data input / output pin	55	41	28	-

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
External Interrupt	INT00_0	External interrupt request 00 input pin	1	1	2	-
	INT00_1		56	42	29	-
	INT01_0	External interrupt request 01 input pin	2	2	3	-
	INT02_0	External interrupt request 02 input pin	3	3	4	-
	INT02_1		41	29	19	-
	INT03_0	External interrupt request 03 input pin	11	10	-	-
	INT03_1		44	32	-	-
	INT03_2		5	5	-	-
	INT04_0	External interrupt request 04 input pin	8	8	7	-
	INT04_2		6	6	5	-
	INT05_1	External interrupt request 05 input pin	38	27	-	-
	INT05_2		7	7	6	-
	INT06_1	External interrupt request 06 input pin	51	39	26	-
	INT06_2		26	18	-	-
	INT07_2	External interrupt request 07 input pin	4	4	-	-
	INT08_1	External interrupt request 08 input pin	10	-	-	-
	INT12_1	External interrupt request 12 input pin	20	-	-	-
	INT13_1	External interrupt request 13 input pin	21	-	-	-
	INT15_1	External interrupt request 15 input pin	33	25	17	-
	NMIX	Non-Maskable Interrupt input pin	64	48	1	-
GPIO	P00	General-purpose I/O port 0	52	-	-	-
	P01		53	40	27	-
	P02		54	-	-	-
	P03		55	41	28	-
	P05		56	42	29	-
	P0B		62	-	-	-
	P0C		63	-	-	-
	P0F		64	48	1	-
GPIO	P10	General-purpose I/O port 1	40	28	18	-
	P11		41	29	19	-
	P12		42	30	20	-
	P13		43	31	21	-
	P14		44	32	-	-
	P15		45	33	-	-
	P1A		38	27	-	-
	P1B		37	26	-	-
	P1C		36	-	-	-
	P1D		35	-	-	-
	P1E		34	-	-	-
	P1F		39	-	-	-
GPIO	P21	General-purpose I/O port 2	51	39	26	-
	P22		47	35	23	-
	P23		46	34	22	-

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	41	29	19	-
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I2C pin (operation mode 4).	42	30	20	-
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I2C pin (operation mode 4).	43	31	21	-
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 input/output pin.	44	32	-	-
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	45	33	-	-
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	1	1	2	-
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I2C pin (operation mode 4).	2	2	3	-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I2C pin (operation mode 4).	3	3	4	-
Multi-function Serial 4	SIN4_1	Multi-function serial interface ch.4 input pin	38	27	-	-
	SOT4_1 (SDA4_1)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I2C pin (operation mode 4).	37	26	-	-
	SCK4_1 (SCL4_1)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I2C pin (operation mode 4).	36	-	-	-
	CTS4_1	Multi-function serial interface ch4 CTS input pin	35	-	-	-
	RTS4_1	Multi-function serial interface ch4 RTS output pin	34	-	-	-

Pin function	Pin name	Function description	Pin no.			
			LQFP-64 QFN-64	LQFP-48 QFN-48	LQFP-32 QFN-32	WLCSP (TBD)
Low Power Consumption Mode	WKUP0	Deep Standby mode return signal input pin 0	64	48	1	-
	WKUP1	Deep Standby mode return signal input pin 1	41	29	19	-
	WKUP2	Deep Standby mode return signal input pin 2	51	39	26	-
	WKUP3	Deep Standby mode return signal input pin 3	56	42	29	-
	WKUP4	Deep Standby mode return signal input pin 4	52	-	-	-
	WKUP5	Deep Standby mode return signal input pin 5	54	-	-	-
	WKUP6	Deep Standby mode return signal input pin 6	62	-	-	-
	WKUP7	Deep Standby mode return signal input pin 7	63	-	-	-
I2C Slave	SI2CSCL6_1	I2C Clock Pin	6	6	5	-
	SI2CSDA6_1	I2C Data Pin	7	7	6	-
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	32	24	16	-
MODE	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	17	13	8	-
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	42	29	-
CLOCK	X0	Main clock (oscillation) input pin	18	14	9	-
	X0A	Sub clock (oscillation) input pin	30	22	14	-
	X1	Main clock (oscillation) I/O pin	19	15	10	-
	X1A	Sub clock (oscillation) I/O pin	31	23	15	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	64	48	1	-
POWER	VCC	Power supply pin	27	19	11	-
	VCC		48	36	24	-
	VCC		57	43	-	-
GND	VSS	GND pin	29	21	13	-
	VSS		60	46	32	-
Analog Reference	AVRH *	A/D converter analog reference voltage input pin	49	37	-	-
	AVRL	A/D converter analog reference voltage input pin	50	38	25	-
C pin	C	Power supply stabilization capacitance pin	28	20	12	-

*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

11.4 AC Characteristics

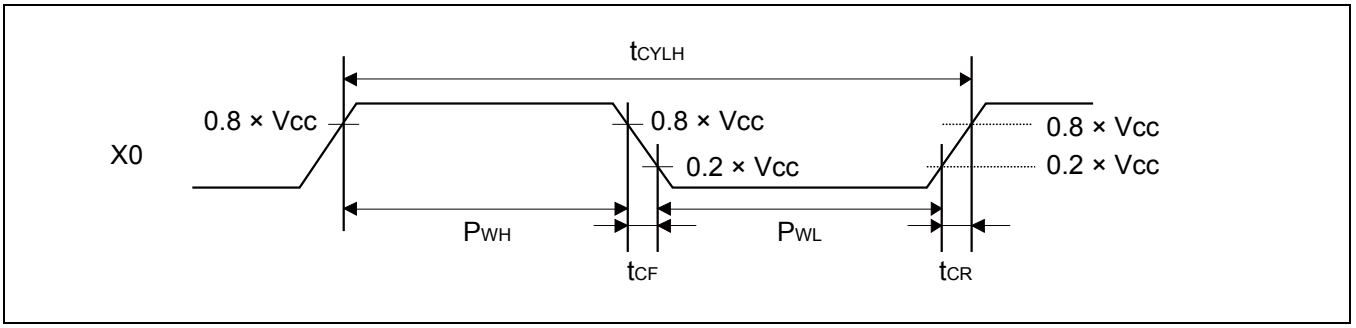
11.4.1 Main Clock Input Characteristics

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	$V_{CC} \geq 2.7V$	8	48	MHz	When the crystal oscillator is connected
			$V_{CC} < 2.7V$	8	20		
			-	8	48	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	20.83	125	ns	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock*1 frequency	F_{CM}	-	-	-	40.8	MHz	Master clock
	F_{CC}	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40.8	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40.8	MHz	APB1 bus clock*2
Internal operating clock*1 cycle time	t_{CYCCM}	-	-	24.5	-	ns	Master clock
	t_{CYCC}	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	24.5	-	ns	APB1 bus clock*2

*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".



11.4.3 Built-in CR Oscillation Characteristics

Built-in High-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS} = 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = - 40°C to + 105°C,	7.84	8	8.16	MHz	After trimming *1
Frequency stabilization time	t_{CRWT}	-	-	-	300	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in Low-Speed CR

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

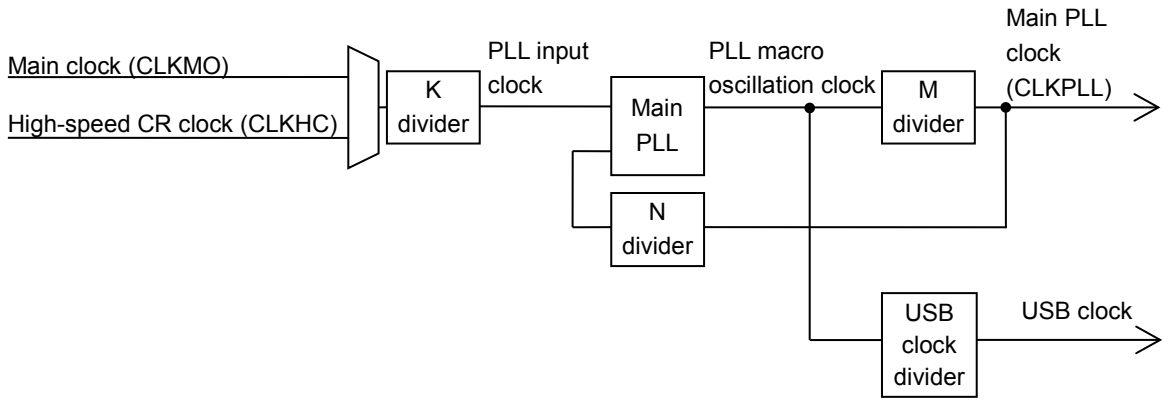
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	8	-	16	MHz	
PLL multiple rate	-	5	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	
USB clock frequency*3	$F_{CLKSPLL}$	-	-	48	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

*3: For more information about USB clock, see "Chapter: USB Clock Generation" in "FM0+ Family Peripheral Manual Communication Macro Part".

Main PLL connection



11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	50	-	-	µs	
PLL input clock frequency	F_{PLLI}	7.84	8	8.16	MHz	
PLL multiple rate	-	9	-	18	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40.8	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

Note:

- *For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency and temperature have been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.*

11.4.6 Reset Input Characteristics

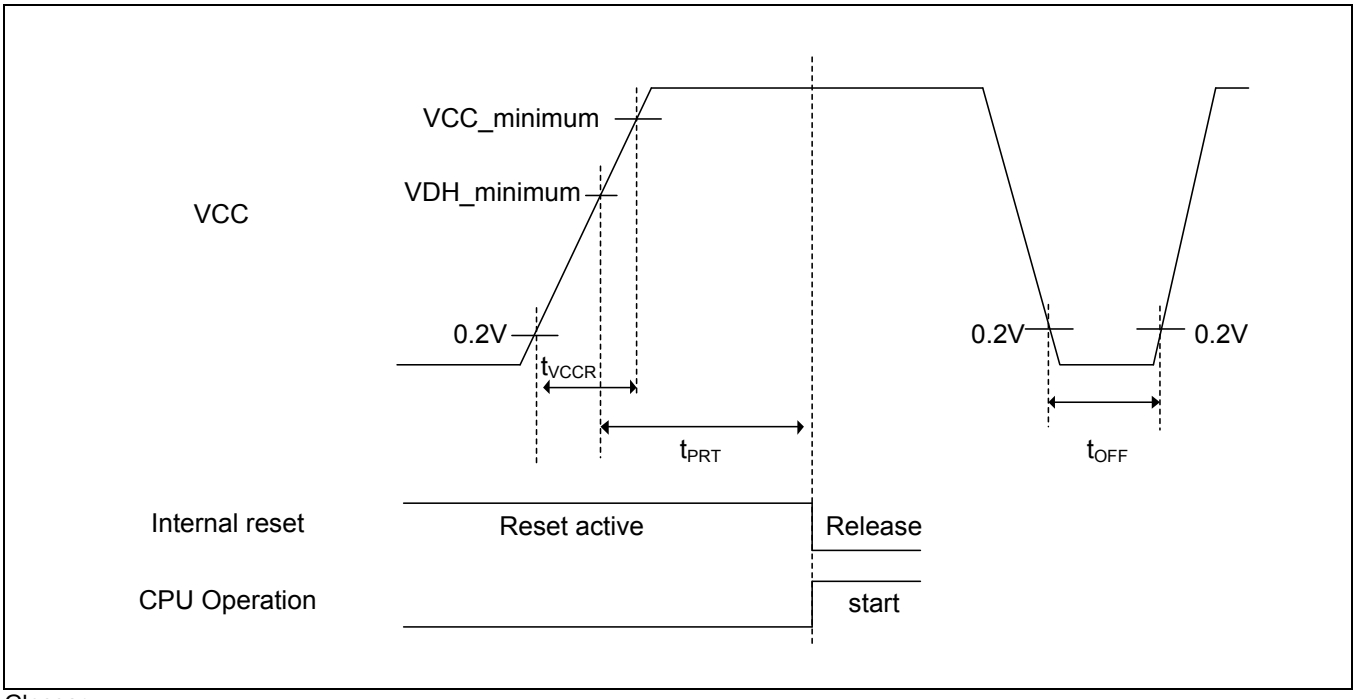
(V_{CC} = 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

11.4.7 Power-on Reset Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

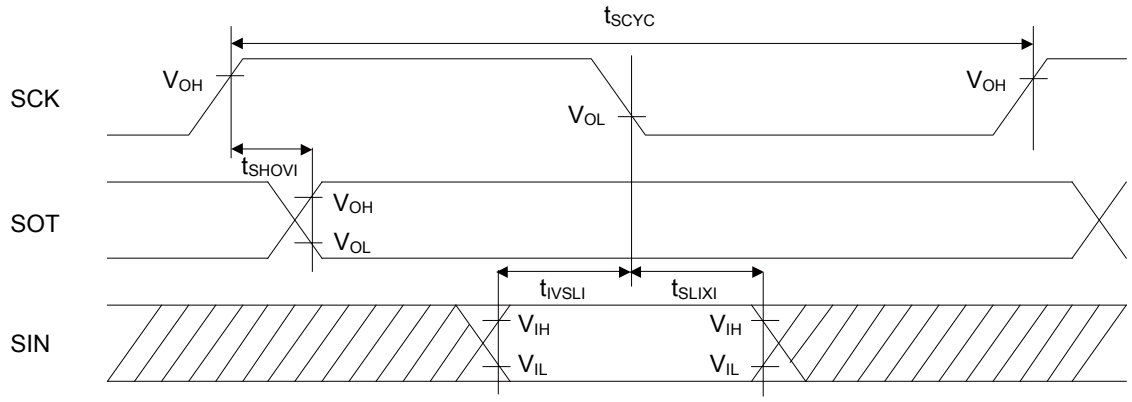
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		0.43	3.4	ms	



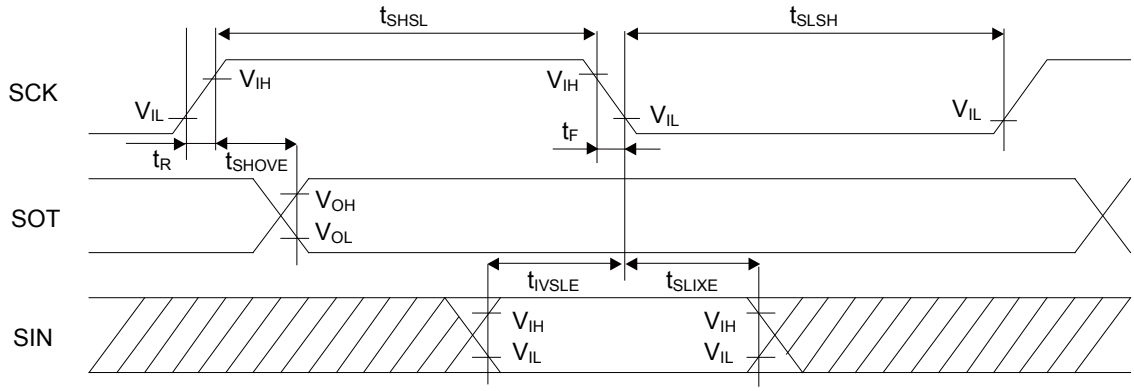
Glossary

- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum detection voltage of Low-Voltage detection reset.

See "11.7 Low-Voltage Detection Characteristics".



Master mode



Slave mode

SPI (SPI=1, SCINV=0)

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	Slave mode	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for clock synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCKx_0 and SOTx_1.
- *External load capacitance C_L=30 pF*

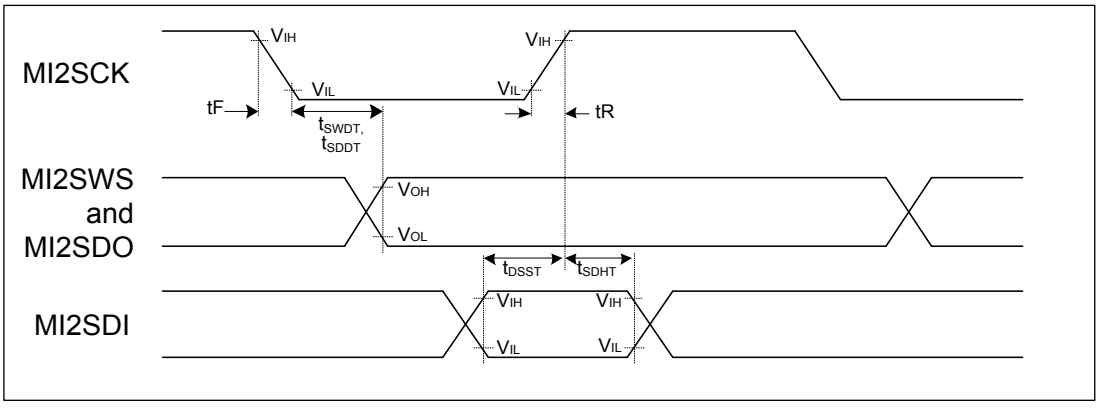
11.4.12 I^2S Timing (MFS-I2S Timing)

Master Mode Timing

(V_{CC}= 1.65 V to 3.6 V, V_{SS}= 0 V, T_A=- 40°C to +105°C)

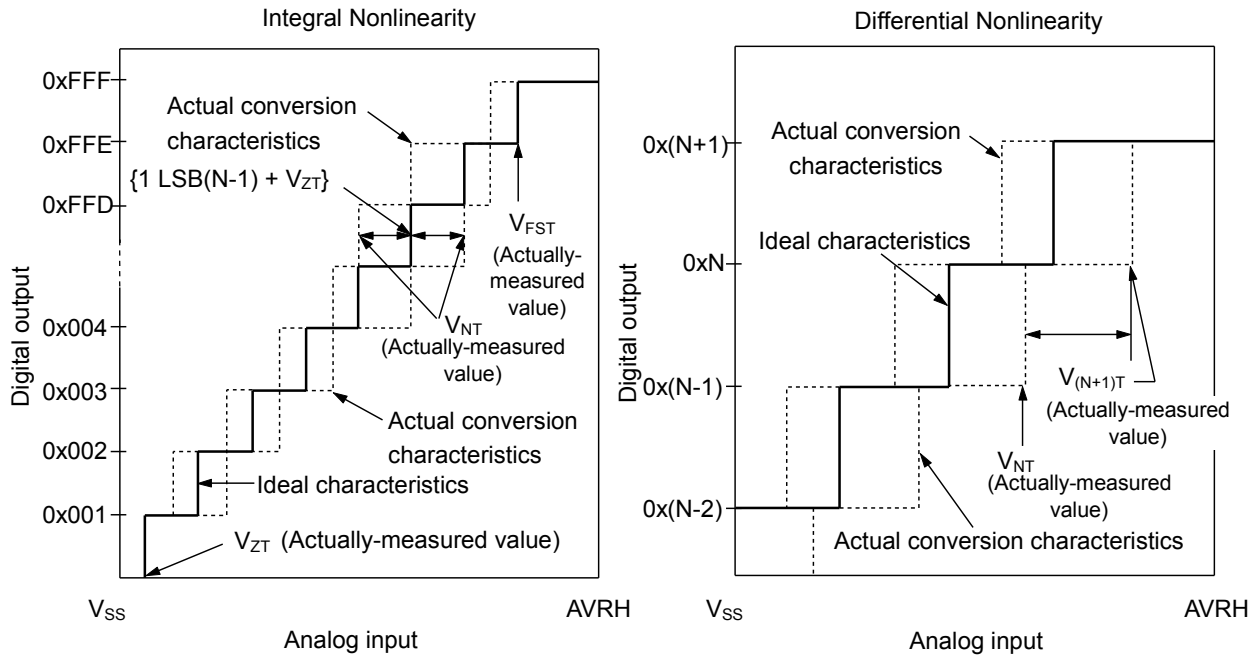
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 2.7 V		V_{CC} ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency (*1)	F_{MI2SCK}	MI2SCKx	C_L=30 pF	-	6.144	-	6.144	MHz
I^2S clock cycle time (*1)	t_{ICYC}	MI2SCKx		4 t_{CYCP}	-	4 t_{CYCP}	-	ns
I^2S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t_{SWDT}	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t_{SDDT}	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t_{DSST}	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t_{SDHT}	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	tF	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	tR	MI2SCKx		-	5	-	5	ns

*1: I^2S clock should meet the multiple of PCLK(t_{ICYC}) and the frequency less than F_{MI2SCK} meantime. The detail information please refer to Chapter I^2S of Communication Macro Part of Peripheral Manual.



Definitions of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

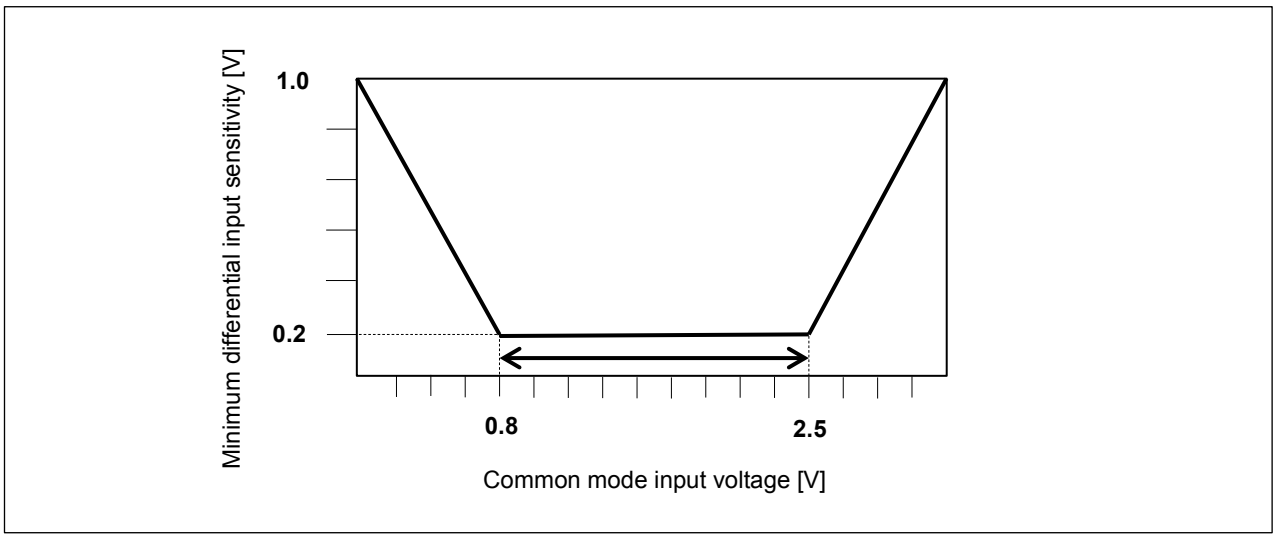
11.6 USB Characteristics

(V_{CC}=3.0 V to 3.6 V, V_{SS}=0 V, T_A=- 40°C to +105°C)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} – 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Differential common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristic	Output H level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-speed	4	20	ns	*5
	Falling time	t_{FF}		Full-speed	4	20	ns	*5
	Rising/Falling time matching	t_{FRFM}		Full-speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-speed	75	300	ns	*7
	Falling time	t_{LF}		Low-speed	75	300	ns	*7
	Rising/Falling time matching	t_{LRFM}		Low-speed	80	125	%	*7

*1 : The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V_{IL}(Max)=0.8 V, VIH(Min)=2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

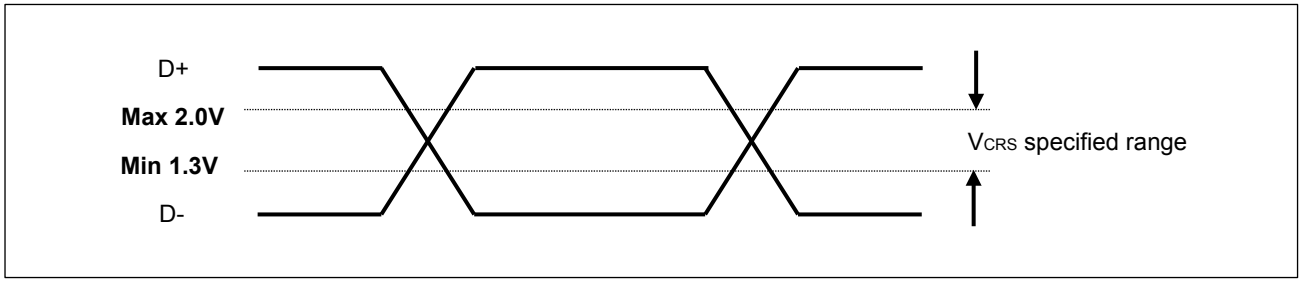
*2 : Use differential-receiver to receive USB differential data signal.
Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.



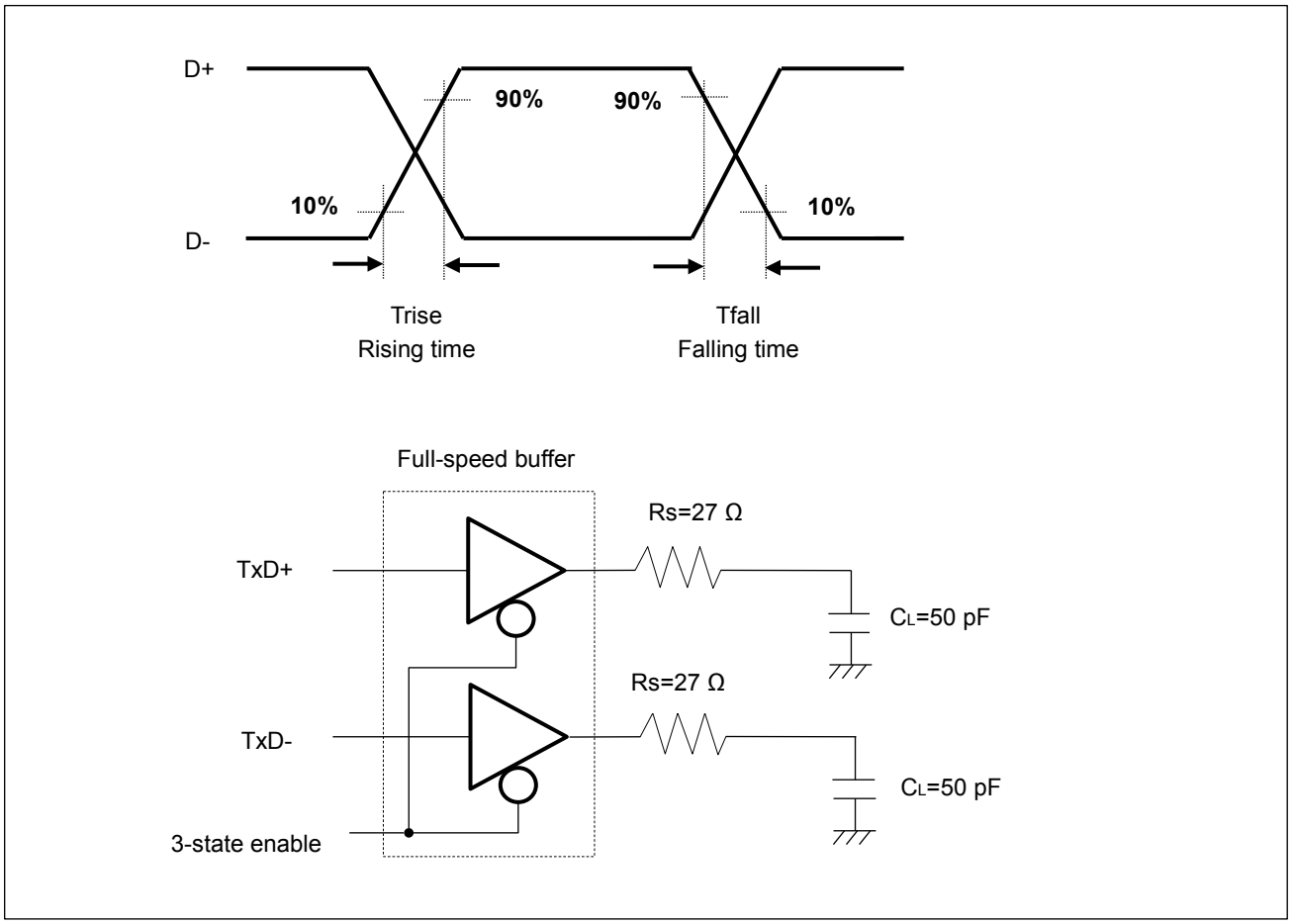
*3 : The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above

(to the VSS and 1.5 kΩ load) at high-state (V_{OH})

*4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.

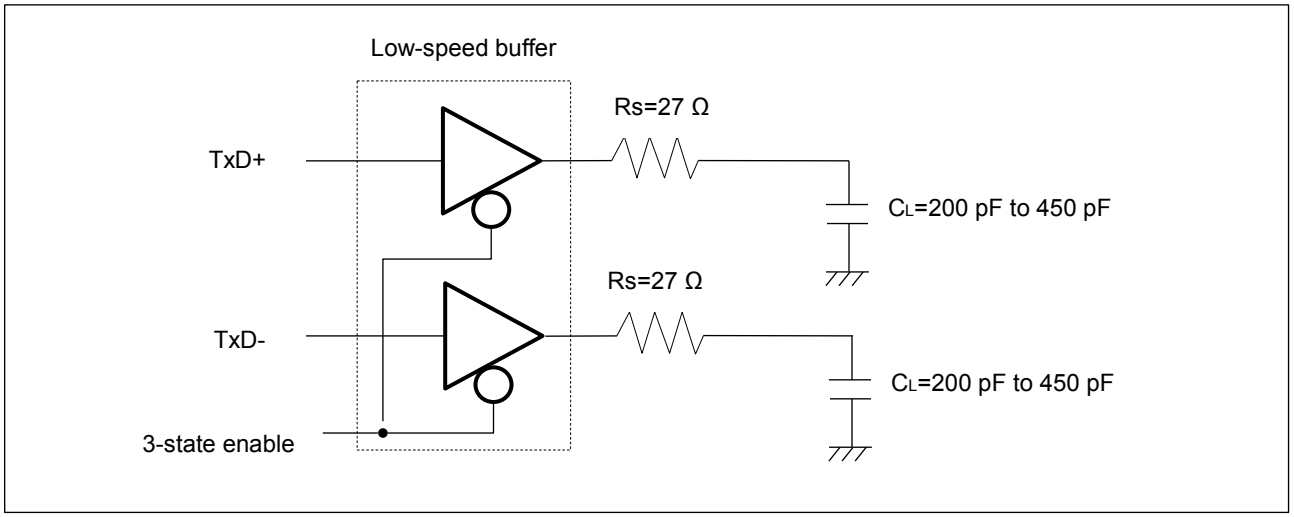


*5 : The indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ±10% to minimize RFI emission.



*6 : USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28Ω to 44Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 33 Ω (recommendation value : 27 Ω) series resistor Rs.

- Low-Speed Load (Compliance Load)



11.8 Flash Memory Write/Erase Characteristics

(V_{CC}=1.65 V to 3.6 V, T_A=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	4.5	11.7	s	The chip erase time includes the time of writing prior to internal erase.

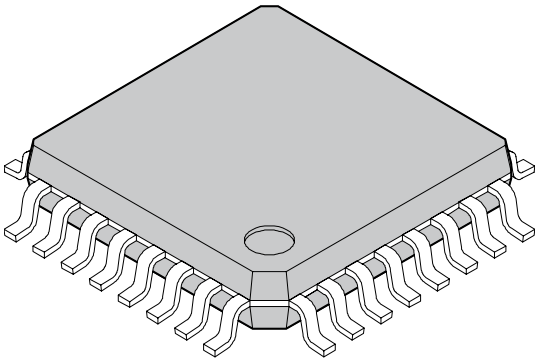
*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

Write/Erase Cycle and Data Hold Time

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

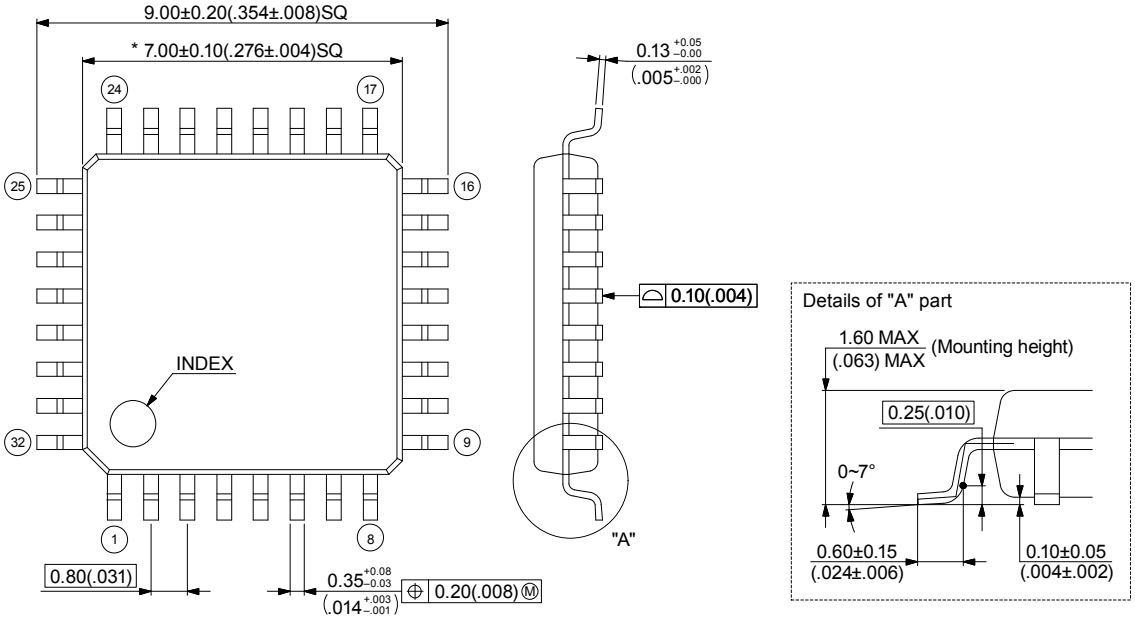
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C).

13. Package Dimensions

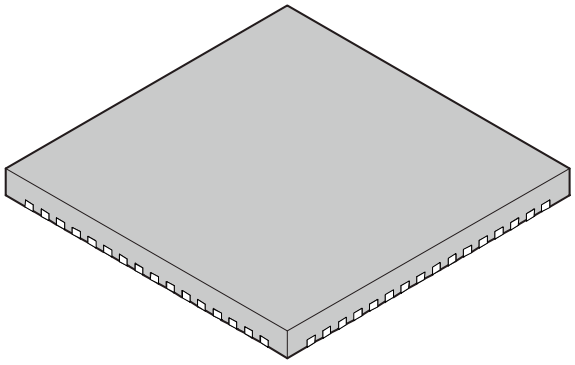
32-pin plastic LQFP		
	Lead pitch	0.80 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm MAX
(FPT-32P-M30)		

32-pin plastic LQFP
(FPT-32P-M30)

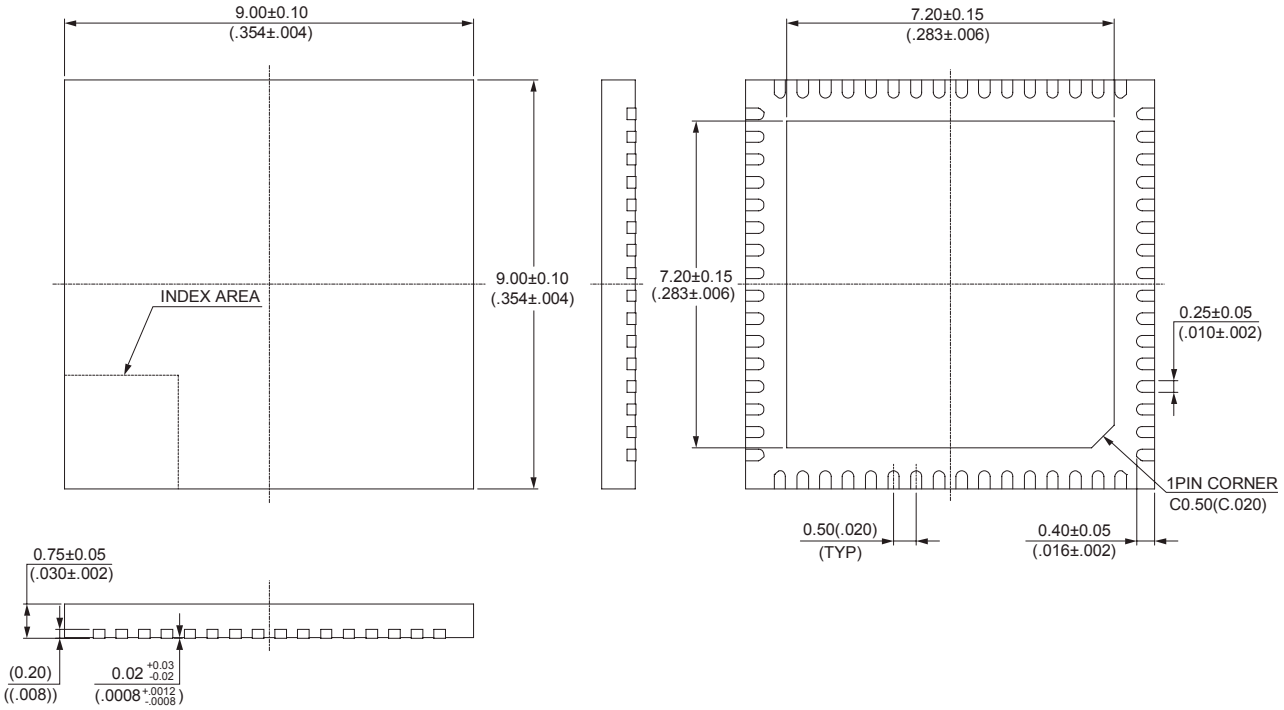
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.21 g
(LCC-64P-M25)		

64-pin plastic QFN
(LCC-64P-M25)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.