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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	57
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=scf5250ag120

1.2.2 DMA Controller

The SCF5250 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

1.2.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

1.2.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5250 processor uses a 8K-byte, direct-mapped instruction cache to achieve 107 MIPS at 120 MHz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

1.2.5 Internal 128-KByte SRAM

The 128-KByte on-chip SRAM is available in two banks, SRAM0 (64K) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in SRAM1 can be accessed under DMA.

1.2.6 SDRAM Controller

The SCF5250 SDRAM controller provides a glueless interface for one bank of SDRAM up to 32 MB (256 Mbits). The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

The CD-ROM decoder performs following functions in hardware:

- Sector sync recognition
- Descrambling of sectors
- Verification of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors
- Third-layer error correction is not performed

The CD-ROM encoder performs following functions in hardware:

- Sector sync recognition
- Scrambling of sectors
- Insertion of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors.
- Third-layer error encoding needs to be done in software. This can use approximately 5–10 MHz of performance for single-speed.

1.2.13 Dual UART Module

Two full-duplex UARTs with independent receive and transmit buffers are in this module. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The Dual UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function from a programmable prescaler. You can select full duplex, auto-echo loopback, local loopback, and remote loopback modes. The programmable Dual UARTs can interrupt the CPU on various normal or error-condition events.

1.2.14 Queued Serial Peripheral Interface QSPI

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfers of up to 15 Mbits/second are possible at a CPU clock of 120 MHz. The QSPI supports master mode operation only.

1.2.15 Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer. Timer0 has an external pin TOUT0, which can be used in Output Compare mode. This mode triggers an external signal or interrupts the CPU when the timer reaches a set value, and can also generate waveforms on TOUT0.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the ÷1 and ÷16 clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

1.2.16 IDE and SmartMedia Interfaces

The SCF5250 system bus allows connection of an IDE hard disk drive or SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5250.

Low cost version SCF5250LPV100 and SCF5250LAG100 does not run production test for the IDE/CF/SD/MMC interfaces. Freescale does not guarantee these interfaces will work on these two devices.

1.2.17 Analog/Digital Converter (ADC)

The six channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. Both the analogue comparator and digital sections of the ADC are provided internally. An external integrator circuit (resistor/capacitor) is required, which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

1.2.18 I^2C Module

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

1.2.19 Chip-Selects

Up to four programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

1.2.20 GPIO Interface

A total of 60 General Purpose inputs and 57 General Purpose outputs are available. These are multiplexed with various other signals. Seven of the GPIO inputs have edge sensitive interrupt capability.

1.2.21 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 7 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

Table 2. SCF5250 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[24:1] A[23]/GPO54	24 address lines, address line 23 multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only).	Out	X
Read-write control	R/$\overline{W}$	Bus write enable - indicates if read or write cycle in progress	Out	H
Output enable	OE	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	$\overline{SDRAS}$/GPIO59	Row address strobe for external SDRAM.	Out	negated
Synchronous column address strobe	$\overline{SDCAS}$/GPIO39	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	$\overline{SDWE}$/GPIO38	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	$\overline{SDUDQM}$/GPO53	Indicates during write cycle if high byte is written	Out	–
SDRAM lower byte enable	$\overline{SDLDQM}$/GPO52	Indicates during write cycle if low byte is written	Out	–
SDRAM chip selects	$\overline{SD\_CS0}$/GPIO60	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE/GPIO63	SDRAM clock enable	Out	–
System clock	BCLK/GPIO40	SDRAM clock output	In/Out	–
ISA bus read strobe	$\overline{IDE\text{-}DIOR}$/GPIO31 (CS2)	There is 1 ISA bus read strobe and 1 ISA bus write strobe. They allow connection of one independent ISA bus peripherals, e.g. an IDE slave device.	In/Out	–
ISA bus write strobe	$\overline{IDE\text{-}DIOW}$/GPIO32 (CS2)		In/Out	–
ISA bus wait signal	$\overline{IDE\text{-}IORDY}$/GPIO33	ISA bus wait line - available for both busses	In/Out	–
Chip Selects[2:0]	$\overline{CS0}$/$\overline{CS4}$ $\overline{CS1}$/QSPI_CS3/GPIO28	Enables peripherals at programmed addresses. $\overline{CS}$[0] provides boot ROM selection	Out In/Out	negated
Buffer enable 1	$\overline{BUFENB1}$/GPIO29	Two programmable buffer enables allow seamless steering of external buffers to split data and address bus in sections.	In/Out	–
Buffer enable 2	$\overline{BUFENB2}$/GPIO30		In/Out	–
Transfer acknowledge	$\overline{TA}$/GPIO12	Transfer Acknowledge signal	In/Out	–
Wake Up	$\overline{WAKE\_UP}$/GPIO21	Wake-up signal input	In	–
Serial Clock Line	SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10	Clock signal for Dual I^2C module operation	In/Out	–
Serial Data Line	SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44	Serial data port for second I^2C module operation	In/Out	–
Receive Data	SDA1/RXD1/GPIO44 RXD0/GPIO46	Signal is receive serial data input for DUART	In	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45	Signal is transmit serial data output for DUART	Out	–
Request-To-Send	DDATA3/$\overline{\text{RTS0}}$/GPIO4 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	DUART signals a ready to receive data query	Out	–
Clear-To-Send	DDATA2/$\overline{\text{CTSO}}$/GPIO3 DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Signals to DUART that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capable of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLK_OUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPI_CS0/EBUIN4/GPIO15	audio interfaces IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPI_CS1/EBUOUT2/GPIO16	audio interfaces IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	audio interfaces serial data inputs	In	–
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	audio interfaces serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/GPIO43/AUDIO_CLOCK	audio interfaces serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	audio interfaces serial bit clocks	In/Out	–
Serial input	EF/GPIO6	error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPI_DIN/QSPI_DOUT/ GPIO26	audio interfaces subcode clock	In/Out	–
Subcode sync	QSPI_DOUT/SFSY/GPIO27	audio interfaces subcode sync	In/Out	–
Subcode data	QSPI_CLK/SUBR/GPIO25	audio interfaces subcode data	In/Out	–
Clock frequency trim	XTRIM/GPIO0	clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPI_CS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/GPIO43/AUDIO_CLOCK	Optional Audio clock Input	–	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Processor Status	PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47	Indicates internal processor status.	In/Out	Hi-Z
Processor Clock	PSTCLK/GPIO51	processor clock output	Out	–
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG.	In	–
Test Reset/Development Serial Clock	$\overline{\text{TRST}}$/DSCLK	Multiplexed signal that is asynchronous reset for JTAG controller. Clock input for debug module.	In	–
Test Mode Select/ Break Point	TMS/$\overline{\text{BKPT}}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode.	In	–
Test Data Input / Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	–
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module.	Out	–

3.1 GPIO

Many pins have an optional GPIO function.

- General purpose input is always active, regardless of state of pin.
- General purpose output or primary output is determined by the appropriate setting of the Pin Multiplex Control Registers, GPIO-FUNCTION, GPIO1-FUNCTION and PIN-CONFIG.
- At Power-on reset, all pins are set to their primary function.

3.2 SCF5250 Bus Signals

These signals provide the external bus interface to the SCF5250 processor.

3.2.1 Address Bus

- The address bus provides the address of the byte or most significant byte of the word or longword being transferred. The address lines also serve as the DRAM address pins, providing multiplexed row and column address signals.
- Bits 23 down to 1 and 24 of the address are available. A24 is intended to be used with 256 Mbit DRAM's. Signals are named:
  - A[23:1]
  - A20/24

3.2.2 Read-Write Control

This signal indicates during any bus cycle whether a read or write is in progress. A low is write cycle and a high is a read cycle.

3.2.3 Output Enable

The $\overline{OE}$ signal is intended to be connected to the output enable of asynchronous memories connected to chip selects. During bus read cycles, the ColdFire processor will drive $\overline{OE}$ low.

3.2.4 Data Bus

The data bus (D[31:16]) is bi-directional and non-multiplexed. Data is registered by the SCF5250 on the rising clock edge. The data bus uses a default configuration if none of the chip-selects or DRAM bank match the address decode. All 16 bits of the data bus are driven during writes, regardless of port width or operand size.

3.2.5 Transfer Acknowledge

The $\overline{TA}$/GPIO12 pin is the transfer acknowledge signal.

3.3 SDRAM Controller Signals

The following SDRAM signals provide a glueless interface to external SDRAM. An SDRAM width of 16 bits is supported and can access as much as 32MB of memory. ADRAMs are not supported.

Table 3. SDRAM Controller Signals

SDRAM Signal	Description
Synchronous DRAM row address strobe	The $\overline{SDRAS}$/GPIO59 active low pin provides a seamless interface to the RAS input on synchronous DRAM
Synchronous DRAM Column Address Strobe	The $\overline{SDCAS}$/GPIO39 active low pin provides a seamless interface to CAS input on synchronous DRAM.
Synchronous DRAM Write	The $\overline{SDWE}$/GPIO38 active-low pin is asserted to signify that a SDRAM write cycle is underway. This pin outputs logic ‘1’ during read bus cycles.
Synchronous DRAM Chip Enable	The $\overline{SD\_CS0}$/GPIO60 active-low output signal is used during synchronous mode to route directly to the chip select of a SDRAM device.
Synchronous DRAM UDQM and LQDM signals	The DRAM byte enables UDMQ and LDQM are driven by the SDUDQM/GPO53 and SDLDQM/GPO52 byte enable outputs.
Synchronous DRAM clock	The DRAM clock is driven by the BCLK/GPIO40 signal
Synchronous DRAM Clock Enable	The BCLKE active high output signal is used during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM.

3.4 Chip Selects

There are three chip select outputs on the SCF5250 device. $\overline{CS0}$/$\overline{CS4}$ and $\overline{CS1}$/QSPI_CS3/GPIO28 and CS2 which is associated with the IDE interface read and write strobes - IDE-DIOR and IDE-DIOW.

CS0 and CS4 are multiplexed. The SCF5250 has the option to boot from an internal Boot ROM. The function of the CS0/CS4 pin is determined by the boot mode. When the device is booted from internal ROM, the internal ROM is accessed with CS0 (required for boot) and the CS0/CS4 pin is driven by CS4. When the device is booted from external ROM / Flash, the CS0/CS4 pin is driven by CS0 and the internal ROM is disabled.

The active low chip selects can be used to access asynchronous memories. The interface is glueless.

3.5 ISA Bus

The SCF5250 supports an ISA bus. Using the ISA bus protocol, reads and writes for one ISA bus peripheral is possible. $\overline{IDE\text{-}DIOR}$/GPIO31 and $\overline{IDE\text{-}DIOW}$/GPIO32 are the read and write strobe. The peripheral can insert wait states by pulling IDE-IORDY/GPIO33.

CS2 is associated with the IDE-DIOR and IDE-DIOW.

3.6 Bus Buffer Signals

As the SCF5250 has a complicated slave bus, which allows SDRAM, asynchronous memories, and ISA peripherals on the bus, it may become necessary to introduce a buffer on the bus in certain applications. The SCF5250 has a glueless interface to steer these bus buffers with two bus buffer output signals $\overline{BUFENB1}$/GPIO29 and $\overline{BUFENB2}$/GPIO30.

3.7 I^2C Module Signals

There are two I^2C interfaces on this device as described in Table 4.

The I^2C module acts as a two-wire, bidirectional serial interface between the SCF5250 processor and peripherals with an I^2C interface (e.g., LED controller, A-to-D converter, D-to-A converter). When devices connected to the I^2C bus drive the bus, they will either drive logic-0 or high-impedance. This can be accomplished with an open-drain output.

Table 4. I^2C Module Signals

I^2c Module Signal	Description
I^2C Serial Clock	The SCL0/SDATA1_BS1/GPIO41 and SCL1/TXD1/GPIO10 bidirectional signals are the clock signal for first and second I^2C module operation. The I^2C module controls this signal when the bus is in master mode; all I^2C devices drive this signal to synchronize I^2C timing. Signals are multiplexed
I^2C Serial Data	The SDA0/SDATA3/GPIO42 and SDA1/RXD1/GPIO44 bidirectional signals are the data input/output for the first and second serial I^2C interface. Signals are multiplexed

3.12 Subcode Interface

There is a 3-line subcode interface on the SCF5250 processor. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 9.

Table 9. Subcode Interface Signal

Signal name	Description
RCK/QSPI_DIN/QSPI_DOUT/GPIO26	Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder.
QSPI_DOUT/SFSY/GPIO27	Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream.
QSPI_CLK/SUBR/GPIO25	Subcode data output This signal is a subcode data out pin.

3.13 Analog to Digital Converter (ADC)

The ADOUT signal on the ADOUT/SCLK4/GPIO58 pin provides the reference voltage in PWM format. This output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be input to the ADREF pin.

The six AD inputs are each fed to their own comparator. The reference input to each (ADREF) is then multiplexed as only one AD comparison can be made at any one time.

NOTE

To use the ADINx as General Purpose inputs (rather than there analogue function) it is necessary to generate a fixed comparator voltage level of VDD/2. This can be accomplished by a potential divider network connected to the ADREF pin. However in portable applications where stand-by power consumption is important the current taken by the divider network (in stand-by mode) could be excessive. Therefore it is possible to generate a VDD/2 voltage by selecting SCLK4 output mode and feeding this clock signal (which is 50% duty cycle) through an external integration circuit. This would generate a voltage level equal to VDD/2 but would be disabled when stand-by mode was selected.

3.14 Secure Digital/Memory Stick Card Interface

The device has a versatile flash card interface that supports both Secure Digital and Memory Stick cards. The interface can either support one Secure Digital or two Memory Stick cards. No mixing of card types is possible. Table 10 gives the pin descriptions.

Table 10. Flash Memory Card Signals

Flash Memory Signal	Description
EBUIN2/SCLKOUT/GPIO13	Clock out for both Memory Stick interfaces and for Secure Digital
EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command line Memory Stick interface 2 data I/O

3.18 Debug and Test Signals

These signals interface with external I/O to provide processor debug and status signals.

3.18.1 Test Mode

The TEST[2:0] inputs are used for various manufacturing and debug tests. For normal mode TEST [2:1] should be ways be tied low. TEST0 should be set high for BDM debug mode and set low for JTAG mode.

3.18.2 High Impedance

The assertion of $\overline{\text{HI\_Z}}$ will force all output drivers to a high-impedance state. The timing on $\overline{\text{HI\_Z}}$ is independent of the clock.

NOTE

JTAG operation will override the $\overline{\text{HI\_Z}}$ pin.

3.18.3 Processor Clock Output

The internal PLL generates this PSTCLK/GPIO51 and output signal, and is the processor clock output that is used as the timing reference for the Debug bus timing (DDATA[3:0] and PST[3:0]). The PSTCLK/GPIO51 is at the same frequency as the core processor.

3.18.4 Debug Data

The debug data pins, DDATA0/CTS1/SDATA0_SDIO1/GPIO1, DDATA1/RTS1/SDATA2_BS2/GPIO2, DDATA2/CTS0/GPIO3, and DDATA3/RTS0/GPIO4, are four bits wide. This nibble-wide bus displays captured processor data and break-point status.

3.18.5 Processor Status

The processor status pins, PST0/GPIO50, PST1/GPIO49, PST2/INTMON/GPIO48, and PST3/INTMON/GPIO47, indicate the SCF5250 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. Table 12 shows the encodings of these signals.

Table 12. Processor Status Signal Encodings

PST[3:0]		Definition
(HEX)	(BINARY)	
$0	0000	Continue execution
$1	0001	Begin execution of an instruction
$2	0010	Reserved
$3	0011	Entry into user-mode
$4	0100	Begin execution of PULSE and WDDATA instructions
$5	0101	Begin execution of taken branch or Synch_PC[1]
$6	0110	Reserved
$7	0111	Begin execution of RTE instruction
$8	1000	Begin 1-byte data transfer on DDATA
$9	1001	Begin 2-byte data transfer on DDATA
$A	1010	Begin 3-byte data transfer on DDATA
$B	1011	Begin 4-byte data transfer on DDATA
$C	1100	Exception processing[2]
$D	1101	Emulator mode entry exception processing[2]
$E	1110	Processor is stopped, waiting for interrupt[2]
$F	1111	Processor is halted[2]

1 Rev. B enhancement.

2 These encodings are asserted for multiple cycles.

3.19 BDM/JTAG Signals

The SCF5250 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

3.20 Clock and Reset Signals

The clock and reset signals configure the SCF5250 processor and provide interface signals to the external system.

3.20.1 Reset In

Asserting $\overline{\text{RSTI}}$ causes the SCF5250SCF5250 to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the data bus is tri-stated.

Table 17 provides the linear regulator operating specifications for the SCF5250 processor.

Table 17. Linear Regulator[1] Operating Specification

Characteristic	Symbol	Min	Typ	Max
Input Voltage	Vin	3.0V	3.3V	3.6
Output Voltage (LINOUT)	Vout	1.14V	1.2V	1.26V
Output Current	Iout	–	100mA	150mA
Power Dissipation	Pd	–	–	436uW
Load Regulation (10% Iout ≥ 90% Iout)	–	40mV	50mV	60mV
Power Supply Rejection	PSRR	–	40dB	–

1 A pmos regulator is employed as a current source in this Linear regulator, so a 10µF capacitor (ESR 0 ... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically this will require the use of a Tantalum type capacitor.

Table 18 provides the DC electrical specifications.

Table 18. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current @ 0.0 V /3.3 V During Normal Operation	I_{in}	–	±1	µµA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	µµA
Output High Voltage I_{OH} = 8mA[1], 4mA[2], 2mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 8mA[1], 4mA[2], 2mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[6]	V_{T+}	1.47	–	V
Schmitt Trigger High to Low Threshold Point[6]	V_{T-}	–	.95	V
Load Capacitance (DATA[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, DDATA[3:0], PST[3:0], PSTCLK, IDE-DIOR, IDE-DIOW, IORDY)	C_L	–	50	pF
Load Capacitance (ADDR[24:9], BCLK)	C_L	–	40	pF
Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SD_CS0, SDUDQM, SDWE, BUFENB[2:1])	C_L	–	30	pF
Load Capacitance (SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, R/$\overline{W}$, TA, TXD[1:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], GP[6:5])	C_L	–	20	pF

Figure 6 and Table 24 provide the timing diagram and timing parameters for the Timer module.

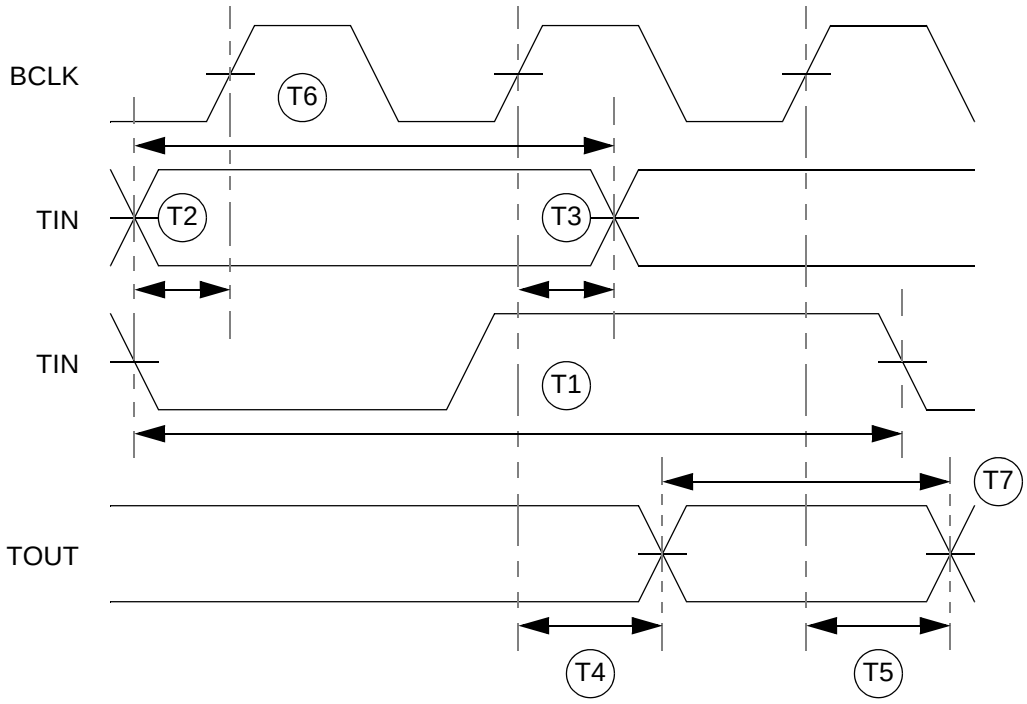

Figure 6. Timer Module AC Timing Definition Diagram

Table 24. Timer Module AC Timing Specification

Num	Characteristic	Min	Max	Units
T1	TIN Cycle time	3T	–	bus clocks
T2	TIN Valid to BCLK (input setup)	6	–	ns
T3	BCLK to TIN Invalid (input hold)	0	–	ns
T4	BCLK to TOUT Valid (output valid)	–	10	ns
T5	BCLK to TOUT Invalid (output hold)	tbd	–	ns
T6	TIN Pulse Width	1T	–	bus clocks
T7	TOUT Pulse Width	1T	–	bus clocks

Figure 11 provides the IEEE 1149.1 JTAG timing diagram and Table 30 provides the timing parameters.

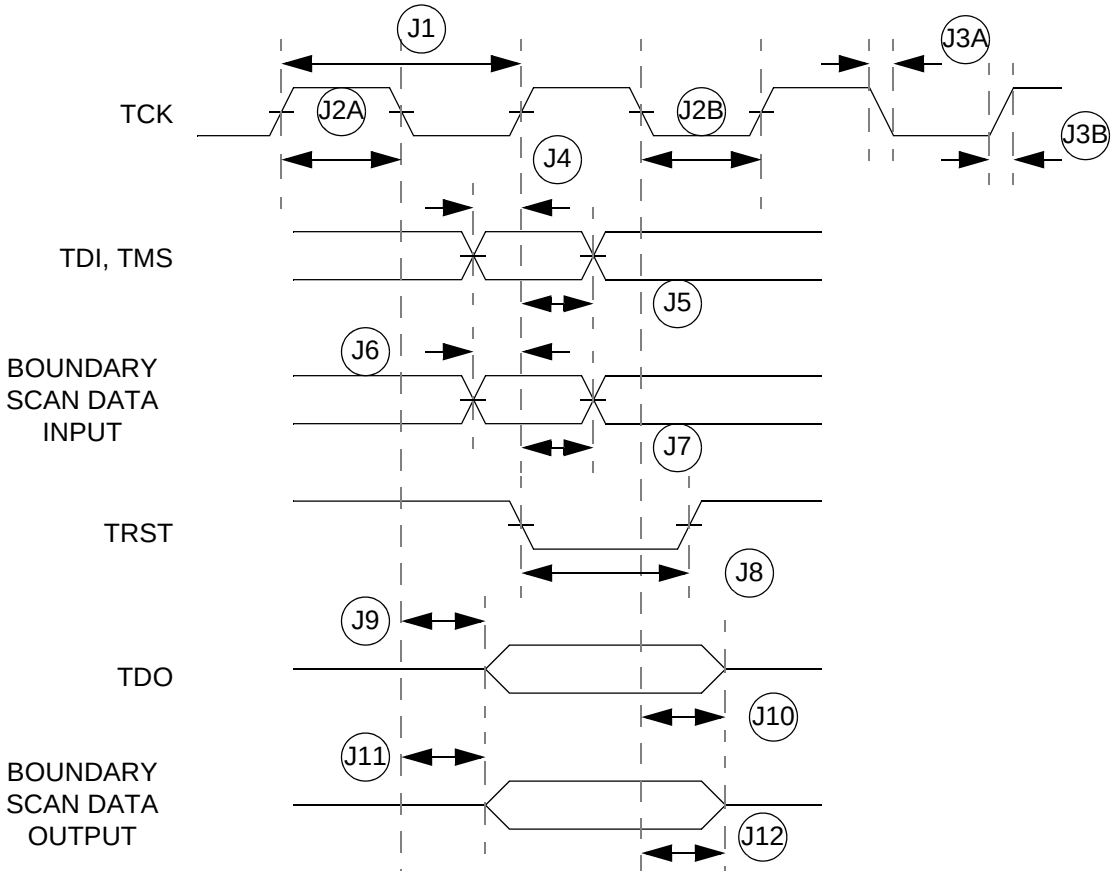

Figure 11. JTAG AC Timing Diagram

Table 30. JTAG AC Timing Specifications

Num	Characteristic	Min	Max	Units
–	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	–	ns
J2a	TCK Clock Pulse High Width	25	–	ns
J2b	TCK Clock Pulse Low Width	25	–	ns
J3a	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	–	5	ns
J3b	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	–	5	ns
J4	TDI, TMS to TCK rising (Input Setup)	8	–	ns
J5	TCK rising to TDI, TMS Invalid (Hold)	10	–	ns
J6	Boundary Scan Data Valid to TCK (Setup)	tbd	–	ns
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	tbd	–	ns
J8	$\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges)	12	–	ns
J9	TCK falling to TDO Valid (signal from driven or three-state)	–	15	ns
J10	TCK falling to TDO High Impedance	–	15	ns

Figure 14 provides the SCLK input/output, SDATA input timing diagram and Table 33 provides the timing parameters.

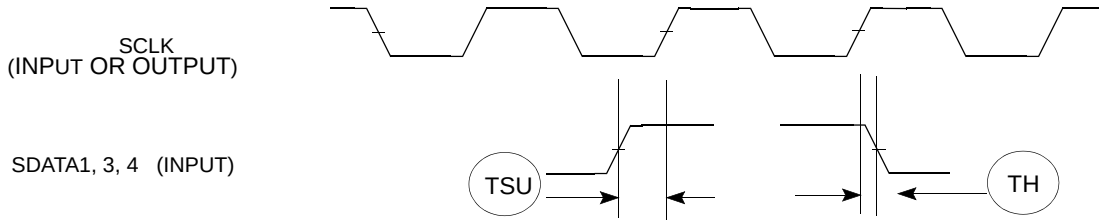

Figure 14. SCLK Input/Output, SDATA Input Timing Diagram

Table 33. SCLK Input/Output, SDATA Input Timing Specifications

Num	Characteristic	Min	Max	Units
TSU	SDATAI IN to SCLKn	-5	–	ns
TH	SCLK rise to SDATAI	3	–	ns

5 Pin-Out and Package Information

Visit the URL [http://www.freescale.com/coldfire] and choose the documentation library to obtain information on the mechanical characteristics of the SCF5250 integrated microprocessor. Thermal characteristics are not available at this time.

The SCF5250 is available in a 144 pin QFP and a 196 pin MAPBGA package. Use Table 34 to find the information desired.

Table 34. Section Quick Reference

For Chip Package		See
144 pin QFP	Pin assignments	Table 35 on page 37
	Package drawings	Figure 15 on page 42 Figure 16 on page 43 Figure 17 on page 44
196 MAPBGA	Pin assignments	Table 36 on page 45
	Package drawings	Figure 18 on page 52 Figure 19 on page 53
	Ball map	Figure 20 on page 54

5.1 144 QFP Pin Assignments

The SCF5250 can be assembled in 144-pin QFP package. Table 35 provides the pin assignments for the package.

Table 35. 144 QFP Pin Assignments

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
01	DATA16	I/O	Data	X
02	A23/GPO54	I/O	SDRAM address / static adr	Out (requires pull up /down for boot-up selection)
03	PAD-VDD	–	–	–
04	A22	O	SDRAM address / static adr	Out
05	A21	O	SDRAM address / static adr	Out
06	A20/A24	O	SDRAM address / static adr	Out
07	A19	O	SDRAM address / static adr	Out
08	A18	O	SDRAM address / static adr	Out
09	PAD-GND	–	–	–
10	A17	O	SDRAM address / static adr	Out
11	A16	O	SDRAM address / static adr	Out
12	A15	O	SDRAM address / static adr	Out
13	A14	O	SDRAM address / static adr	Out
14	A13	O	SDRAM address / static adr	Out
15	PAD-VDD	–	–	–
16	A12	O	SDRAM address / static adr	Out
17	A11	O	SDRAM address / static adr	Out
18	CORE-VDD	–	–	–
19	CORE-GND	–	–	–
20	A10	O	SDRAM address / static adr	Out
21	A9	O	SDRAM address / static adr	Out
22	A8	O	SDRAM address / static adr	Out
23	A7	O	SDRAM address / static adr	Out
24	A6	O	SDRAM address / static adr	Out
25	A5	O	SDRAM address / static adr	Out
26	PAD-GND	–	PAD-GND	–
27	A4	O	SDRAM address / static adr	Out
28	A3	O	SDRAM address / static adr	Out
29	A2	O	SDRAM address / static adr	Out
30	A1	O	SDRAM address / static adr	Out
31	CS0/CS4	O	Static chip select 0 / static chip select 4	Out

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
59	QSPI_CS1/EBUOUT2/ GPIO16	I/O	QSPI Chip select 1 output / audio interface EBU output 2	Out / LOW
60	QSPI_CS0/EBUIN4/ GPIO15	I/O	QSPI chip select 0 / audio interface EBUIN 4	Out / LOW
61	PAD GND	–	–	–
62	SCLK1/GPIO20	I/O	Audio interfaces serial clock 1	In / LOW
63	LRCK1/GPIO19	I/O	Audio interfaces word clock 1	In / LOW
64	SDATAO1/TOUT0/ GPIO18	I/O	Audio interfaces serial data output 1 / Timer output 0	Out / LOW
65	SDATAI1/GPIO17	I	Audio interfaces serial data in 1	In / LOW
66	CFLG/GPIO5	I/O	CFLG input	In / LOW
67	EF/GPIO6	I/O	Error flag input	In / LOW
68	QSPI_CS2/MCLK2/ GPIO24	I/O	QSPI Chip Select output 2 / audio master clock output 2	Out / LOW
69	SDATAI3/GPIO8	I/O	Audio interfaces serial data input 3	In / LOW
70	ADIN0/GPI52	A	AD input 0	In only
71	ADIN1/GPI53	A	AD input 1	In only
72	ADIN2/GPI54	A	AD input 2	In only
73	ADVDD	–	–	–
74	ADGND	–	–	–
75	ADIN3/GPI55	A	AD input 3	In only
76	ADIN4/GPI56	A	AD input 4	In only
77	ADIN5/GPI57	A	AD input 5	In only
78	ADREF	A	ADC reference input	In
79	ADOUT/SCLK4/ GPIO58	I/O	AD output / SCLK4 (for GPI function in low power applications)	Out / clock output
80	LRCK3/GPIO43/ AUDIO_CLOCK	I/O	Audio interface LRCK3 / Audio master clock input	In / LOW
81	SCLK3/GPIO35	I/O	Audio interface SCLK3	In / LOW
82	SCL0/SDATA1_BS1/ GPIO41	I/O	I2C0 clock line / FlashMedia Data interface	Out / LOW
83	SDA0/SDATA3/GPIO42	I/O	I2C0 data / FlashMedia data interface	Hi-Z
84	DDATA0/CTS1/ SDATA0_SDIO1/GPIO1	I/O	Debug / UART1 CTS / FlashMedia data interface	Out / HIGH
85	DDATA1/RTS1/ SDATA2_BS2/GPIO2	I/O	Debug / UART1 RTS / FlashMedia data interface	Out / HIGH

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS D AND E ARE DETERMINED AT THE SEATING PLANE, DATUM A.

DIM	MIN	MAX	DIM	MIN	MAX	DIM	MIN	MAX
A	–	1.6	L1	– 1 REF	–	–	–	–
A1	0.05	0.15	L2	– 0.5 REF	–	–	–	–
A2	1.35	1.45	R1	0.13	0.2	–	–	–
b	0.17	0.27	R2	0.13	–	–	–	–
b1	0.17	0.23	S	– 0.25 REF	–	–	–	–
c	0.09	0.20	θ	0°	7°	–	–	–
c1	0.09	0.16	θ1	0°	–	–	–	–
D	– 22 BSC	–	θ2	– 12° REF	–	–	–	–
D1	– 20 BSC	–	–	–	–	–	–	–
e	– 0.5 BSC	–	–	–	–	–	–	–
E	– 22 BSC	–	–	–	–	–	–	–
E1	– 20 BSC	–	–	–	–	–	–	–
L	0.45	0.75	–	–	–	–	–	–

TITLE:	CASE NUMBER: 918-03	
144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	STANDARD: MOTOROLA	
	PACKAGE CODE: 8259	SHEET: 3 OF 3

Figure 17. 144 QFP Package (3 of 3)

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
N5	WAKEUP_GP21	I/O	Wake-up input	In (requires pull-up for normal operation)
P3	EBUIN2_SCLKOUT_GP13	I/O	Audio interfaces EBUIN2 / FlashMedia Clock	In / Low
P4	EBUIN3_CMDSDIO2_GP14	I/O	Audio interfaces EBUIN3 / FlashMedia Clock	In / Low
P_VDD	PAD_VDD	I/O	PAD_VDD	
N6	EBUIN1_GP36	I/O	Audio interfaces EBUIN1	In / Low
P5	EBUOUT1_GP37	I/O	Audio interfaces EBUOUT1	Out / Low
M7	XTRIM_GP0	I/O	Audio interfaces X-tal trim	Out / clock out
P6	QSPICS3_CS1_GP28	I/O	QSPI Chip select 3	Out / High
N7	RCK_QSPIDIN_QSPIDOUT_GP26	I/O	Subcode RCK interface / QSPI Data In / Data out	Out / Low
P7	QSPICLK_SUBR_GP25	I/O	QSPI clockpin / subcode interface	Out / Low
P8	QSPIDOUT_SFSY_GP27	I/O	QSPI Data Output / subcode interface SFSY	Out / Low
M8	QSPICS1_EBUOUT2_GP16	I/O	QSPI Chip select 1 output / audio interface EBU output 2	Out / Low
N8	QSPICS0_EBUIN4_GP15	I/O	QSPI Chip select 0 output / audio interface EBUIN4	Out / Low
P_GND	PAD_GND	I/O	PAD_GND	
P9	SCLK1_GP20	I/O	Audio interfaces serial clock 1	In / Low
M9	LRCK1_GP19	I/O	Audio interfaces word clock 1	In / Low
N9	SDATAO1_TOUT1_GP18	I/O	Audio interfaces serial data output 1 / Timer output 1	Out / Low
P10	SDATAI1_GP17	I/O	Audio interfaces serial data input 1	In / Low
N10	CFLG_GP5	I/O	CFLG input	In / Low
M10	EF_GP6	I/O	Error flag input	In / Low
P11	QSPICS2_MCLK2_GP24	I/O	QSPI Chip select output 2 / audio master clock output 2	Out / Low
N11	SDATAI3_GP8	I/O	Audio interfaces serial data input 3	In / Low

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		PAGE 1128C	
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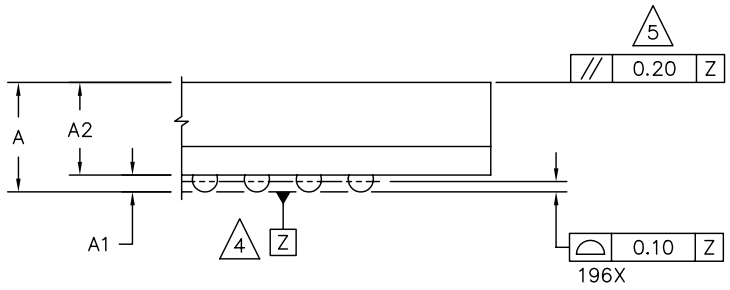

DETAIL K
ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE	CASE NUMBER: 1128C–01	
196 I/O STD MAP BGA, 15 X 15 PKG, 1.00 PITCH	STANDARD: MOTOROLA	
	REFERENCE: U, X	SHEET 2 OF 2

Figure 19. 196 MAPBGA Package (2 of 2)