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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	57
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/scf5250cag120

1.2.2 DMA Controller

The SCF5250 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

1.2.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

1.2.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5250 processor uses a 8K-byte, direct-mapped instruction cache to achieve 107 MIPS at 120 MHz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

1.2.5 Internal 128-KByte SRAM

The 128-KByte on-chip SRAM is available in two banks, SRAM0 (64K) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in SRAM1 can be accessed under DMA.

1.2.6 SDRAM Controller

The SCF5250 SDRAM controller provides a glueless interface for one bank of SDRAM up to 32 MB (256 Mbits). The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

1.2.16 IDE and SmartMedia Interfaces

The SCF5250 system bus allows connection of an IDE hard disk drive or SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5250.

Low cost version SCF5250LPV100 and SCF5250LAG100 does not run production test for the IDE/CF/SD/MMC interfaces. Freescale does not guarantee these interfaces will work on these two devices.

1.2.17 Analog/Digital Converter (ADC)

The six channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. Both the analogue comparator and digital sections of the ADC are provided internally. An external integrator circuit (resistor/capacitor) is required, which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

1.2.18 I^2C Module

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

1.2.19 Chip-Selects

Up to four programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

1.2.20 GPIO Interface

A total of 60 General Purpose inputs and 57 General Purpose outputs are available. These are multiplexed with various other signals. Seven of the GPIO inputs have edge sensitive interrupt capability.

1.2.21 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 7 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

Table 2. SCF5250 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[24:1] A[23]/GPO54	24 address lines, address line 23 multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only).	Out	X
Read-write control	R/$\overline{W}$	Bus write enable - indicates if read or write cycle in progress	Out	H
Output enable	OE	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	$\overline{SDRAS}$/GPIO59	Row address strobe for external SDRAM.	Out	negated
Synchronous column address strobe	$\overline{SDCAS}$/GPIO39	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	$\overline{SDWE}$/GPIO38	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	$\overline{SDUDQM}$/GPO53	Indicates during write cycle if high byte is written	Out	–
SDRAM lower byte enable	$\overline{SDLDQM}$/GPO52	Indicates during write cycle if low byte is written	Out	–
SDRAM chip selects	$\overline{SD\_CS0}$/GPIO60	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE/GPIO63	SDRAM clock enable	Out	–
System clock	BCLK/GPIO40	SDRAM clock output	In/Out	–
ISA bus read strobe	$\overline{IDE\text{-}DIOR}$/GPIO31 (CS2)	There is 1 ISA bus read strobe and 1 ISA bus write strobe. They allow connection of one independent ISA bus peripherals, e.g. an IDE slave device.	In/Out	–
ISA bus write strobe	$\overline{IDE\text{-}DIOW}$/GPIO32 (CS2)		In/Out	–
ISA bus wait signal	$\overline{IDE\text{-}IORDY}$/GPIO33	ISA bus wait line - available for both busses	In/Out	–
Chip Selects[2:0]	$\overline{CS0}$/$\overline{CS4}$ $\overline{CS1}$/QSPI_CS3/GPIO28	Enables peripherals at programmed addresses. $\overline{CS}$[0] provides boot ROM selection	Out In/Out	negated
Buffer enable 1	$\overline{BUFENB1}$/GPIO29	Two programmable buffer enables allow seamless steering of external buffers to split data and address bus in sections.	In/Out	–
Buffer enable 2	$\overline{BUFENB2}$/GPIO30		In/Out	–
Transfer acknowledge	$\overline{TA}$/GPIO12	Transfer Acknowledge signal	In/Out	–
Wake Up	$\overline{WAKE\_UP}$/GPIO21	Wake-up signal input	In	–
Serial Clock Line	SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10	Clock signal for Dual I^2C module operation	In/Out	–
Serial Data Line	SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44	Serial data port for second I^2C module operation	In/Out	–
Receive Data	SDA1/RXD1/GPIO44 RXD0/GPIO46	Signal is receive serial data input for DUART	In	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45	Signal is transmit serial data output for DUART	Out	–
Request-To-Send	DDATA3/$\overline{\text{RTS0}}$/GPIO4 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	DUART signals a ready to receive data query	Out	–
Clear-To-Send	DDATA2/$\overline{\text{CTSO}}$/GPIO3 DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Signals to DUART that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capable of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLK_OUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPI_CS0/EBUIN4/GPIO15	audio interfaces IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPI_CS1/EBUOUT2/GPIO16	audio interfaces IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	audio interfaces serial data inputs	In	–
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	audio interfaces serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/GPIO43/AUDIO_CLOCK	audio interfaces serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	audio interfaces serial bit clocks	In/Out	–
Serial input	EF/GPIO6	error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPI_DIN/QSPI_DOUT/ GPIO26	audio interfaces subcode clock	In/Out	–
Subcode sync	QSPI_DOUT/SFSY/GPIO27	audio interfaces subcode sync	In/Out	–
Subcode data	QSPI_CLK/SUBR/GPIO25	audio interfaces subcode data	In/Out	–
Clock frequency trim	XTRIM/GPIO0	clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPI_CS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/GPIO43/AUDIO_CLOCK	Optional Audio clock Input	–	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Processor Status	PST0/GPIO50 PST1/GPIO49 PST2/INTMON2/GPIO48 PST3/INTMON1/GPIO47	Indicates internal processor status.	In/Out	Hi-Z
Processor Clock	PSTCLK/GPIO51	processor clock output	Out	–
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG.	In	–
Test Reset/Development Serial Clock	$\overline{\text{TRST}}$/DSCLK	Multiplexed signal that is asynchronous reset for JTAG controller. Clock input for debug module.	In	–
Test Mode Select/ Break Point	TMS/$\overline{\text{BKPT}}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode.	In	–
Test Data Input / Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	–
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module.	Out	–

3.1 GPIO

Many pins have an optional GPIO function.

- General purpose input is always active, regardless of state of pin.
- General purpose output or primary output is determined by the appropriate setting of the Pin Multiplex Control Registers, GPIO-FUNCTION, GPIO1-FUNCTION and PIN-CONFIG.
- At Power-on reset, all pins are set to their primary function.

3.2 SCF5250 Bus Signals

These signals provide the external bus interface to the SCF5250 processor.

3.2.1 Address Bus

- The address bus provides the address of the byte or most significant byte of the word or longword being transferred. The address lines also serve as the DRAM address pins, providing multiplexed row and column address signals.
- Bits 23 down to 1 and 24 of the address are available. A24 is intended to be used with 256 Mbit DRAM's. Signals are named:
  - A[23:1]
  - A20/24

3.12 Subcode Interface

There is a 3-line subcode interface on the SCF5250 processor. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 9.

Table 9. Subcode Interface Signal

Signal name	Description
RCK/QSPI_DIN/QSPI_DOUT/GPIO26	Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder.
QSPI_DOUT/SFSY/GPIO27	Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream.
QSPI_CLK/SUBR/GPIO25	Subcode data output This signal is a subcode data out pin.

3.13 Analog to Digital Converter (ADC)

The ADOUT signal on the ADOUT/SCLK4/GPIO58 pin provides the reference voltage in PWM format. This output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be input to the ADREF pin.

The six AD inputs are each fed to their own comparator. The reference input to each (ADREF) is then multiplexed as only one AD comparison can be made at any one time.

NOTE

To use the ADINx as General Purpose inputs (rather than there analogue function) it is necessary to generate a fixed comparator voltage level of VDD/2. This can be accomplished by a potential divider network connected to the ADREF pin. However in portable applications where stand-by power consumption is important the current taken by the divider network (in stand-by mode) could be excessive. Therefore it is possible to generate a VDD/2 voltage by selecting SCLK4 output mode and feeding this clock signal (which is 50% duty cycle) through an external integration circuit. This would generate a voltage level equal to VDD/2 but would be disabled when stand-by mode was selected.

3.14 Secure Digital/Memory Stick Card Interface

The device has a versatile flash card interface that supports both Secure Digital and Memory Stick cards. The interface can either support one Secure Digital or two Memory Stick cards. No mixing of card types is possible. Table 10 gives the pin descriptions.

Table 10. Flash Memory Card Signals

Flash Memory Signal	Description
EBUIN2/SCLKOUT/GPIO13	Clock out for both Memory Stick interfaces and for Secure Digital
EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command line Memory Stick interface 2 data I/O

Table 12. Processor Status Signal Encodings

PST[3:0]		Definition
(HEX)	(BINARY)	
$0	0000	Continue execution
$1	0001	Begin execution of an instruction
$2	0010	Reserved
$3	0011	Entry into user-mode
$4	0100	Begin execution of PULSE and WDDATA instructions
$5	0101	Begin execution of taken branch or Synch_PC[1]
$6	0110	Reserved
$7	0111	Begin execution of RTE instruction
$8	1000	Begin 1-byte data transfer on DDATA
$9	1001	Begin 2-byte data transfer on DDATA
$A	1010	Begin 3-byte data transfer on DDATA
$B	1011	Begin 4-byte data transfer on DDATA
$C	1100	Exception processing[2]
$D	1101	Emulator mode entry exception processing[2]
$E	1110	Processor is stopped, waiting for interrupt[2]
$F	1111	Processor is halted[2]

1 Rev. B enhancement.

2 These encodings are asserted for multiple cycles.

3.19 BDM/JTAG Signals

The SCF5250 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

3.20 Clock and Reset Signals

The clock and reset signals configure the SCF5250 processor and provide interface signals to the external system.

3.20.1 Reset In

Asserting $\overline{\text{RSTI}}$ causes the SCF5250SCF5250 to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the data bus is tri-stated.

Table 14. Maximum Ratings

Rating	Symbol	Value	Units
Supply Core Voltage	V_{cc}	-0.5 to +2.5	V
Maximum Core Operating Voltage	V_{cc}	+1.32	V
Minimum Core Operating Voltage	V_{cc}	+1.08	V
Supply I/O Voltage	V_{cc}	-0.5 to +4.6	V
Maximum I/O Operating Voltage	V_{cc}	+3.6	V
Minimum I/O Operating Voltage	V_{cc}	+3.0	V
Input Voltage	V_{in}	-0.5 to +6.0	V
Storage Temperature Range	T_{stg}	-65 to150	°C

Table 15 provides the recommended operating temperatures for the SCF5250 processor.

Table 15. Operating Temperature

Characteristic	Symbol	Value	Units
Maximum Operating Ambient Temperature	T_{Amax}	85[1]	°C
Minimum Operating Ambient Temperature	T_{Amin}	-40	°C

1 This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature does not exceed 105°C.

Table 16 provides the recommended operating supply voltages for the SCF5250 processor.

Table 16. Recommended Operating Supply Voltages

Pin Name	Min	Typ	Max
CORE-VDD	1.08V	1.2V	1.32V
CORE-VSS	–	gnd	–
PAD-VDD	3.0V	3.3v	3.6V
PAD-VSS	–	gnd	–
ADVDD	3.0V	3.3v	3.6V
ADGND	–	gnd	–
OSCPAD-VDD	3.0V	3.3v	3.6V
OSCPAD-GND	–	gnd	–
PLLCORE1VDD	1.08V	1.2V	1.32V
PLLCORE1GND	–	gnd	–
PLLCORE2VDD	1.08V	1.2v	1.32V
PLLCORE2GND	–	gnd	–
LIN	3.0v	3.3V	3.6V

Table 17 provides the linear regulator operating specifications for the SCF5250 processor.

Table 17. Linear Regulator[1] Operating Specification

Characteristic	Symbol	Min	Typ	Max
Input Voltage	Vin	3.0V	3.3V	3.6
Output Voltage (LINOUT)	Vout	1.14V	1.2V	1.26V
Output Current	Iout	–	100mA	150mA
Power Dissipation	Pd	–	–	436uW
Load Regulation (10% Iout ≥ 90% Iout)	–	40mV	50mV	60mV
Power Supply Rejection	PSRR	–	40dB	–

1 A pmos regulator is employed as a current source in this Linear regulator, so a 10µF capacitor (ESR 0 ... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically this will require the use of a Tantalum type capacitor.

Table 18 provides the DC electrical specifications.

Table 18. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current @ 0.0 V /3.3 V During Normal Operation	I_{in}	–	±1	µµA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	µµA
Output High Voltage I_{OH} = 8mA[1], 4mA[2], 2mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 8mA[1], 4mA[2], 2mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[6]	V_{T+}	1.47	–	V
Schmitt Trigger High to Low Threshold Point[6]	V_{T-}	–	.95	V
Load Capacitance (DATA[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, DDATA[3:0], PST[3:0], PSTCLK, IDE-DIOR, IDE-DIOW, IORDY)	C_L	–	50	pF
Load Capacitance (ADDR[24:9], BCLK)	C_L	–	40	pF
Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SD_CS0, SDUDQM, SDWE, BUFENB[2:1])	C_L	–	30	pF
Load Capacitance (SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, R/$\overline{W}$, TA, TXD[1:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], GP[6:5])	C_L	–	20	pF

Figure 3 and Figure 4 provide the input and output AC timing definition diagrams and Table 21 and Table 22 provide the input and output AC timing parameters.

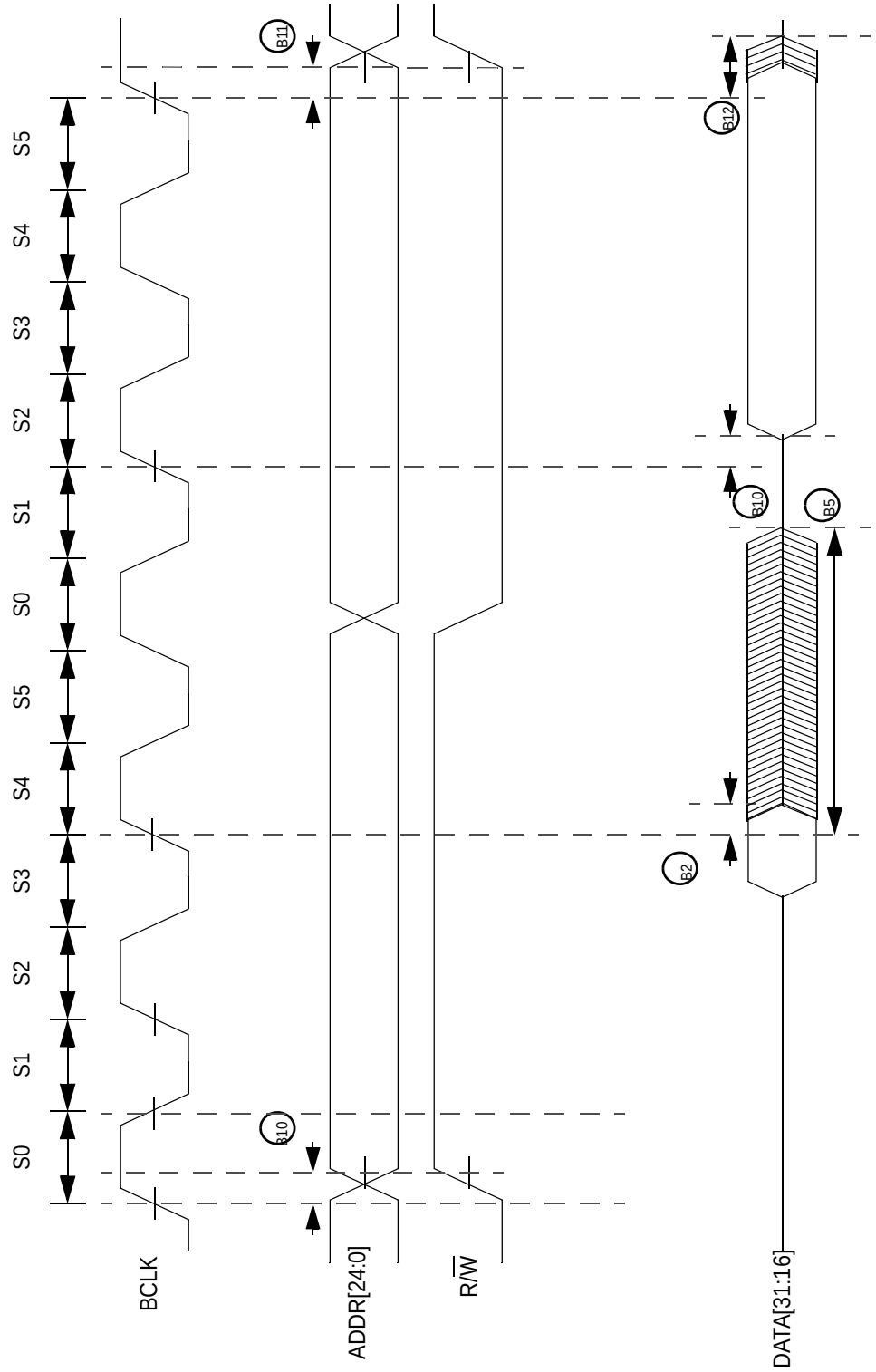

Figure 3. Input/Output Timing Definition-I

Table 22. Output AC Timing Specification (continued)

Num	Characteristic[1]	Min	Max	Units
H1	$\overline{HIZ}$ to High Impedance	–	tbd	ns
H2	$\overline{HIZ}$ to Low Impedance	–	tbd	ns

1 AC timing specs assume 40pF load capacitance on BCLK and a 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 Outputs (8mA): DATA[31:16], ADDR[25,23:9]

3 Outputs (4mA): SDRAS, SDCAS, SDWE, SD_CS0, SDUDQM, SDLDQM, BCLKE

4 High Impedance (Three-State): DATA[31:16]

Figure 5 and Table 23 provide the timing diagram and timing parameters for the Debug AC.

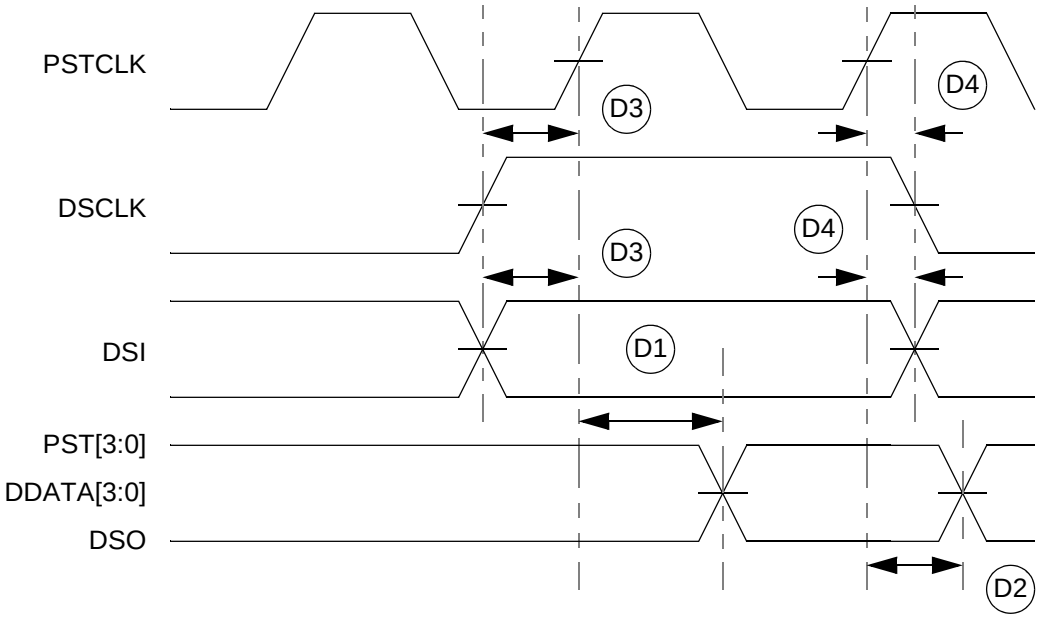

Figure 5. Debug AC Timing Definition Diagram

Table 23. Debug AC Timing Specification[1]

Num	Characteristic	Min	Max	Units
D1	PSTCLK to signal Valid (Output valid)	–	6	ns
D2	PSTCLK to signal Invalid (Output hold)	1.8	–	ns
D3[2]	Signal Valid to PSTCLK (Input setup)	3	–	ns
D4	PSTCLK to signal Invalid (Input hold)	5	–	ns

1 AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.

Figure 14 provides the SCLK input/output, SDATA input timing diagram and Table 33 provides the timing parameters.

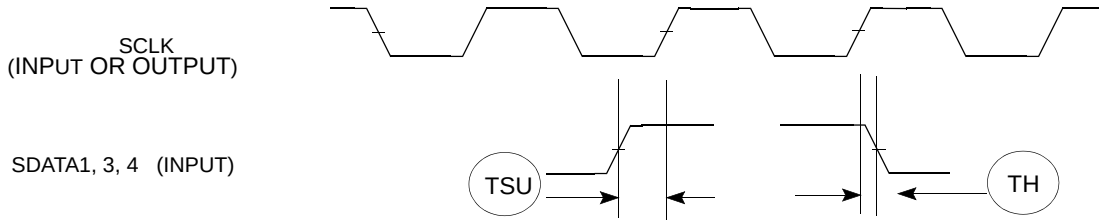

Figure 14. SCLK Input/Output, SDATA Input Timing Diagram

Table 33. SCLK Input/Output, SDATA Input Timing Specifications

Num	Characteristic	Min	Max	Units
TSU	SDATAI IN to SCLKn	-5	–	ns
TH	SCLK rise to SDATAI	3	–	ns

5 Pin-Out and Package Information

Visit the URL [http://www.freescale.com/coldfire] and choose the documentation library to obtain information on the mechanical characteristics of the SCF5250 integrated microprocessor. Thermal characteristics are not available at this time.

The SCF5250 is available in a 144 pin QFP and a 196 pin MAPBGA package. Use Table 34 to find the information desired.

Table 34. Section Quick Reference

For Chip Package		See
144 pin QFP	Pin assignments	Table 35 on page 37
	Package drawings	Figure 15 on page 42 Figure 16 on page 43 Figure 17 on page 44
196 MAPBGA	Pin assignments	Table 36 on page 45
	Package drawings	Figure 18 on page 52 Figure 19 on page 53
	Ball map	Figure 20 on page 54

5.1 144 QFP Pin Assignments

The SCF5250 can be assembled in 144-pin QFP package. Table 35 provides the pin assignments for the package.

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
86	DDATA2/CTS0/GPIO3	I/O	Debug / UART0 CTS	Out / HIGH
87	DDATA3/RTS0/GPIO4	I/O	Debug / UART0 RTS	Out / HIGH
88	SCL1/TXD1/GPIO10	I/O	I2C1 clock line / second UART transmit data output	Out / LOW
89	CORE VDD	–	–	–
90	CORE GND	–	–	–
91	SDA1/RXD1/GPIO44	I/O	I2C1 data line / second UART receive data input	Hi-Z
92	PAD VDD	–	–	–
93	TXD0/GPIO45	I/O	First UART transmit data output	Out / HIGH
94	RXD0/GPIO46	I/O	First UART receive data input	In / LOW
95	PST3/INTMON1/ GPIO47	I/O	Debug / interrupt monitor output 1	Out / HIGH
96	PST2/INTMON2/GPIO48	I/O	Debug / interrupt monitor output 2	Out / HIGH
97	PAD GND	–	–	–
98	PST1/GPIO49	I/O	Debug	Out / HIGH
99	PST0/GPIO50	I/O	Debug	Out / HIGH
100	PSTCLK/GPIO51	I/O	Debug	Out / clock output
101	TDO/DSO	O	JTAG/debug	BDM
102	TDI/DSI	I	JTAG/debug	BDM
103	TCK	I	JTAG	BDM
104	TMS/BKPT	I	JTAG/debug	BDM
105	TRST/DSCLK	I	JTAG/Debug	BDM
106	RSTI	I	Reset	X
107	SCLK2/GPIO22	I/O	Audio interfaces serial clock 2	In / LOW
108	LRCK2/GPIO23	I/O	Audio interfaces EBU out 1	In /LOW
109	LINOUT	A	Linear regulator output	X
110	LININ	A	Linear regulator input	X
111	LINGND	–	Linear regulator ground	X
112	SDATAO2/GPIO34	I/O	Audio interfaces serial data output 2	Out / LOW
113	MCLK1/GPIO11	I/O	Audio master clock output 1	Out / clock output
114	HI-Z	I	JTAG	X
115	TEST2	I	Test	X

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS D AND E ARE DETERMINED AT THE SEATING PLANE, DATUM A.

DIM	MIN	MAX	DIM	MIN	MAX	DIM	MIN	MAX
A	–	1.6	L1	– 1 REF	–	–	–	–
A1	0.05	0.15	L2	– 0.5 REF	–	–	–	–
A2	1.35	1.45	R1	0.13	0.2	–	–	–
b	0.17	0.27	R2	0.13	–	–	–	–
b1	0.17	0.23	S	– 0.25 REF	–	–	–	–
c	0.09	0.20	θ	0°	7°	–	–	–
c1	0.09	0.16	θ1	0°	–	–	–	–
D	– 22 BSC	–	θ2	– 12° REF	–	–	–	–
D1	– 20 BSC	–	–	–	–	–	–	–
e	– 0.5 BSC	–	–	–	–	–	–	–
E	– 22 BSC	–	–	–	–	–	–	–
E1	– 20 BSC	–	–	–	–	–	–	–
L	0.45	0.75	–	–	–	–	–	–

TITLE:	CASE NUMBER: 918-03	
144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	STANDARD: MOTOROLA	
	PACKAGE CODE: 8259	SHEET: 3 OF 3

Figure 17. 144 QFP Package (3 of 3)

5.3 196 MAPBGA Pin Assignments

The SCF5250 can be assembled in a 196-pin MAPBGA package. Table 36 lists the 196 MAPBGA pin assignments.

Table 36. 196 MAPBGA Pin Assignments

MAPBGA Pin	Name	Type	Description	Pin State After Reset
B1	DATA16	I/O	Data	X
D3	A23_GPO54	I/O	SDRAM address / static adr	Out (requires pull up/down for boot-up selection
P_VDD	PST_VDD		PST_VDD	
C1	A22	O	SDRAM address / static adr	Out
D2	A21	O	SDRAM address / static adr	Out
E3	A20_A24	I/O	SDRAM address / static adr	Out (requires pull up/down for boot-up selection
D1	A19	O	SDRAM address / static adr	Out
E2	A18	O	SDRAM address / static adr	Out
P_GND	PST_GND		PST_GND	
F3	A17	O	SDRAM address / static adr	Out
E1	A16	O	SDRAM address / static adr	Out
F2	A15	O	SDRAM address / static adr	Out
F1	A14	O	SDRAM address / static adr	Out
G3	A13	O	SDRAM address / static adr	Out
P_VDD	PAD_VDD		PAD_VDD	
G2	A12	O	SDRAM address / static adr	Out
G1	A11	O	SDRAM address / static adr	Out
CORE_VDD	CORE_VDD		CORE_VDD	
C_GND	CORE_VSS		CORE_VSS	Out
H2	A10	O	SDRAM address / static adr	Out
J1	A9	O	SDRAM address / static adr	Out
H3	A8	O	SDRAM address / static adr	Out
K1	A7	O	SDRAM address / static adr	Out

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
G13	RXD1_GP46	I/O	UART1 receive data input	Out / Low
G12	PST3_INTMON1_GP47	I/O	Debug / interrupt monitor output 1	Out / High
F12	PST2_INTMON2_GP48	I/O	Debug / interrupt monitor output 2	Out / High
P_GND	PAD_GND	I/O	PAD_GND	
F14	PST1_GP49	I/O	Debug	Out / High
F13	PST0_GP50	I/O	Debug	Out / High
E14	PSTCLK_GP51	I/O	Debug	Out / clock output
E13	TDO_DSO	O	JTAG / Debug	BDM
D13	TDI_DSI	I	JTAG / Debug	BDM
E12	TCK	I	JTAG	BDM
C13	TMS_BKPT	I	JTAG / Debug	BDM
D12	TRST_DSCLK	I	JTAG / Debug	BDM
D14	RSTI	I	Reset	X
C14	SCLK2_GP22	I/O	Audio interfaces serial clock 2	In / Low
B14	LRCK2_GP23	I/O	Audio interfaces word clock 2	In / Low
C11	LINOUT	A	Linear regulator output	X
C11	LINOUT	A	Linear regulator output	X
B12	LININ	A	Linear regulator input	X
B12	LININ	A	Linear regulator input	X
P_GND	LIN_GND		Linear regulator ground	X
C10	SDATAO2_GP34	I/O	Audio interfaces serial data output 2	Out / Low
A12	MCLK1_GP11	I/O	Audio master clock output 1	Out / clock output
---	VBGT			
B11	HIZ_B	I	JTAG	X
B10	TEST2	I	Test	X
C9	TEST1	I	Test	X
A11	TEST0	I	Test	X

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
B9	SDWE_GP38	I/O	SDRAM write enable	Out / High
A10	SDCAS_GP39	I/O	SDRA CAS	Out / High
P_VDD	PAD_VDD		PAD_VDD	Out / High
C8	SDRAS_GP59	I/O	SDRAM RAS	Out / High
A9	SDCS0_GP60	I/O	SDRAM chip select out 0	Out / High
B8	SDLDQM_GPO52	O	SDRAM LDQM	Out / High
A8	SDUDQM_GPO53	O	SDRAM UDQM	Out / High
A7	BCLKE_GPO63	O	SDRAM clock enable output	Out / High
A6	BCLK_GP40	I/O	SDRAM clock output	Out / High
B7	DATA31	I/O	Data	X
A5	DATA30	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C7	DATA29	I/O	Data	X
B6	DATA28	I/O	Data	X
A4	DATA27	I/O	Data	X
B5	DATA26	I/O	Data	X
C6	DATA25	I/O	Data	X
P_VDD	PAD_VDD	I/O	PAD_VDD	
B4	DATA24	I/O	Data	X
B3	DATA23	I/O	Data	X
C5	DATA22	I/O	Data	X
A2	DATA21	I/O	Data	X
B2	DATA20	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C4	DATA19	I/O	Data	X
C3	DATA18	I/O	Data	X
C2	DATA17	I/O	Data	X

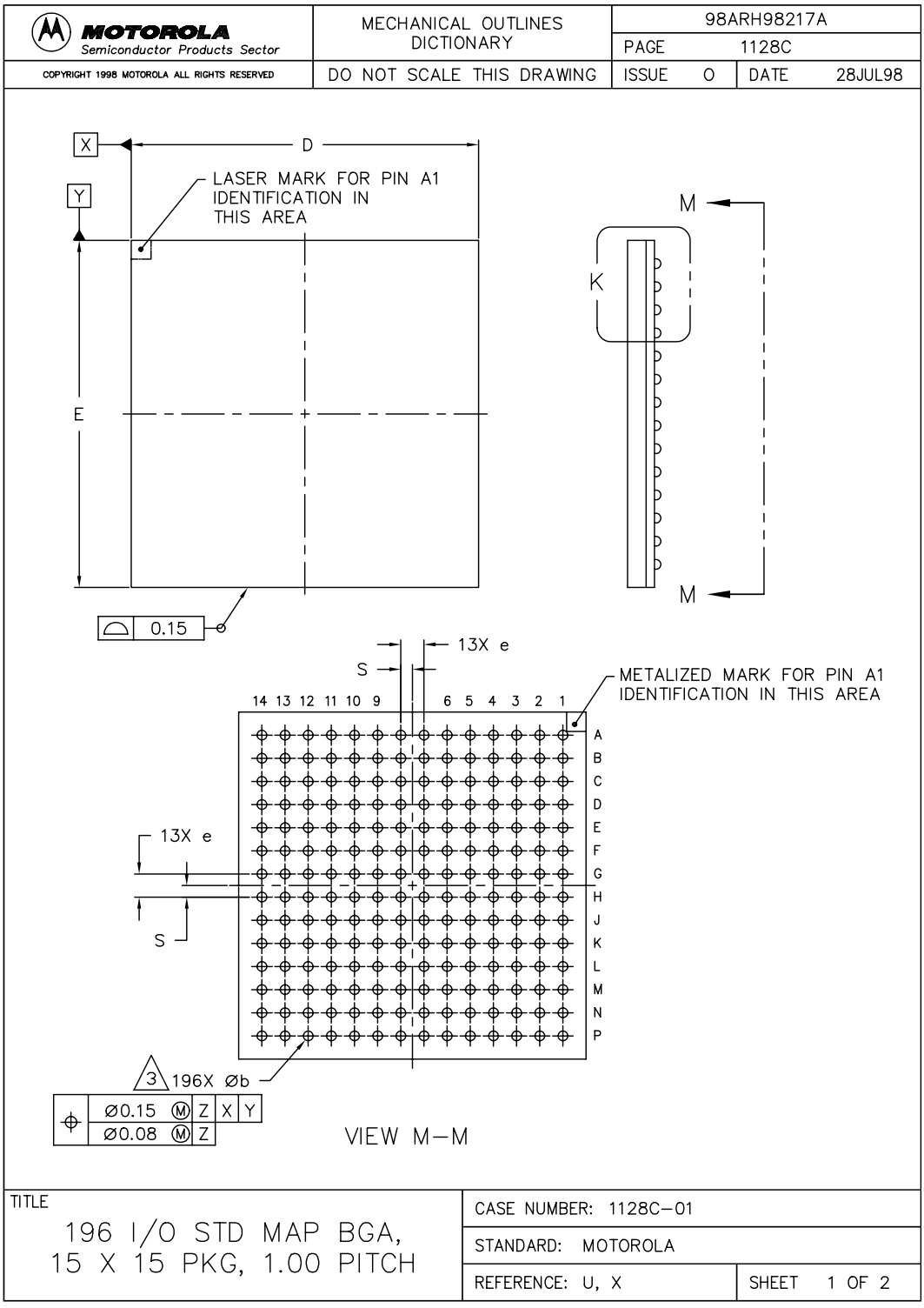

Figure 18. 196 MAPBGA Package (1 of 2)

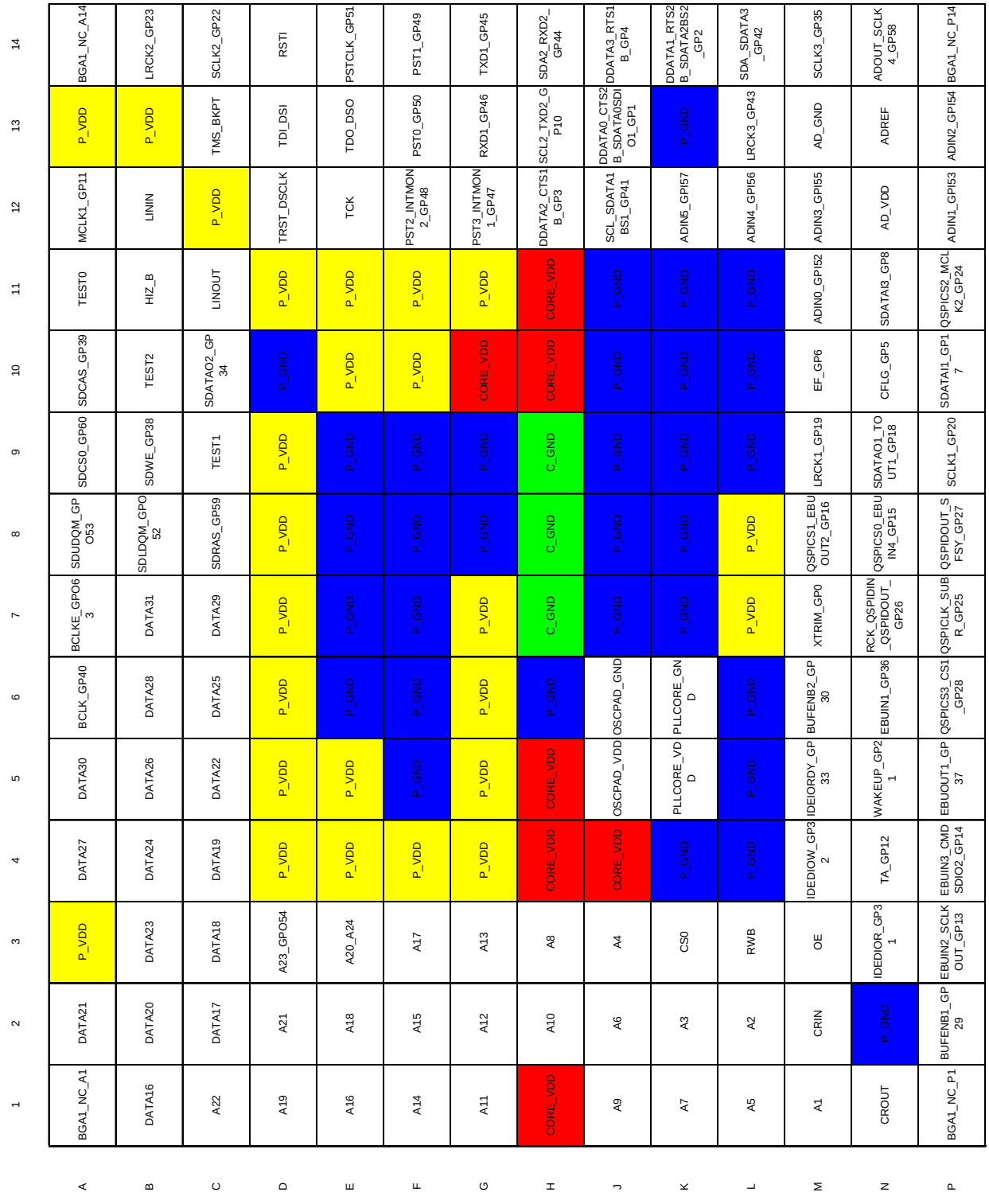

Figure 20. 196 MAPBGA Ball Map

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