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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	57
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/scf5250cag120r2

1.2.7 System Interface

The SCF5250 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SCF5250 also supports bursting ROMs.

1.2.8 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

1.2.9 Serial Audio Interfaces

The SC5250 digital audio interface provides three serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other two interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

1.2.10 IEC958 Digital Audio Interfaces

The SCF5250 has one digital audio input interface, and one digital audio output interface. The single output carries the consumer “c” channel.

1.2.11 Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

1.2.12 CD-ROM Encoder/Decoder

The SCF5250 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

1.2.16 IDE and SmartMedia Interfaces

The SCF5250 system bus allows connection of an IDE hard disk drive or SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5250.

Low cost version SCF5250LPV100 and SCF5250LAG100 does not run production test for the IDE/CF/SD/MMC interfaces. Freescale does not guarantee these interfaces will work on these two devices.

1.2.17 Analog/Digital Converter (ADC)

The six channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. Both the analogue comparator and digital sections of the ADC are provided internally. An external integrator circuit (resistor/capacitor) is required, which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

1.2.18 I^2C Module

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

1.2.19 Chip-Selects

Up to four programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

1.2.20 GPIO Interface

A total of 60 General Purpose inputs and 57 General Purpose outputs are available. These are multiplexed with various other signals. Seven of the GPIO inputs have edge sensitive interrupt capability.

1.2.21 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 7 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

1.2.22 JTAG

To help with system diagnostics and manufacturing testing, the SCF5250 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1A standard. Freescale provides BSDL files for JTAG testing.

1.2.23 System Debug Interface

The ColdFire processor core debug interface supports real-time instruction trace and debug, plus background-debug mode. A background-debug mode (BDM) interface provides system debug.

In real-time instruction trace, four status lines provide information on processor activity in real time (PST pins). A four-bit wide debug data bus (DDATA) displays operand data and change-of-flow addresses, which helps track the machine's dynamic execution path.

1.2.24 Crystal and On-Chip PLL

Typically, an external 16.92 MHz or 33.86 MHz clock input is used for CD R/W applications, while an 11.2896 MHz clock is more practical for Portable CD player applications. However, the on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5-35 MHz).

Two clock outputs (MCLK1 and MCLK2) are provided for use as Audio Master Clock. The output frequencies of both outputs are programmable to Fxtal, Fxtal/2, Fxtal/3, and Fxtal/4. The Fxtal/3 option is only available when the 33.86 MHz crystal is connected.

The SCF5250 supports VCO operation of the oscillator by means of a 16-bit pulse density modulation output. Using this mode, it is possible to lock the oscillator to the frequency of an incoming IEC958 or IIS signal. The maximum trim depends on the type and design of the oscillator. Typically a trim of +/- 100 ppm can be achieved with a crystal oscillator and over +/- 1000 ppm with an LC oscillator.

1.2.25 Boot ROM

The boot ROM on the SCF5250 serves to boot the CPU in designs which do not have external Flash memory or ROM. Typically this occurs in systems which have a separate MCU to control the system, and/or the SCF5250 is used as a stand-alone decoder.

The SCF5250 can be booted in one of three modes:

- External ROM
- Internal ROM Master mode – boots from I2C, SPI, or IDE
- Internal ROM Slave mode – boots from I2C or UART

1.2.26 Voltage Regulator

The SCF5250 contains an on-chip linear regulator that generates 1.2V from a 3.3V input. The regulator is self-contained and drives the 1.2V core voltage out on one pin that can be used to power the core supply

pins at the board level. In battery powered portable applications, it is recommended that an external dc-dc converter be used to generate the 1.2V core voltage to minimize power consumption.

2 SCF5250 Block Diagram

Figure 1 illustrates the functional block diagram of the SCF5250 processor.

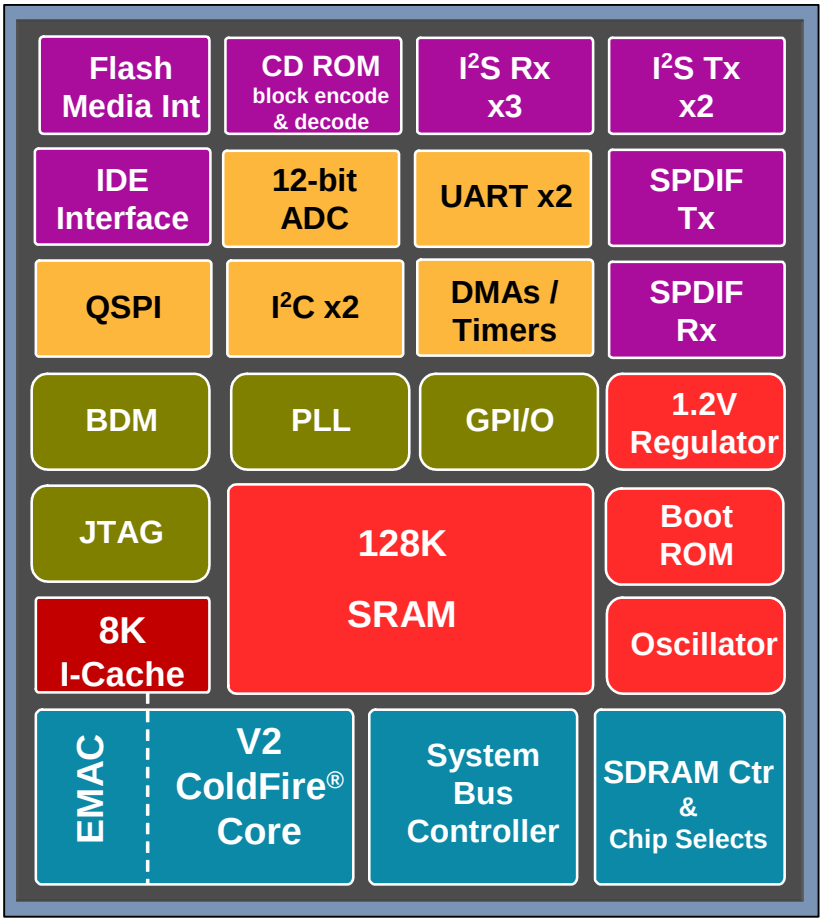

Figure 1. SCF5250 Block Diagram

3 Signal Descriptions

This section describes the SCF5250 processor's input and output signals. The signal descriptions shown in Table 2 are grouped according to relevant functionality.

Table 2. SCF5250 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[24:1] A[23]/GPO54	24 address lines, address line 23 multiplexed with GPO54 and address 24 is multiplexed with A20 (SDRAM access only).	Out	X
Read-write control	R/$\overline{W}$	Bus write enable - indicates if read or write cycle in progress	Out	H
Output enable	OE	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	$\overline{SDRAS}$/GPIO59	Row address strobe for external SDRAM.	Out	negated
Synchronous column address strobe	$\overline{SDCAS}$/GPIO39	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	$\overline{SDWE}$/GPIO38	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	$\overline{SDUDQM}$/GPO53	Indicates during write cycle if high byte is written	Out	–
SDRAM lower byte enable	$\overline{SDLDQM}$/GPO52	Indicates during write cycle if low byte is written	Out	–
SDRAM chip selects	$\overline{SD\_CS0}$/GPIO60	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE/GPIO63	SDRAM clock enable	Out	–
System clock	BCLK/GPIO40	SDRAM clock output	In/Out	–
ISA bus read strobe	$\overline{IDE\text{-}DIOR}$/GPIO31 (CS2)	There is 1 ISA bus read strobe and 1 ISA bus write strobe. They allow connection of one independent ISA bus peripherals, e.g. an IDE slave device.	In/Out	–
ISA bus write strobe	$\overline{IDE\text{-}DIOW}$/GPIO32 (CS2)		In/Out	–
ISA bus wait signal	$\overline{IDE\text{-}IORDY}$/GPIO33	ISA bus wait line - available for both busses	In/Out	–
Chip Selects[2:0]	$\overline{CS0}$/$\overline{CS4}$ $\overline{CS1}$/QSPI_CS3/GPIO28	Enables peripherals at programmed addresses. $\overline{CS}$[0] provides boot ROM selection	Out In/Out	negated
Buffer enable 1	$\overline{BUFENB1}$/GPIO29	Two programmable buffer enables allow seamless steering of external buffers to split data and address bus in sections.	In/Out	–
Buffer enable 2	$\overline{BUFENB2}$/GPIO30		In/Out	–
Transfer acknowledge	$\overline{TA}$/GPIO12	Transfer Acknowledge signal	In/Out	–
Wake Up	$\overline{WAKE\_UP}$/GPIO21	Wake-up signal input	In	–
Serial Clock Line	SCL0/SDATA1_BS1/GPIO41 SCL1/TXD1/GPIO10	Clock signal for Dual I^2C module operation	In/Out	–
Serial Data Line	SDA0/SDATA3/GPIO42 SDA1/RXD1/GPIO44	Serial data port for second I^2C module operation	In/Out	–
Receive Data	SDA1/RXD1/GPIO44 RXD0/GPIO46	Signal is receive serial data input for DUART	In	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45	Signal is transmit serial data output for DUART	Out	–
Request-To-Send	DDATA3/$\overline{\text{RTS0}}$/GPIO4 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	DUART signals a ready to receive data query	Out	–
Clear-To-Send	DDATA2/$\overline{\text{CTSO}}$/GPIO3 DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Signals to DUART that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capable of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLK_OUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPI_CS0/EBUIN4/GPIO15	audio interfaces IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPI_CS1/EBUOUT2/GPIO16	audio interfaces IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	audio interfaces serial data inputs	In	–
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	audio interfaces serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/GPIO43/AUDIO_CLOCK	audio interfaces serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	audio interfaces serial bit clocks	In/Out	–
Serial input	EF/GPIO6	error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPI_DIN/QSPI_DOUT/ GPIO26	audio interfaces subcode clock	In/Out	–
Subcode sync	QSPI_DOUT/SFSY/GPIO27	audio interfaces subcode sync	In/Out	–
Subcode data	QSPI_CLK/SUBR/GPIO25	audio interfaces subcode data	In/Out	–
Clock frequency trim	XTRIM/GPIO0	clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPI_CS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/GPIO43/AUDIO_CLOCK	Optional Audio clock Input	–	–

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Memory Stick/ Secure Digital interface	EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command lane Memory Stick interface 2 data I/O	In/Out	–
	EBUIN2/SCLK_OUT/GPIO13	Clock out for both Memory Stick interfaces and for Secure Digital	In/Out	–
	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Secure Digital serial data bit 0 Memory Stick interface 1 data I/O	In/Out	–
	SCL0/SDATA1_BS1/GPIO41	Secure Digital serial data bit 1 Memory Stick interface 1 strobe	In/Out	–
	DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	Secure Digital serial data bit 2 Memory Stick interface 2 strobe Reset output signal	In/Out	–
	SDA0/SDATA3/GPIO42	Secure Digital serial data bit 3	In/Out	–
ADC IN	ADIN0/GPI52 ADIN1/GPI53 ADIN2/GPI54 ADIN3/GPI55 ADIN4/GPI56 ADIN5/GPI57	Analog to Digital converter input signals	In	–
ADC OUT	ADREF ADOUT/SCLK4/GPIO58	Analog to digital convertor output signal. Connect to ADREF via integrator network.	In/Out	–
QSPI clock	QSPI_CLK/SUBR/GPIO25	QSPI clock signal	In/Out	–
QSPI data in	RCK/QSPI_DIN/QSPI_DOUT/GPIO26	QSPI data input	In/Out	–
QSPI data out	RCK/QSPI_DIN/QSPI_DOUT/GPIO26 QSPI_DOUT/SFSY/GPIO27	QSPI data out	In/Out	–
QSPI chip selects	QSPI_CS0/EBUIN4/GPIO15 QSPI_CS1/EBUOUT2/GPIO16 QSPI_CS2/MCLK2/GPIO24 $\overline{\text{CS1}}$/QSPI_CS3/GPIO28	QSPI chip selects	In/Out	–
Crystal in	CRIN	Crystal input	In	–
Crystal out	CROUT	Crystal Out	Out	–
Reset In	RSTI	Processor Reset Input	In	–
Freescale Test Mode	TEST[2:0]	TEST pins.	In	–
Linear regulator output	LINOUT	outputs 1.2 V to supply core	Out	–
Linear regulator input	LININ	Input, typically I/O supply (3.3V)	In	–
Linear regulator ground	LINGND	–	–	–
High Impedance	HI-Z	Assertion Tri-states all output signal pins.	In	–
Debug Data	DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2 DDATA2/$\overline{\text{CTS0}}$/GPIO3 DDATA3/$\overline{\text{RTS0}}$/GPIO4	Displays captured processor data and break-point status.	In/Out	Hi-Z

3.12 Subcode Interface

There is a 3-line subcode interface on the SCF5250 processor. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 9.

Table 9. Subcode Interface Signal

Signal name	Description
RCK/QSPI_DIN/QSPI_DOUT/GPIO26	Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder.
QSPI_DOUT/SFSY/GPIO27	Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream.
QSPI_CLK/SUBR/GPIO25	Subcode data output This signal is a subcode data out pin.

3.13 Analog to Digital Converter (ADC)

The ADOUT signal on the ADOUT/SCLK4/GPIO58 pin provides the reference voltage in PWM format. This output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be input to the ADREF pin.

The six AD inputs are each fed to their own comparator. The reference input to each (ADREF) is then multiplexed as only one AD comparison can be made at any one time.

NOTE

To use the ADINx as General Purpose inputs (rather than there analogue function) it is necessary to generate a fixed comparator voltage level of VDD/2. This can be accomplished by a potential divider network connected to the ADREF pin. However in portable applications where stand-by power consumption is important the current taken by the divider network (in stand-by mode) could be excessive. Therefore it is possible to generate a VDD/2 voltage by selecting SCLK4 output mode and feeding this clock signal (which is 50% duty cycle) through an external integration circuit. This would generate a voltage level equal to VDD/2 but would be disabled when stand-by mode was selected.

3.14 Secure Digital/Memory Stick Card Interface

The device has a versatile flash card interface that supports both Secure Digital and Memory Stick cards. The interface can either support one Secure Digital or two Memory Stick cards. No mixing of card types is possible. Table 10 gives the pin descriptions.

Table 10. Flash Memory Card Signals

Flash Memory Signal	Description
EBUIN2/SCLKOUT/GPIO13	Clock out for both Memory Stick interfaces and for Secure Digital
EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command line Memory Stick interface 2 data I/O

Table 12. Processor Status Signal Encodings

PST[3:0]		Definition
(HEX)	(BINARY)	
$0	0000	Continue execution
$1	0001	Begin execution of an instruction
$2	0010	Reserved
$3	0011	Entry into user-mode
$4	0100	Begin execution of PULSE and WDDATA instructions
$5	0101	Begin execution of taken branch or Synch_PC[1]
$6	0110	Reserved
$7	0111	Begin execution of RTE instruction
$8	1000	Begin 1-byte data transfer on DDATA
$9	1001	Begin 2-byte data transfer on DDATA
$A	1010	Begin 3-byte data transfer on DDATA
$B	1011	Begin 4-byte data transfer on DDATA
$C	1100	Exception processing[2]
$D	1101	Emulator mode entry exception processing[2]
$E	1110	Processor is stopped, waiting for interrupt[2]
$F	1111	Processor is halted[2]

1 Rev. B enhancement.

2 These encodings are asserted for multiple cycles.

3.19 BDM/JTAG Signals

The SCF5250 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

3.20 Clock and Reset Signals

The clock and reset signals configure the SCF5250 processor and provide interface signals to the external system.

3.20.1 Reset In

Asserting $\overline{\text{RSTI}}$ causes the SCF5250SCF5250 to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the data bus is tri-stated.

Figure 3 and Figure 4 provide the input and output AC timing definition diagrams and Table 21 and Table 22 provide the input and output AC timing parameters.

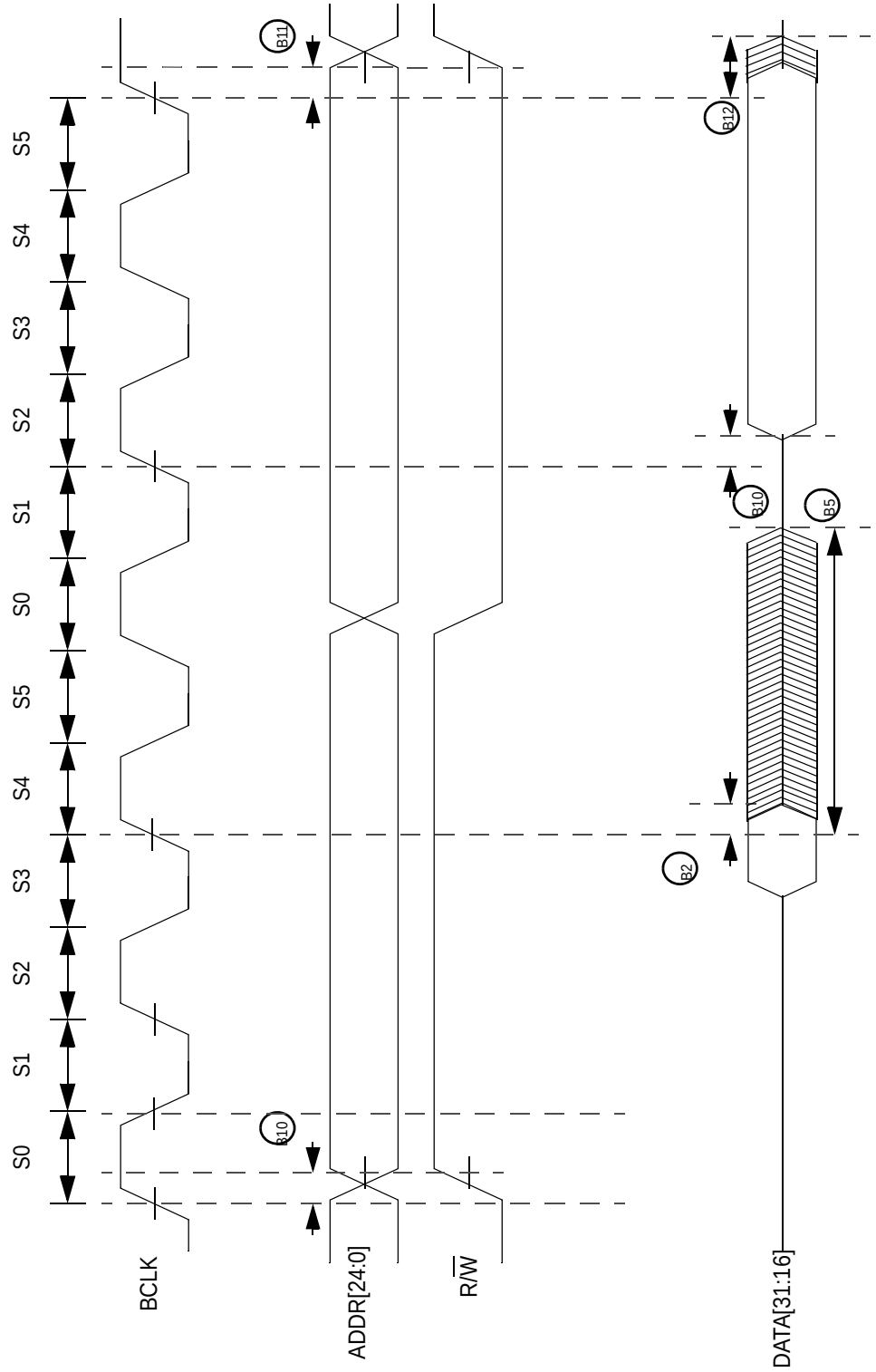

Figure 3. Input/Output Timing Definition-I

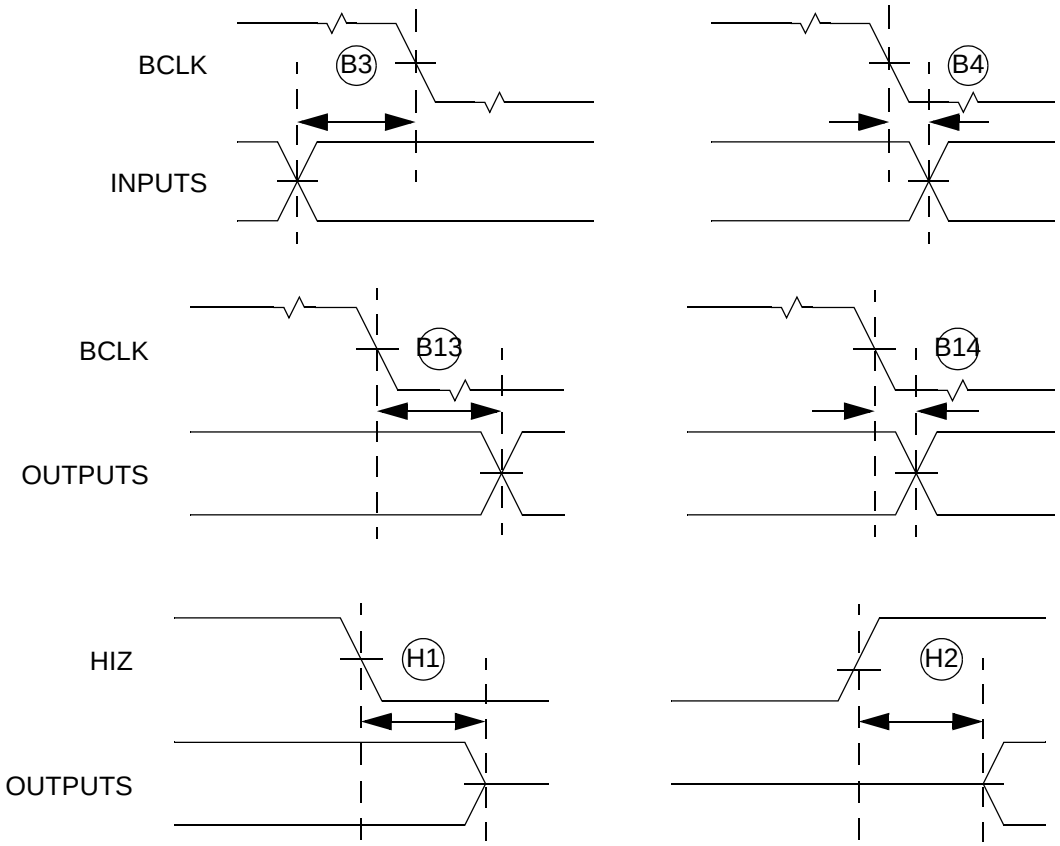

Figure 4. Input/Output AC Timing Definition-III

Table 21. Input AC Timing Specification

Num	Characteristic	Min	Max	Units
B1[1,2]	Signal Valid to BCLK Rising (setup)	3	–	ns
B2[1]	BCLK Rising to signal Invalid (hold)	2	–	ns
B3[1]	BCLK to Input High Impedance	–	5	BCLK cycle

1 Inputs (rising): DATA[31:16]

2 AC timing specs assume 40pF load capacitance on BCLK and 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

Table 22. Output AC Timing Specification

Num	Characteristic[1]	Min	Max	Units
B10[2]	BCLK (8mA) Rising to signal Valid	–	10	ns
B11[2]	BCLK (8mA) Rising to signal Invalid (hold)	3.5	–	ns
B10[3]	BCLK (4mA) Rising to signal Valid	–	11	ns
B11[3]	BCLK (4mA) Rising to signal Invalid (hold)	4	–	ns
B12[4]	BCLK to High Impedance (Three-State)	–	14	ns

Table 22. Output AC Timing Specification (continued)

Num	Characteristic[1]	Min	Max	Units
H1	$\overline{HIZ}$ to High Impedance	–	tbd	ns
H2	$\overline{HIZ}$ to Low Impedance	–	tbd	ns

1 AC timing specs assume 40pF load capacitance on BCLK and a 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 Outputs (8mA): DATA[31:16], ADDR[25,23:9]

3 Outputs (4mA): SDRAS, SDCAS, SDWE, SD_CS0, SDUDQM, SDLDQM, BCLKE

4 High Impedance (Three-State): DATA[31:16]

Figure 5 and Table 23 provide the timing diagram and timing parameters for the Debug AC.

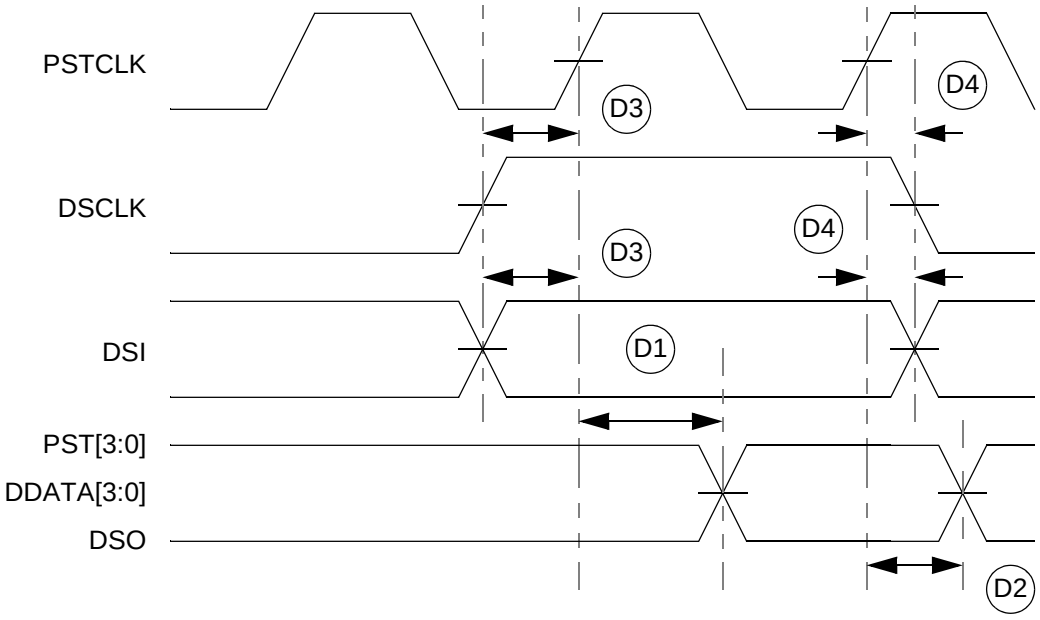

Figure 5. Debug AC Timing Definition Diagram

Table 23. Debug AC Timing Specification[1]

Num	Characteristic	Min	Max	Units
D1	PSTCLK to signal Valid (Output valid)	–	6	ns
D2	PSTCLK to signal Invalid (Output hold)	1.8	–	ns
D3[2]	Signal Valid to PSTCLK (Input setup)	3	–	ns
D4	PSTCLK to signal Invalid (Input hold)	5	–	ns

1 AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.

Figure 6 and Table 24 provide the timing diagram and timing parameters for the Timer module.

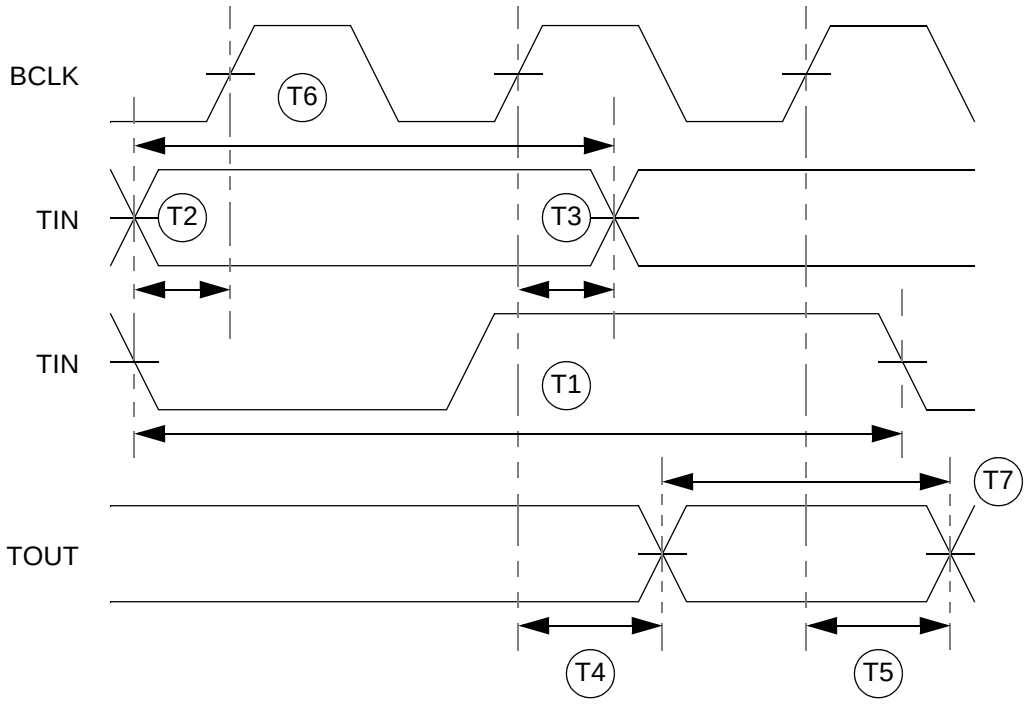

Figure 6. Timer Module AC Timing Definition Diagram

Table 24. Timer Module AC Timing Specification

Num	Characteristic	Min	Max	Units
T1	TIN Cycle time	3T	–	bus clocks
T2	TIN Valid to BCLK (input setup)	6	–	ns
T3	BCLK to TIN Invalid (input hold)	0	–	ns
T4	BCLK to TOUT Valid (output valid)	–	10	ns
T5	BCLK to TOUT Invalid (output hold)	tbd	–	ns
T6	TIN Pulse Width	1T	–	bus clocks
T7	TOUT Pulse Width	1T	–	bus clocks

Figure 11 provides the IEEE 1149.1 JTAG timing diagram and Table 30 provides the timing parameters.

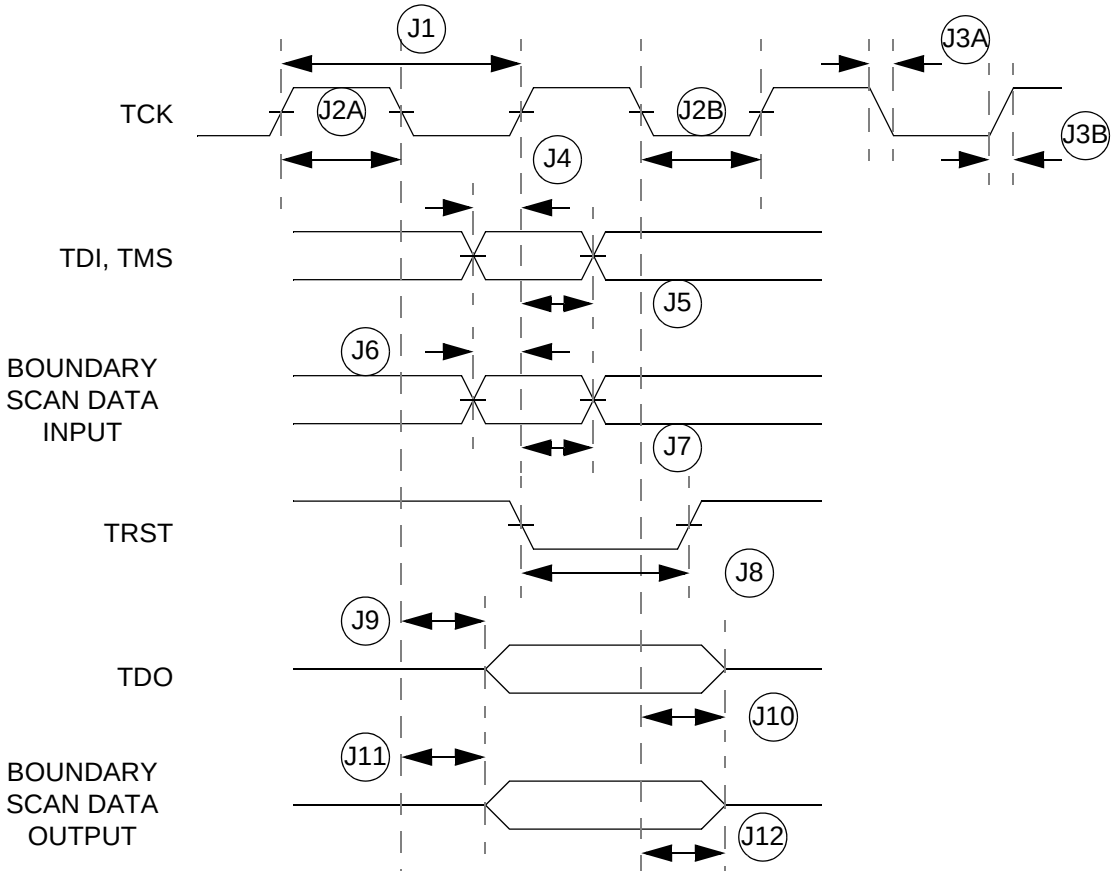

Figure 11. JTAG AC Timing Diagram

Table 30. JTAG AC Timing Specifications

Num	Characteristic	Min	Max	Units
–	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	–	ns
J2a	TCK Clock Pulse High Width	25	–	ns
J2b	TCK Clock Pulse Low Width	25	–	ns
J3a	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	–	5	ns
J3b	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	–	5	ns
J4	TDI, TMS to TCK rising (Input Setup)	8	–	ns
J5	TCK rising to TDI, TMS Invalid (Hold)	10	–	ns
J6	Boundary Scan Data Valid to TCK (Setup)	tbd	–	ns
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	tbd	–	ns
J8	$\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges)	12	–	ns
J9	TCK falling to TDO Valid (signal from driven or three-state)	–	15	ns
J10	TCK falling to TDO High Impedance	–	15	ns

Table 30. JTAG AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Units
J11	TCK falling to Boundary Scan Data Valid (signal from driven or three-state)	–	tbd	ns
J12	TCK falling to Boundary Scan. Data High Impedance	–	tbd	ns

Figure 12 provides the SCLK input, SDATA output timing diagram for the IIS module and Table 31 provides the timing parameters.

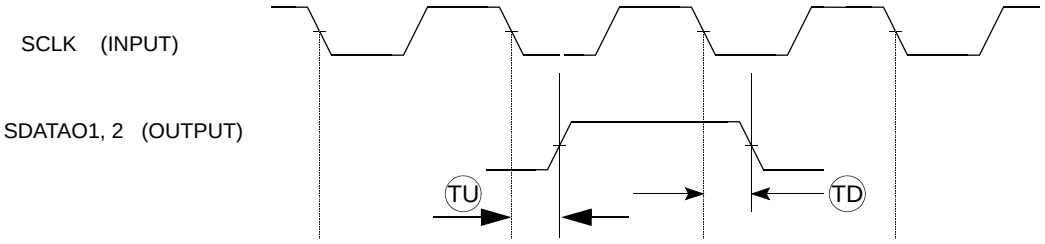

Figure 12. SCLK Input, SDATA Output Timing Diagram

Table 31. SCLK Input, SDATA Output Timing Specifications

Num	Characteristic	Min	Max	Units
TU	SCLK fall to SDATAO rise	–	25	ns
TD	SCLK fall to SDATAO fall	–	25	ns

Figure 13 provides the SCLK output, SDATA output timing diagram for the IIS module and Table 32 provides the timing parameters.

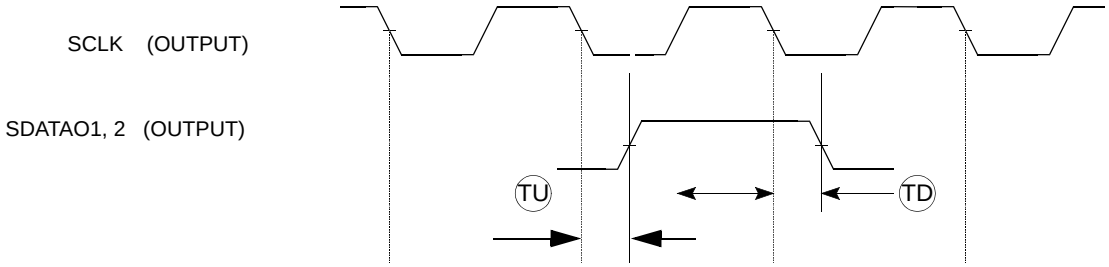

Figure 13. SCLK Output, SDATA Output Timing Diagram

Table 32. SCLK Output, SDATA Output Timing Specifications

Num	Characteristic	Min	Max	Units
TU	SCLK fall to SDATAO rise	–	3	ns
TD	SCLK fall to SDATAO fall	–	3	ns

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
86	DDATA2/CTS0/GPIO3	I/O	Debug / UART0 CTS	Out / HIGH
87	DDATA3/RTS0/GPIO4	I/O	Debug / UART0 RTS	Out / HIGH
88	SCL1/TXD1/GPIO10	I/O	I2C1 clock line / second UART transmit data output	Out / LOW
89	CORE VDD	–	–	–
90	CORE GND	–	–	–
91	SDA1/RXD1/GPIO44	I/O	I2C1 data line / second UART receive data input	Hi-Z
92	PAD VDD	–	–	–
93	TXD0/GPIO45	I/O	First UART transmit data output	Out / HIGH
94	RXD0/GPIO46	I/O	First UART receive data input	In / LOW
95	PST3/INTMON1/ GPIO47	I/O	Debug / interrupt monitor output 1	Out / HIGH
96	PST2/INTMON2/GPIO48	I/O	Debug / interrupt monitor output 2	Out / HIGH
97	PAD GND	–	–	–
98	PST1/GPIO49	I/O	Debug	Out / HIGH
99	PST0/GPIO50	I/O	Debug	Out / HIGH
100	PSTCLK/GPIO51	I/O	Debug	Out / clock output
101	TDO/DSO	O	JTAG/debug	BDM
102	TDI/DSI	I	JTAG/debug	BDM
103	TCK	I	JTAG	BDM
104	TMS/BKPT	I	JTAG/debug	BDM
105	TRST/DSCLK	I	JTAG/Debug	BDM
106	RSTI	I	Reset	X
107	SCLK2/GPIO22	I/O	Audio interfaces serial clock 2	In / LOW
108	LRCK2/GPIO23	I/O	Audio interfaces EBU out 1	In /LOW
109	LINOUT	A	Linear regulator output	X
110	LININ	A	Linear regulator input	X
111	LINGND	–	Linear regulator ground	X
112	SDATAO2/GPIO34	I/O	Audio interfaces serial data output 2	Out / LOW
113	MCLK1/GPIO11	I/O	Audio master clock output 1	Out / clock output
114	HI-Z	I	JTAG	X
115	TEST2	I	Test	X

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
J2	A6	O	SDRAM address / static adr	Out
L1	A5	O	SDRAM address / static adr	Out
P_GND	PAD_GND		PAD_GND	
J3	A4	O	SDRAM address / static adr	Out
K2	A3	O	SDRAM address / static adr	Out
L2	A2	O	SDRAM address / static adr	Out
M1	A1	O	SDRAM address / static adr	Out
K3	CS0	O	Static chip select 0	Out
L3	RWB	O	Bus write enable	Out
J5	OSCPAD_VDD		OSCPAD_VDD	
M2	CRIN		Crystal / external clock input	X
N1	CROUT		Crystal clock output	X
J6	OSCPAD_GND		OSCPAD_GND	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
M3	OE	O	Output enable	Out
M4	IDEDIOW_GP32	I/O	IDE DIOW	Out / High
M5	IDEIORDY_GP33	I/O	IDE interface IORDY	Out / Low
N3	IDEDIOR_GP31	I/O	IDE interface DIOR	Out / High
M6	BUFENB2_GP30	I/O	External Buffer 2 enable	Out / High
P2	BUFENB1_GP29	I/O	External Buffer 1 enable	Out / High
N4	TA_GP12	I/O	Transfer acknowledge	In (requires pull-up for normal operation)

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
B9	SDWE_GP38	I/O	SDRAM write enable	Out / High
A10	SDCAS_GP39	I/O	SDRA CAS	Out / High
P_VDD	PAD_VDD		PAD_VDD	Out / High
C8	SDRAS_GP59	I/O	SDRAM RAS	Out / High
A9	SDCS0_GP60	I/O	SDRAM chip select out 0	Out / High
B8	SDLDQM_GPO52	O	SDRAM LDQM	Out / High
A8	SDUDQM_GPO53	O	SDRAM UDQM	Out / High
A7	BCLKE_GPO63	O	SDRAM clock enable output	Out / High
A6	BCLK_GP40	I/O	SDRAM clock output	Out / High
B7	DATA31	I/O	Data	X
A5	DATA30	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C7	DATA29	I/O	Data	X
B6	DATA28	I/O	Data	X
A4	DATA27	I/O	Data	X
B5	DATA26	I/O	Data	X
C6	DATA25	I/O	Data	X
P_VDD	PAD_VDD	I/O	PAD_VDD	
B4	DATA24	I/O	Data	X
B3	DATA23	I/O	Data	X
C5	DATA22	I/O	Data	X
A2	DATA21	I/O	Data	X
B2	DATA20	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C4	DATA19	I/O	Data	X
C3	DATA18	I/O	Data	X
C2	DATA17	I/O	Data	X

6 Product Documentation

This section contains this document's revision history and the reference documents that are available to provide more information about the SCF5250 processor.

6.1 Reference Documents

The following list contains the documents that provide a complete description of the SCF5250 and are required to design properly with the part. The documents are available at: http://www.freescale.com.

ColdFire Family Programmer's Reference Manual (order number CFPRM)

Version 2/2M ColdFire Core Processor User's Manual (order number ColdFire2UM)

Version 2/2M ColdFire Core Processor User's Manual Addendum (order number ColdFire2UMAD)

SCF5250 User's Manual (order number SCF5250UM)

6.2 Revision History

Table 37 list the revision history for this data sheet.

Table 37. Revision History

Revision	Description
1.3	Added 144 LQFP package drawings. Added 196 MAPBGA package drawings, pin assignments, and ball map.
1.2	Added SCF5250DAG120 and SCF5250EAG120 parts in Table 1. Content has been reorganized, however there are no other content removal or additions.

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