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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	57
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=scf5250lag100

integrated peripherals and enhanced MAC unit allow the SCF5250 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

1.1 Orderable Part Numbers

Table 1 lists the orderable part numbers for the SCF5250 processor.

Table 1. Orderable Part Numbers

Orderable Part Number	Maximum Clock Frequency	Package Type	Operating Temperature Range	Part Status
SCF5250LPV100	100 MHz	144 pin QFP	-20°C to 70°C	Leaded
SCF5250LAG100	100 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250PV120	120 MHz	144 pin QFP	-20°C to 70°C	Leaded
SCF5250AG120	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250DAG120[1]	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250EAG120[2]	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250CPV120	120 MHz	144 pin QFP	-40°C to 85°C	Leaded
SCF5250CAG120	120 MHz	144 pin QFP	-40°C to 85°C	Lead Free
SCF5250VM120	120 MHz	196 ball MAPBGA	-20°C to 70°C	Lead Free

1 SCF5250DAG120—This device has the same feature set, pin assignment and specification as SCF5250AG120 with the addition of including the cost of the MP3 decoder royalty to be paid to Thomson Licensing S.A. for use of the MP3 patent rights described at http://mp3licensing.com/patents/index.html.

2 SCF5250EAG120—This device has the same feature set, pin assignment and specification as SCF5250AG120 with the addition of including the cost of the MP3 encoder and decoder royalty to be paid to Thomson Licensing S.A. for use of the MP3 patent rights described at http://mp3licensing.com/patents/index.html.

1.2 SCF5250 Features

This section provides brief descriptions of the features of the SCF5250 processor.

1.2.1 ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

1.2.2 DMA Controller

The SCF5250 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

1.2.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

1.2.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5250 processor uses a 8K-byte, direct-mapped instruction cache to achieve 107 MIPS at 120 MHz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

1.2.5 Internal 128-KByte SRAM

The 128-KByte on-chip SRAM is available in two banks, SRAM0 (64K) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in SRAM1 can be accessed under DMA.

1.2.6 SDRAM Controller

The SCF5250 SDRAM controller provides a glueless interface for one bank of SDRAM up to 32 MB (256 Mbits). The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

The CD-ROM decoder performs following functions in hardware:

- Sector sync recognition
- Descrambling of sectors
- Verification of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors
- Third-layer error correction is not performed

The CD-ROM encoder performs following functions in hardware:

- Sector sync recognition
- Scrambling of sectors
- Insertion of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors.
- Third-layer error encoding needs to be done in software. This can use approximately 5–10 MHz of performance for single-speed.

1.2.13 Dual UART Module

Two full-duplex UARTs with independent receive and transmit buffers are in this module. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The Dual UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function from a programmable prescaler. You can select full duplex, auto-echo loopback, local loopback, and remote loopback modes. The programmable Dual UARTs can interrupt the CPU on various normal or error-condition events.

1.2.14 Queued Serial Peripheral Interface QSPI

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfers of up to 15 Mbits/second are possible at a CPU clock of 120 MHz. The QSPI supports master mode operation only.

1.2.15 Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer. Timer0 has an external pin TOUT0, which can be used in Output Compare mode. This mode triggers an external signal or interrupts the CPU when the timer reaches a set value, and can also generate waveforms on TOUT0.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the ÷1 and ÷16 clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

3.2.2 Read-Write Control

This signal indicates during any bus cycle whether a read or write is in progress. A low is write cycle and a high is a read cycle.

3.2.3 Output Enable

The $\overline{OE}$ signal is intended to be connected to the output enable of asynchronous memories connected to chip selects. During bus read cycles, the ColdFire processor will drive $\overline{OE}$ low.

3.2.4 Data Bus

The data bus (D[31:16]) is bi-directional and non-multiplexed. Data is registered by the SCF5250 on the rising clock edge. The data bus uses a default configuration if none of the chip-selects or DRAM bank match the address decode. All 16 bits of the data bus are driven during writes, regardless of port width or operand size.

3.2.5 Transfer Acknowledge

The $\overline{TA}$/GPIO12 pin is the transfer acknowledge signal.

3.3 SDRAM Controller Signals

The following SDRAM signals provide a glueless interface to external SDRAM. An SDRAM width of 16 bits is supported and can access as much as 32MB of memory. ADRAMs are not supported.

Table 3. SDRAM Controller Signals

SDRAM Signal	Description
Synchronous DRAM row address strobe	The $\overline{SDRAS}$/GPIO59 active low pin provides a seamless interface to the RAS input on synchronous DRAM
Synchronous DRAM Column Address Strobe	The $\overline{SDCAS}$/GPIO39 active low pin provides a seamless interface to CAS input on synchronous DRAM.
Synchronous DRAM Write	The $\overline{SDWE}$/GPIO38 active-low pin is asserted to signify that a SDRAM write cycle is underway. This pin outputs logic ‘1’ during read bus cycles.
Synchronous DRAM Chip Enable	The $\overline{SD\_CS0}$/GPIO60 active-low output signal is used during synchronous mode to route directly to the chip select of a SDRAM device.
Synchronous DRAM UDQM and LQDM signals	The DRAM byte enables UDMQ and LDQM are driven by the SDUDQM/GPO53 and SDLDQM/GPO52 byte enable outputs.
Synchronous DRAM clock	The DRAM clock is driven by the BCLK/GPIO40 signal
Synchronous DRAM Clock Enable	The BCLKE active high output signal is used during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM.

3.4 Chip Selects

There are three chip select outputs on the SCF5250 device. $\overline{CS0}$/$\overline{CS4}$ and $\overline{CS1}$/QSPI_CS3/GPIO28 and CS2 which is associated with the IDE interface read and write strobes - IDE-DIOR and IDE-DIOW.

CS0 and CS4 are multiplexed. The SCF5250 has the option to boot from an internal Boot ROM. The function of the CS0/CS4 pin is determined by the boot mode. When the device is booted from internal ROM, the internal ROM is accessed with CS0 (required for boot) and the CS0/CS4 pin is driven by CS4. When the device is booted from external ROM / Flash, the CS0/CS4 pin is driven by CS0 and the internal ROM is disabled.

The active low chip selects can be used to access asynchronous memories. The interface is glueless.

3.5 ISA Bus

The SCF5250 supports an ISA bus. Using the ISA bus protocol, reads and writes for one ISA bus peripheral is possible. $\overline{IDE\text{-}DIOR}$/GPIO31 and $\overline{IDE\text{-}DIOW}$/GPIO32 are the read and write strobe. The peripheral can insert wait states by pulling IDE-IORDY/GPIO33.

CS2 is associated with the IDE-DIOR and IDE-DIOW.

3.6 Bus Buffer Signals

As the SCF5250 has a complicated slave bus, which allows SDRAM, asynchronous memories, and ISA peripherals on the bus, it may become necessary to introduce a buffer on the bus in certain applications. The SCF5250 has a glueless interface to steer these bus buffers with two bus buffer output signals $\overline{BUFENB1}$/GPIO29 and $\overline{BUFENB2}$/GPIO30.

3.7 I^2C Module Signals

There are two I^2C interfaces on this device as described in Table 4.

The I^2C module acts as a two-wire, bidirectional serial interface between the SCF5250 processor and peripherals with an I^2C interface (e.g., LED controller, A-to-D converter, D-to-A converter). When devices connected to the I^2C bus drive the bus, they will either drive logic-0 or high-impedance. This can be accomplished with an open-drain output.

Table 4. I^2C Module Signals

I^2c Module Signal	Description
I^2C Serial Clock	The SCL0/SDATA1_BS1/GPIO41 and SCL1/TXD1/GPIO10 bidirectional signals are the clock signal for first and second I^2C module operation. The I^2C module controls this signal when the bus is in master mode; all I^2C devices drive this signal to synchronize I^2C timing. Signals are multiplexed
I^2C Serial Data	The SDA0/SDATA3/GPIO42 and SDA1/RXD1/GPIO44 bidirectional signals are the data input/output for the first and second serial I^2C interface. Signals are multiplexed

3.8 Serial Module Signals

The signals described in Table 5 transfer serial data between the two UART modules and the external peripherals.

Table 5. Serial Module Signals

Serial Module Signal	Description
Receive Data	The RXD0/GPIO46 and SDA1/RXD1/GPIO44 are the inputs on which serial data is received by the DUART. Data is sampled on RxD[1:0] on the rising edge of the serial clock source, with the least significant bit received first.
Transmit Data	The DUART transmits serial data on the TXD0/GPIO45 and SCL1/TXD1/GPIO10 output signals. Data is transmitted on the falling edge of the serial clock source, with the least significant bit transmitted (LSB) first. When no data is being transmitted or the transmitter is disabled, these two signals are held high. TxD[1:0] are also held high in local loopback mode.
Request To Send	The DDATA3/RTS0/GP104 and DDATA1/RTS1/SDATA2_BS2/GPIO2 request-to-send outputs indicate to the peripheral device that the DUART is ready to send data and requires a clear-to-send signal to initiate transfer.
Clear To Send	Peripherals drive the DDATA2/CTS0/GPIO3 and DDATA0/CTS1/SDATA0_SDIO1/GPIO1 inputs to indicate to the SCF5250 serial module that it can begin data transmission.

3.9 Timer Module Signals

Table 6 describes the Timer module signal which provides an external interface to Timer0.

Table 6. Timer Module Signals

Serial Module Signal	Description
Timer Output	The SDATAO1/TOUT0/GPIO18 programmable output pulse or toggle on various timer events.

3.12 Subcode Interface

There is a 3-line subcode interface on the SCF5250 processor. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 9.

Table 9. Subcode Interface Signal

Signal name	Description
RCK/QSPI_DIN/QSPI_DOUT/GPIO26	Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder.
QSPI_DOUT/SFSY/GPIO27	Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream.
QSPI_CLK/SUBR/GPIO25	Subcode data output This signal is a subcode data out pin.

3.13 Analog to Digital Converter (ADC)

The ADOUT signal on the ADOUT/SCLK4/GPIO58 pin provides the reference voltage in PWM format. This output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be input to the ADREF pin.

The six AD inputs are each fed to their own comparator. The reference input to each (ADREF) is then multiplexed as only one AD comparison can be made at any one time.

NOTE

To use the ADINx as General Purpose inputs (rather than there analogue function) it is necessary to generate a fixed comparator voltage level of VDD/2. This can be accomplished by a potential divider network connected to the ADREF pin. However in portable applications where stand-by power consumption is important the current taken by the divider network (in stand-by mode) could be excessive. Therefore it is possible to generate a VDD/2 voltage by selecting SCLK4 output mode and feeding this clock signal (which is 50% duty cycle) through an external integration circuit. This would generate a voltage level equal to VDD/2 but would be disabled when stand-by mode was selected.

3.14 Secure Digital/Memory Stick Card Interface

The device has a versatile flash card interface that supports both Secure Digital and Memory Stick cards. The interface can either support one Secure Digital or two Memory Stick cards. No mixing of card types is possible. Table 10 gives the pin descriptions.

Table 10. Flash Memory Card Signals

Flash Memory Signal	Description
EBUIN2/SCLKOUT/GPIO13	Clock out for both Memory Stick interfaces and for Secure Digital
EBUIN3/CMD_SDIO2/GPIO14	Secure Digital command line Memory Stick interface 2 data I/O

Table 10. Flash Memory Card Signals (continued)

Flash Memory Signal	Description
DDATAO/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Secure Digital serial data bit 0 Memory Stick interface 1 data I/O
SCL0/SDATA1_BS1/GPIO41	Secure Digital serial data bit 1 Memory Stick interface 1 strobe
DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	Secure Digital serial data bit 2 Memory Stick interface 2 strobe Reset output signal Selection between Reset function and SDATA2_BS2 is done by programming PLLCR register.
SDA0/SDATA3/GPIO42	Secure Digital serial data bit 3

3.15 Queued Serial Peripheral Interface (QSPI)

The QSPI interface is a high-speed serial interface allowing transmit and receive of serial data. Pin descriptions are given in Table 11.

Table 11. Queued Serial Peripheral Interface (QSPI) Signals

Serial Module Signal	Description
QSPICLK/SUBR/GPIO25	Multiplexed signal IIC interface clock or QSPI clock output Function select is done via PLLCR register.
RCK/QSPIDIN/QSPI_DOUT/GPIO26	Multiplexed signal IIC interface data or QSPI data input. Function select is done via PLLCR register.
RCK/QSPI_DIN/QSPI_DOUT/GPIO26 QSPI_DOUT/SFSY/GPIO27	QSPI data output.
QSPICS0/EBUIN4GPIO15	4 different QSPI chip selects.
QSPICS1/EBUOUT2/GPIO16	
QSPICS2/MCLK2/GPIO24	
CS1/QSPICS3/GPIO28	

3.16 Crystal Trim

The XTRIM/GPIO0 output produces a pulse-density modulated phase/frequency difference signal to be used after low-pass filtering to control varicap-voltage to control crystal oscillation frequency. This will lock the crystal to the incoming digital audio signal.

3.17 Clock Out

The MCLK1/GPIO11 and QSPI_CS2/MCLK2/GPIO24 can serve as DAC clock outputs. When programmed as DAC clock outputs, these signals are directly derived from the crystal oscillator or clock Input (CRIN).

3.18 Debug and Test Signals

These signals interface with external I/O to provide processor debug and status signals.

3.18.1 Test Mode

The TEST[2:0] inputs are used for various manufacturing and debug tests. For normal mode TEST [2:1] should be ways be tied low. TEST0 should be set high for BDM debug mode and set low for JTAG mode.

3.18.2 High Impedance

The assertion of $\overline{\text{HI\_Z}}$ will force all output drivers to a high-impedance state. The timing on $\overline{\text{HI\_Z}}$ is independent of the clock.

NOTE

JTAG operation will override the $\overline{\text{HI\_Z}}$ pin.

3.18.3 Processor Clock Output

The internal PLL generates this PSTCLK/GPIO51 and output signal, and is the processor clock output that is used as the timing reference for the Debug bus timing (DDATA[3:0] and PST[3:0]). The PSTCLK/GPIO51 is at the same frequency as the core processor.

3.18.4 Debug Data

The debug data pins, DDATA0/CTS1/SDATA0_SDIO1/GPIO1, DDATA1/RTS1/SDATA2_BS2/GPIO2, DDATA2/CTS0/GPIO3, and DDATA3/RTS0/GPIO4, are four bits wide. This nibble-wide bus displays captured processor data and break-point status.

3.18.5 Processor Status

The processor status pins, PST0/GPIO50, PST1/GPIO49, PST2/INTMON/GPIO48, and PST3/INTMON/GPIO47, indicate the SCF5250 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. Table 12 shows the encodings of these signals.

Table 17 provides the linear regulator operating specifications for the SCF5250 processor.

Table 17. Linear Regulator[1] Operating Specification

Characteristic	Symbol	Min	Typ	Max
Input Voltage	Vin	3.0V	3.3V	3.6
Output Voltage (LINOUT)	Vout	1.14V	1.2V	1.26V
Output Current	Iout	–	100mA	150mA
Power Dissipation	Pd	–	–	436uW
Load Regulation (10% Iout ≥ 90% Iout)	–	40mV	50mV	60mV
Power Supply Rejection	PSRR	–	40dB	–

1 A pmos regulator is employed as a current source in this Linear regulator, so a 10µF capacitor (ESR 0 ... 5 Ohm) is needed on the output pin (LINOUT) to integrate the current. Typically this will require the use of a Tantalum type capacitor.

Table 18 provides the DC electrical specifications.

Table 18. DC Electrical Specifications (I/O Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current @ 0.0 V /3.3 V During Normal Operation	I_{in}	–	±1	µµA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	–	±1	µµA
Output High Voltage I_{OH} = 8mA[1], 4mA[2], 2mA[3]	V_{OH}	2.4	–	V
Output Low Voltage I_{OL} = 8mA[1], 4mA[2], 2mA[3]	V_{OL}	–	0.4	V
Schmitt Trigger Low to High Threshold Point[6]	V_{T+}	1.47	–	V
Schmitt Trigger High to Low Threshold Point[6]	V_{T-}	–	.95	V
Load Capacitance (DATA[31:16], SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[3:1], SDATAO[2:1], CFLG, EF, DDATA[3:0], PST[3:0], PSTCLK, IDE-DIOR, IDE-DIOW, IORDY)	C_L	–	50	pF
Load Capacitance (ADDR[24:9], BCLK)	C_L	–	40	pF
Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SD_CS0, SDUDQM, SDWE, BUFENB[2:1])	C_L	–	30	pF
Load Capacitance (SDA0, SDA1, SCL0, SCL1, CMD_SDIO2, SDATA2_BS2, SDATA1_BS1, SDATA0_SDIO1, CS0/CS4, CS1, OE, R/$\overline{W}$, TA, TXD[1:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT0, QSPID_OUT, QSPICS[3:0], GP[6:5])	C_L	–	20	pF

Table 22. Output AC Timing Specification (continued)

Num	Characteristic[1]	Min	Max	Units
H1	$\overline{HIZ}$ to High Impedance	–	tbd	ns
H2	$\overline{HIZ}$ to Low Impedance	–	tbd	ns

1 AC timing specs assume 40pF load capacitance on BCLK and a 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 Outputs (8mA): DATA[31:16], ADDR[25,23:9]

3 Outputs (4mA): SDRAS, SDCAS, SDWE, SD_CS0, SDUDQM, SDLDQM, BCLKE

4 High Impedance (Three-State): DATA[31:16]

Figure 5 and Table 23 provide the timing diagram and timing parameters for the Debug AC.

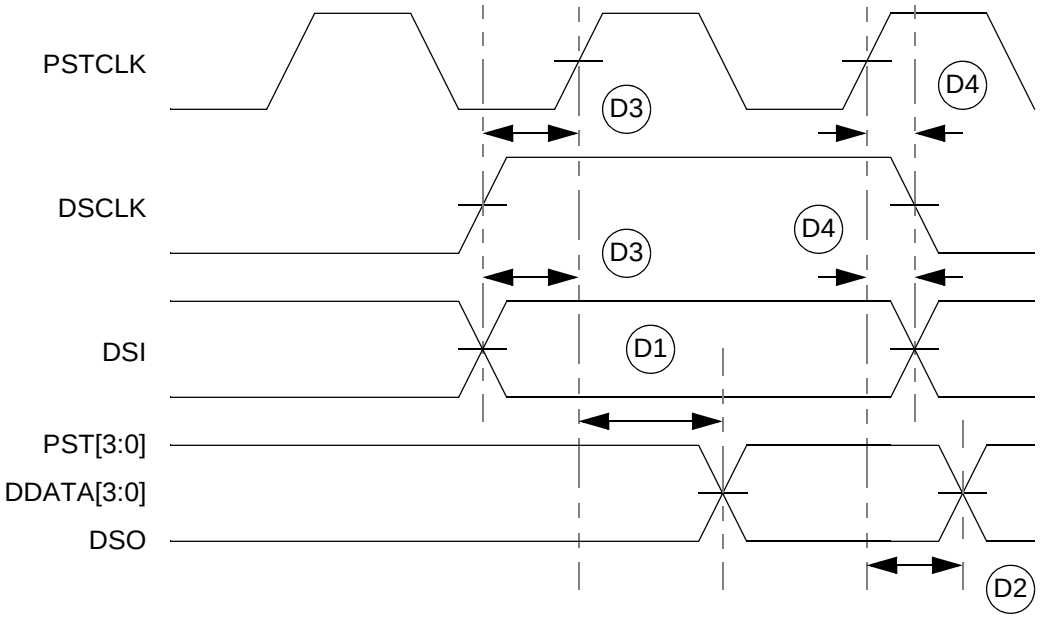

Figure 5. Debug AC Timing Definition Diagram

Table 23. Debug AC Timing Specification[1]

Num	Characteristic	Min	Max	Units
D1	PSTCLK to signal Valid (Output valid)	–	6	ns
D2	PSTCLK to signal Invalid (Output hold)	1.8	–	ns
D3[2]	Signal Valid to PSTCLK (Input setup)	3	–	ns
D4	PSTCLK to signal Invalid (Input hold)	5	–	ns

1 AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.

Figure 7 and Table 25 provide the timing diagram and timing parameters for the UART module.

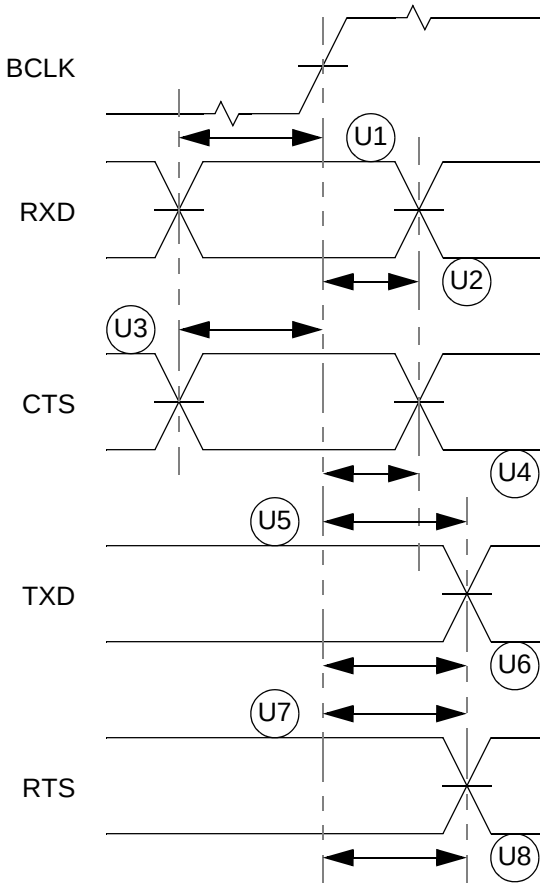

Figure 7. UART Module AC Timing Definition Diagram

Table 25. UART Module AC Timing Specifications

Num	Characteristic	Min	Max	Units
U1	RXD Valid to BCLK (input setup)	6	–	ns
U2	BCLK to RXD Invalid (input hold)	0	–	ns
U3	$\overline{\text{CTS}}$ Valid to BCLK (input setup)	6	–	ns
U4	BCLK to $\overline{\text{CTS}}$ Invalid (input hold)	0	–	ns
U5	BCLK to TXD Valid (output valid)	–	tbd	ns
U6	BCLK to TXD Invalid (output hold)	3	–	ns
U7	BCLK to $\overline{\text{RTS}}$ Valid (output valid)	–	tbd	ns
U8	BCLK to $\overline{\text{RTS}}$ Invalid (output hold)	3	–	ns

Table 30. JTAG AC Timing Specifications (continued)

Num	Characteristic	Min	Max	Units
J11	TCK falling to Boundary Scan Data Valid (signal from driven or three-state)	–	tbd	ns
J12	TCK falling to Boundary Scan. Data High Impedance	–	tbd	ns

Figure 12 provides the SCLK input, SDATA output timing diagram for the IIS module and Table 31 provides the timing parameters.

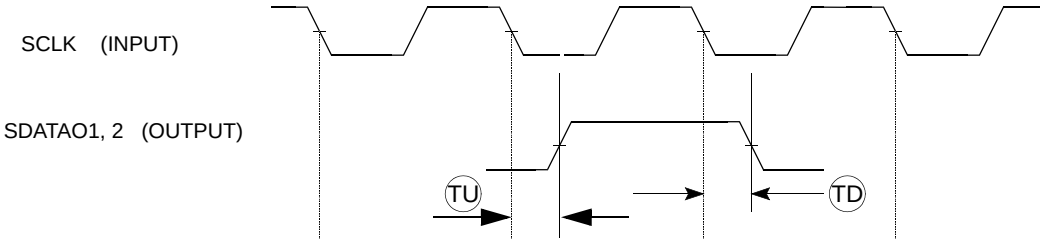

Figure 12. SCLK Input, SDATA Output Timing Diagram

Table 31. SCLK Input, SDATA Output Timing Specifications

Num	Characteristic	Min	Max	Units
TU	SCLK fall to SDATAO rise	–	25	ns
TD	SCLK fall to SDATAO fall	–	25	ns

Figure 13 provides the SCLK output, SDATA output timing diagram for the IIS module and Table 32 provides the timing parameters.

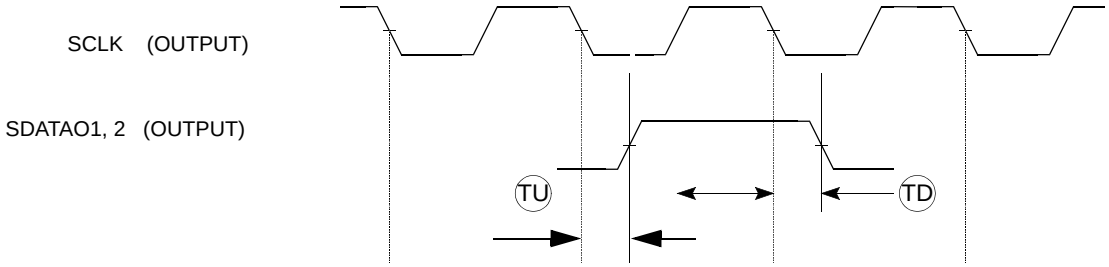

Figure 13. SCLK Output, SDATA Output Timing Diagram

Table 32. SCLK Output, SDATA Output Timing Specifications

Num	Characteristic	Min	Max	Units
TU	SCLK fall to SDATAO rise	–	3	ns
TD	SCLK fall to SDATAO fall	–	3	ns

Table 35. 144 QFP Pin Assignments

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
01	DATA16	I/O	Data	X
02	A23/GPO54	I/O	SDRAM address / static adr	Out (requires pull up /down for boot-up selection)
03	PAD-VDD	–	–	–
04	A22	O	SDRAM address / static adr	Out
05	A21	O	SDRAM address / static adr	Out
06	A20/A24	O	SDRAM address / static adr	Out
07	A19	O	SDRAM address / static adr	Out
08	A18	O	SDRAM address / static adr	Out
09	PAD-GND	–	–	–
10	A17	O	SDRAM address / static adr	Out
11	A16	O	SDRAM address / static adr	Out
12	A15	O	SDRAM address / static adr	Out
13	A14	O	SDRAM address / static adr	Out
14	A13	O	SDRAM address / static adr	Out
15	PAD-VDD	–	–	–
16	A12	O	SDRAM address / static adr	Out
17	A11	O	SDRAM address / static adr	Out
18	CORE-VDD	–	–	–
19	CORE-GND	–	–	–
20	A10	O	SDRAM address / static adr	Out
21	A9	O	SDRAM address / static adr	Out
22	A8	O	SDRAM address / static adr	Out
23	A7	O	SDRAM address / static adr	Out
24	A6	O	SDRAM address / static adr	Out
25	A5	O	SDRAM address / static adr	Out
26	PAD-GND	–	PAD-GND	–
27	A4	O	SDRAM address / static adr	Out
28	A3	O	SDRAM address / static adr	Out
29	A2	O	SDRAM address / static adr	Out
30	A1	O	SDRAM address / static adr	Out
31	CS0/CS4	O	Static chip select 0 / static chip select 4	Out

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
32	RW	O	Bus write enable	Out
33	OSC PAD VDD	–	–	–
34	CRIN	I	Crystal / external clock input	X
35	CROUT	O	Crystal clock output	X
36	OSC PAD GND	–	OSC_PAD_GND	–
37	PLL CORE1 VDD	–	–	–
38	PLL CORE2 VDD	–	–	–
39	PLL CORE2 GND	–	–	–
40	PLL CORE1 GND	–	–	–
41	OE	O	Output Enable	Out
42	IDE-DIOW/GPIO32	I/O	IDE DIOW	Out / HIGH
43	IDE-IORDY/GPIO33	I/O	IDE interface IORDY	In / LOW
44	IDE-DIOR/GPIO31	I/O	IDE interface DIOR	Out / HIGH
45	BUFENB2/GPIO30	I/O	External buffer 2 enable	Out / HIGH
46	BUFENB1/GPIO29	I/O	External buffer 1 enable	Out / HIGH
47	TA/GPIO12	I/O	Transfer acknowledge	In (requires pull-up for normal operation)
48	WAKE_UP/GPIO21	I/O	Wake-up input	In (requires pull-up for normal operation)
49	EBUIN2/SCLK_OUT/ GPIO13	I/O	Audio interfaces EBU in 2 / FlashMedia Clock	In / LOW
50	EBUIN3/CMD_SDIO2/ GPIO14	I/O	Audio interfaces EBU in 3 / FlashMedia Command interface	In / LOW
51	PAD VDD	–	–	–
52	EBUIN1/GPIO36	I/O	Audio interfaces EBU in 1	In / LOW
53	EBUOUT1/GPIO37	I/O	Audio interfaces EBU out 1	Out / LOW
54	XTRIM/GPIO0	I/O	Audio interfaces X-tal trim	Out / clock out
55	CS1/QSPI_CS3/GPIO28	I/O	Chip select 1/ QSPI Chip Select 3	Out / HIGH
56	RCK/ QSPI_DIN/QSPI_DOUT/ GPIO26	I/O	Subcode RCK interface / QSPI Data In / Data Out	Out / LOW
57	QSPI_CLK/SUBR/GPIO25	I/O	QSPI clock pin / subcode interface	Out / LOW
58	QSPI_DOUT/SFSY/ GPIO27	I/O	QSPI Data Output / subcode interface SFSY	Out / LOW

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
116	TEST1	I	Test	X
117	TEST0	I	Test	X
118	SDWE/GPIO38	I/O	SDRAM write enable	Out / HIGH
119	SDCAS/GPIO39	I/O	SDRAM CAS	Out / HIGH
120	PAD VDD	–	–	–
121	SDRAS/GPIO59	I/O	SDRAM RAS	Out / HIGH
122	SD_CS0/GPIO60	I/O	SDRAM chip select out 0	Out / HIGH
123	SDLDQM/GPO52	O	SDRAM LDQM	Out / HIGH
124	SDUDQM/GPO53	O	SDRAM UDQM	Out / HIGH
125	BCLKE/GPIO63	I/O	SDRAM clock enable output	Out / HIGH
126	BCLK/GPIO40	I/O	SDRAM clock output	Out / HIGH
127	DATA31	I/O	Data	X
128	DATA30	I/O	Data	X
129	PAD GND	–	–	–
130	DATA29	I/O	Data	X
131	DATA28	I/O	Data	X
132	DATA27	I/O	Data	X
133	DATA26	I/O	Data	X
134	DATA25	I/O	Data	X
135	PAD-VDD	–	–	–
136	DATA24	I/O	Data	X
137	DATA23	I/O	Data	X
138	DATA22	I/O	Data	X
139	DATA21	I/O	Data	X
140	DATA20	I/O	Data	X
141	PAD GND	–	–	–
142	DATA19	I/O	Data	X
143	DATA18	I/O	Data	X
144	DATA17	I/O	Data	X

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
J2	A6	O	SDRAM address / static adr	Out
L1	A5	O	SDRAM address / static adr	Out
P_GND	PAD_GND		PAD_GND	
J3	A4	O	SDRAM address / static adr	Out
K2	A3	O	SDRAM address / static adr	Out
L2	A2	O	SDRAM address / static adr	Out
M1	A1	O	SDRAM address / static adr	Out
K3	CS0	O	Static chip select 0	Out
L3	RWB	O	Bus write enable	Out
J5	OSCPAD_VDD		OSCPAD_VDD	
M2	CRIN		Crystal / external clock input	X
N1	CROUT		Crystal clock output	X
J6	OSCPAD_GND		OSCPAD_GND	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
M3	OE	O	Output enable	Out
M4	IDEDIOW_GP32	I/O	IDE DIOW	Out / High
M5	IDEIORDY_GP33	I/O	IDE interface IORDY	Out / Low
N3	IDEDIOR_GP31	I/O	IDE interface DIOR	Out / High
M6	BUFENB2_GP30	I/O	External Buffer 2 enable	Out / High
P2	BUFENB1_GP29	I/O	External Buffer 1 enable	Out / High
N4	TA_GP12	I/O	Transfer acknowledge	In (requires pull-up for normal operation)

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
B9	SDWE_GP38	I/O	SDRAM write enable	Out / High
A10	SDCAS_GP39	I/O	SDRA CAS	Out / High
P_VDD	PAD_VDD		PAD_VDD	Out / High
C8	SDRAS_GP59	I/O	SDRAM RAS	Out / High
A9	SDCS0_GP60	I/O	SDRAM chip select out 0	Out / High
B8	SDLDQM_GPO52	O	SDRAM LDQM	Out / High
A8	SDUDQM_GPO53	O	SDRAM UDQM	Out / High
A7	BCLKE_GPO63	O	SDRAM clock enable output	Out / High
A6	BCLK_GP40	I/O	SDRAM clock output	Out / High
B7	DATA31	I/O	Data	X
A5	DATA30	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C7	DATA29	I/O	Data	X
B6	DATA28	I/O	Data	X
A4	DATA27	I/O	Data	X
B5	DATA26	I/O	Data	X
C6	DATA25	I/O	Data	X
P_VDD	PAD_VDD	I/O	PAD_VDD	
B4	DATA24	I/O	Data	X
B3	DATA23	I/O	Data	X
C5	DATA22	I/O	Data	X
A2	DATA21	I/O	Data	X
B2	DATA20	I/O	Data	X
P_GND	PAD_GND	I/O	PAD_GND	
C4	DATA19	I/O	Data	X
C3	DATA18	I/O	Data	X
C2	DATA17	I/O	Data	X

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
A1	BGA1_NC_A1	NC		
A14	BGA1_NC_A14	NC		
P1	BGA1_NC_P1	NC		
P14	BGA1_NC_P14	NC		

5.4 196 MAPBGA Package and Ball Map

The SCF5250 is available in a 196-pin MAPBGA package. For the 196 MAPBGA package drawings, refer to Figure 18 on page 52 and Figure 19 on page 53.

For the 196 MAPBGA ball map, refer to Figure 20 on page 54.

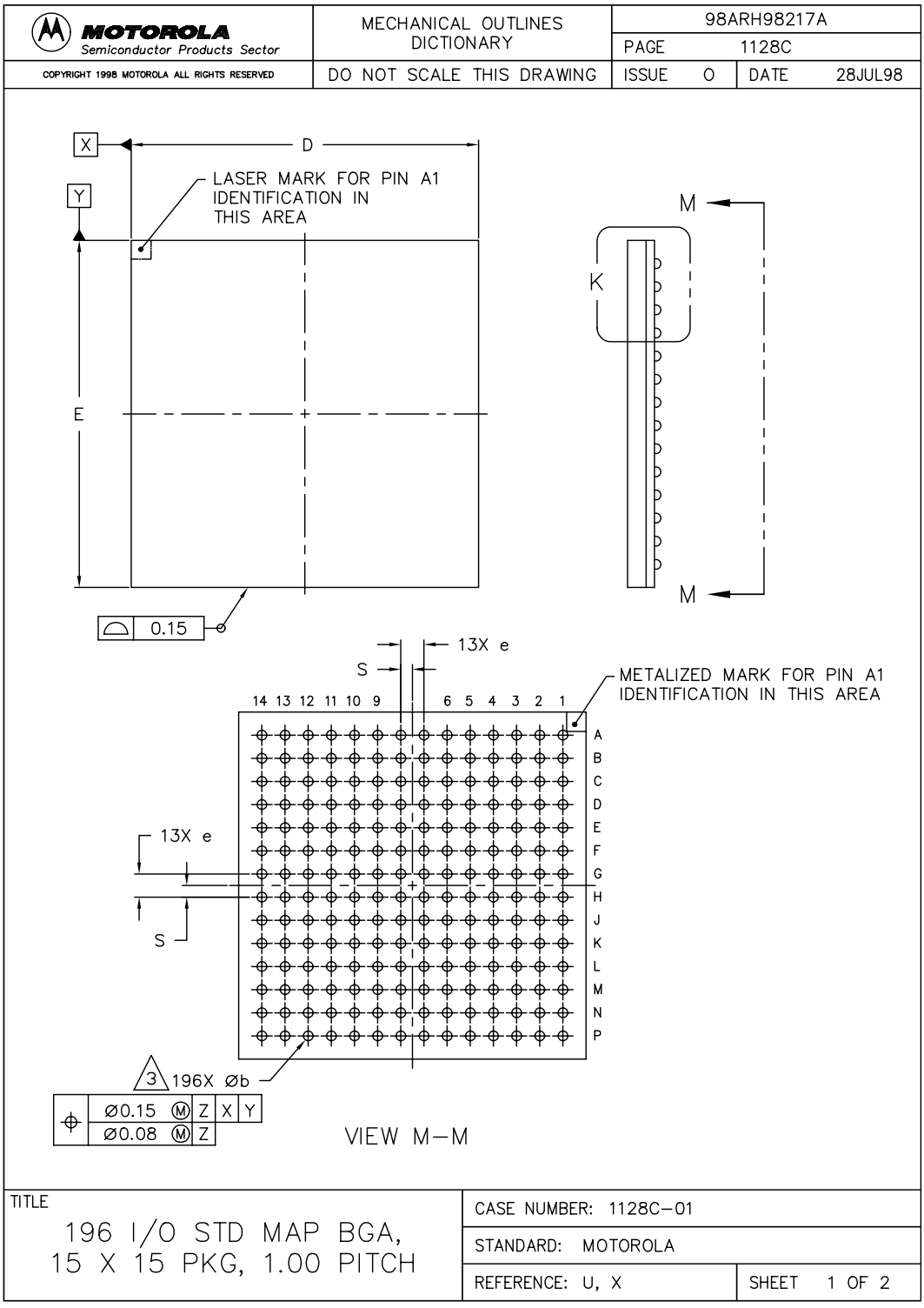

Figure 18. 196 MAPBGA Package (1 of 2)