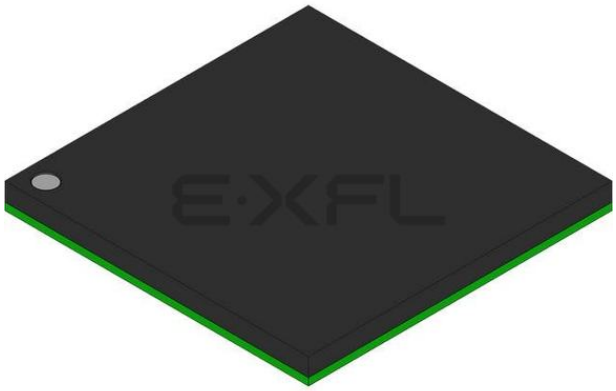

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	57
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 1.32V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=scf5250vm120

integrated peripherals and enhanced MAC unit allow the SCF5250 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

1.1 Orderable Part Numbers

Table 1 lists the orderable part numbers for the SCF5250 processor.

Table 1. Orderable Part Numbers

Orderable Part Number	Maximum Clock Frequency	Package Type	Operating Temperature Range	Part Status
SCF5250LPV100	100 MHz	144 pin QFP	-20°C to 70°C	Leaded
SCF5250LAG100	100 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250PV120	120 MHz	144 pin QFP	-20°C to 70°C	Leaded
SCF5250AG120	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250DAG120[1]	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250EAG120[2]	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5250CPV120	120 MHz	144 pin QFP	-40°C to 85°C	Leaded
SCF5250CAG120	120 MHz	144 pin QFP	-40°C to 85°C	Lead Free
SCF5250VM120	120 MHz	196 ball MAPBGA	-20°C to 70°C	Lead Free

1 SCF5250DAG120—This device has the same feature set, pin assignment and specification as SCF5250AG120 with the addition of including the cost of the MP3 decoder royalty to be paid to Thomson Licensing S.A. for use of the MP3 patent rights described at http://mp3licensing.com/patents/index.html.

2 SCF5250EAG120—This device has the same feature set, pin assignment and specification as SCF5250AG120 with the addition of including the cost of the MP3 encoder and decoder royalty to be paid to Thomson Licensing S.A. for use of the MP3 patent rights described at http://mp3licensing.com/patents/index.html.

1.2 SCF5250 Features

This section provides brief descriptions of the features of the SCF5250 processor.

1.2.1 ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

1.2.7 System Interface

The SCF5250 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SCF5250 also supports bursting ROMs.

1.2.8 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

1.2.9 Serial Audio Interfaces

The SC5250 digital audio interface provides three serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other two interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

1.2.10 IEC958 Digital Audio Interfaces

The SCF5250 has one digital audio input interface, and one digital audio output interface. The single output carries the consumer “c” channel.

1.2.11 Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

1.2.12 CD-ROM Encoder/Decoder

The SCF5250 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

1.2.22 JTAG

To help with system diagnostics and manufacturing testing, the SCF5250 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1A standard. Freescale provides BSDL files for JTAG testing.

1.2.23 System Debug Interface

The ColdFire processor core debug interface supports real-time instruction trace and debug, plus background-debug mode. A background-debug mode (BDM) interface provides system debug.

In real-time instruction trace, four status lines provide information on processor activity in real time (PST pins). A four-bit wide debug data bus (DDATA) displays operand data and change-of-flow addresses, which helps track the machine's dynamic execution path.

1.2.24 Crystal and On-Chip PLL

Typically, an external 16.92 MHz or 33.86 MHz clock input is used for CD R/W applications, while an 11.2896 MHz clock is more practical for Portable CD player applications. However, the on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5-35 MHz).

Two clock outputs (MCLK1 and MCLK2) are provided for use as Audio Master Clock. The output frequencies of both outputs are programmable to Fxtal, Fxtal/2, Fxtal/3, and Fxtal/4. The Fxtal/3 option is only available when the 33.86 MHz crystal is connected.

The SCF5250 supports VCO operation of the oscillator by means of a 16-bit pulse density modulation output. Using this mode, it is possible to lock the oscillator to the frequency of an incoming IEC958 or IIS signal. The maximum trim depends on the type and design of the oscillator. Typically a trim of +/- 100 ppm can be achieved with a crystal oscillator and over +/- 1000 ppm with an LC oscillator.

1.2.25 Boot ROM

The boot ROM on the SCF5250 serves to boot the CPU in designs which do not have external Flash memory or ROM. Typically this occurs in systems which have a separate MCU to control the system, and/or the SCF5250 is used as a stand-alone decoder.

The SCF5250 can be booted in one of three modes:

- External ROM
- Internal ROM Master mode – boots from I2C, SPI, or IDE
- Internal ROM Slave mode – boots from I2C or UART

1.2.26 Voltage Regulator

The SCF5250 contains an on-chip linear regulator that generates 1.2V from a 3.3V input. The regulator is self-contained and drives the 1.2V core voltage out on one pin that can be used to power the core supply

Table 2. SCF5250 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Transmit Data	SCL1/TXD1/GPIO10 TXD0/GPIO45	Signal is transmit serial data output for DUART	Out	–
Request-To-Send	DDATA3/$\overline{\text{RTS0}}$/GPIO4 DDATA1/$\overline{\text{RTS1}}$/SDATA2_BS2/GPIO2	DUART signals a ready to receive data query	Out	–
Clear-To-Send	DDATA2/$\overline{\text{CTSO}}$/GPIO3 DDATA0/$\overline{\text{CTS1}}$/SDATA0_SDIO1/GPIO1	Signals to DUART that data can be transmitted to peripheral	In	–
Timer Output	SDATAO1/TOUT0/GPIO18	Capable of output waveform or pulse generation	Out	–
IEC958 inputs	EBUIN1/GPIO36 EBUIN2/SCLK_OUT/GPIO13 EBUIN3/CMD_SDIO2/GPIO14 QSPI_CS0/EBUIN4/GPIO15	audio interfaces IEC958 inputs	In	–
IEC958 outputs	EBUOUT1/GPIO37 QSPI_CS1/EBUOUT2/GPIO16	audio interfaces IEC958 outputs	Out	–
Serial data in	SDATAI1/GPIO17 SDATAI3/GPIO8	audio interfaces serial data inputs	In	–
Serial data out	SDATAO1/TOUT0/GPIO18 SDATAO2/GPIO34	audio interfaces serial data outputs	In/Out Out	–
Word clock	LRCK1/GPIO19 LRCK2/GPIO23 LRCK3/GPIO43/AUDIO_CLOCK	audio interfaces serial word clocks	In/Out	–
Bit clock	SCLK1/GPIO20 SCLK2/GPIO22 SCLK3/GPIO35	audio interfaces serial bit clocks	In/Out	–
Serial input	EF/GPIO6	error flag serial in	In/Out	–
Serial input	CFLG/GPIO5	C-flag serial in	In/Out	–
Subcode clock	RCK/QSPI_DIN/QSPI_DOUT/ GPIO26	audio interfaces subcode clock	In/Out	–
Subcode sync	QSPI_DOUT/SFSY/GPIO27	audio interfaces subcode sync	In/Out	–
Subcode data	QSPI_CLK/SUBR/GPIO25	audio interfaces subcode data	In/Out	–
Clock frequency trim	XTRIM/GPIO0	clock trim control	Out	–
Audio clocks out	MCLK1/GPIO11 QSPI_CS2/MCLK2/GPIO24	DAC output clocks	Out	–
Audio clock in	LRCK3/GPIO43/AUDIO_CLOCK	Optional Audio clock Input	–	–

3.4 Chip Selects

There are three chip select outputs on the SCF5250 device. $\overline{CS0}$/$\overline{CS4}$ and $\overline{CS1}$/QSPI_CS3/GPIO28 and CS2 which is associated with the IDE interface read and write strobes - IDE-DIOR and IDE-DIOW.

CS0 and CS4 are multiplexed. The SCF5250 has the option to boot from an internal Boot ROM. The function of the CS0/CS4 pin is determined by the boot mode. When the device is booted from internal ROM, the internal ROM is accessed with CS0 (required for boot) and the CS0/CS4 pin is driven by CS4. When the device is booted from external ROM / Flash, the CS0/CS4 pin is driven by CS0 and the internal ROM is disabled.

The active low chip selects can be used to access asynchronous memories. The interface is glueless.

3.5 ISA Bus

The SCF5250 supports an ISA bus. Using the ISA bus protocol, reads and writes for one ISA bus peripheral is possible. $\overline{IDE\text{-}DIOR}$/GPIO31 and $\overline{IDE\text{-}DIOW}$/GPIO32 are the read and write strobe. The peripheral can insert wait states by pulling IDE-IORDY/GPIO33.

CS2 is associated with the IDE-DIOR and IDE-DIOW.

3.6 Bus Buffer Signals

As the SCF5250 has a complicated slave bus, which allows SDRAM, asynchronous memories, and ISA peripherals on the bus, it may become necessary to introduce a buffer on the bus in certain applications. The SCF5250 has a glueless interface to steer these bus buffers with two bus buffer output signals $\overline{BUFENB1}$/GPIO29 and $\overline{BUFENB2}$/GPIO30.

3.7 I^2C Module Signals

There are two I^2C interfaces on this device as described in Table 4.

The I^2C module acts as a two-wire, bidirectional serial interface between the SCF5250 processor and peripherals with an I^2C interface (e.g., LED controller, A-to-D converter, D-to-A converter). When devices connected to the I^2C bus drive the bus, they will either drive logic-0 or high-impedance. This can be accomplished with an open-drain output.

Table 4. I^2C Module Signals

I^2c Module Signal	Description
I^2C Serial Clock	The SCL0/SDATA1_BS1/GPIO41 and SCL1/TXD1/GPIO10 bidirectional signals are the clock signal for first and second I^2C module operation. The I^2C module controls this signal when the bus is in master mode; all I^2C devices drive this signal to synchronize I^2C timing. Signals are multiplexed
I^2C Serial Data	The SDA0/SDATA3/GPIO42 and SDA1/RXD1/GPIO44 bidirectional signals are the data input/output for the first and second serial I^2C interface. Signals are multiplexed

Table 14. Maximum Ratings

Rating	Symbol	Value	Units
Supply Core Voltage	V_{cc}	-0.5 to +2.5	V
Maximum Core Operating Voltage	V_{cc}	+1.32	V
Minimum Core Operating Voltage	V_{cc}	+1.08	V
Supply I/O Voltage	V_{cc}	-0.5 to +4.6	V
Maximum I/O Operating Voltage	V_{cc}	+3.6	V
Minimum I/O Operating Voltage	V_{cc}	+3.0	V
Input Voltage	V_{in}	-0.5 to +6.0	V
Storage Temperature Range	T_{stg}	-65 to150	°C

Table 15 provides the recommended operating temperatures for the SCF5250 processor.

Table 15. Operating Temperature

Characteristic	Symbol	Value	Units
Maximum Operating Ambient Temperature	T_{Amax}	85[1]	°C
Minimum Operating Ambient Temperature	T_{Amin}	-40	°C

1 This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature does not exceed 105°C.

Table 16 provides the recommended operating supply voltages for the SCF5250 processor.

Table 16. Recommended Operating Supply Voltages

Pin Name	Min	Typ	Max
CORE-VDD	1.08V	1.2V	1.32V
CORE-VSS	–	gnd	–
PAD-VDD	3.0V	3.3v	3.6V
PAD-VSS	–	gnd	–
ADVDD	3.0V	3.3v	3.6V
ADGND	–	gnd	–
OSCPAD-VDD	3.0V	3.3v	3.6V
OSCPAD-GND	–	gnd	–
PLLCORE1VDD	1.08V	1.2V	1.32V
PLLCORE1GND	–	gnd	–
PLLCORE2VDD	1.08V	1.2v	1.32V
PLLCORE2GND	–	gnd	–
LIN	3.0v	3.3V	3.6V

Table 22. Output AC Timing Specification (continued)

Num	Characteristic[1]	Min	Max	Units
H1	$\overline{HIZ}$ to High Impedance	–	tbd	ns
H2	$\overline{HIZ}$ to Low Impedance	–	tbd	ns

1 AC timing specs assume 40pF load capacitance on BCLK and a 50pF load capacitance on output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 Outputs (8mA): DATA[31:16], ADDR[25,23:9]

3 Outputs (4mA): SDRAS, SDCAS, SDWE, SD_CS0, SDUDQM, SDLDQM, BCLKE

4 High Impedance (Three-State): DATA[31:16]

Figure 5 and Table 23 provide the timing diagram and timing parameters for the Debug AC.

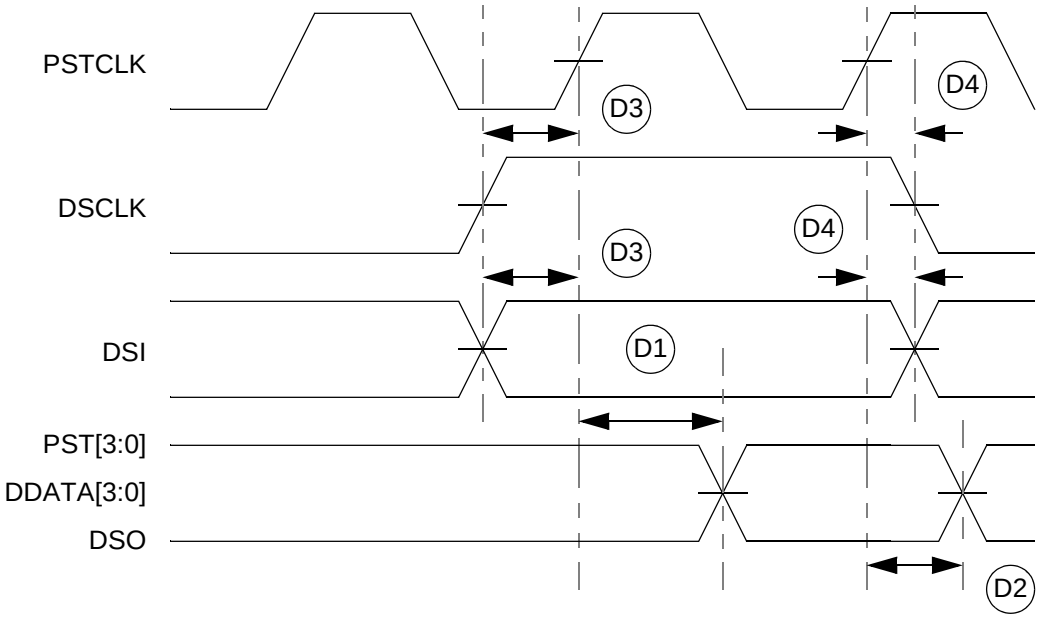

Figure 5. Debug AC Timing Definition Diagram

Table 23. Debug AC Timing Specification[1]

Num	Characteristic	Min	Max	Units
D1	PSTCLK to signal Valid (Output valid)	–	6	ns
D2	PSTCLK to signal Invalid (Output hold)	1.8	–	ns
D3[2]	Signal Valid to PSTCLK (Input setup)	3	–	ns
D4	PSTCLK to signal Invalid (Input hold)	5	–	ns

1 AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

2 DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.

Figure 7 and Table 25 provide the timing diagram and timing parameters for the UART module.

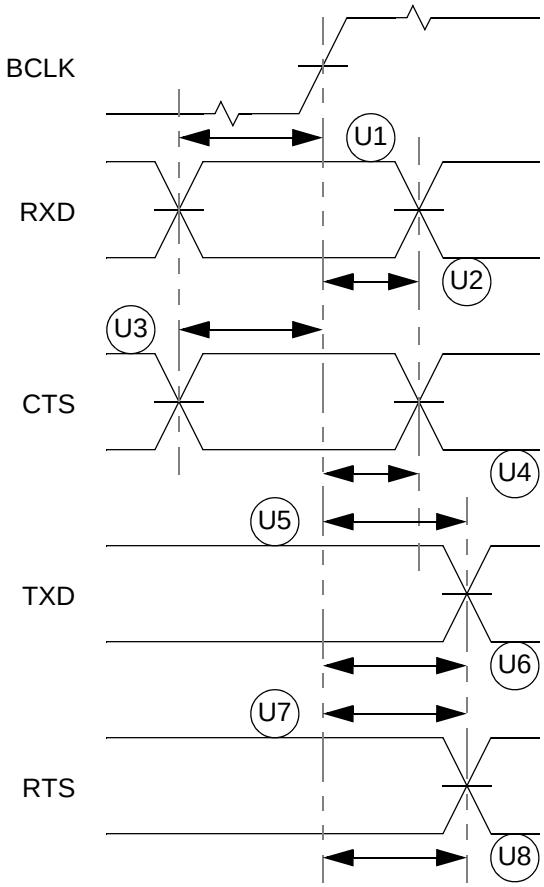

Figure 7. UART Module AC Timing Definition Diagram

Table 25. UART Module AC Timing Specifications

Num	Characteristic	Min	Max	Units
U1	RXD Valid to BCLK (input setup)	6	–	ns
U2	BCLK to RXD Invalid (input hold)	0	–	ns
U3	$\overline{\text{CTS}}$ Valid to BCLK (input setup)	6	–	ns
U4	BCLK to $\overline{\text{CTS}}$ Invalid (input hold)	0	–	ns
U5	BCLK to TXD Valid (output valid)	–	tbd	ns
U6	BCLK to TXD Invalid (output hold)	3	–	ns
U7	BCLK to $\overline{\text{RTS}}$ Valid (output valid)	–	tbd	ns
U8	BCLK to $\overline{\text{RTS}}$ Invalid (output hold)	3	–	ns

Table 35. 144 QFP Pin Assignments

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
01	DATA16	I/O	Data	X
02	A23/GPO54	I/O	SDRAM address / static adr	Out (requires pull up /down for boot-up selection)
03	PAD-VDD	–	–	–
04	A22	O	SDRAM address / static adr	Out
05	A21	O	SDRAM address / static adr	Out
06	A20/A24	O	SDRAM address / static adr	Out
07	A19	O	SDRAM address / static adr	Out
08	A18	O	SDRAM address / static adr	Out
09	PAD-GND	–	–	–
10	A17	O	SDRAM address / static adr	Out
11	A16	O	SDRAM address / static adr	Out
12	A15	O	SDRAM address / static adr	Out
13	A14	O	SDRAM address / static adr	Out
14	A13	O	SDRAM address / static adr	Out
15	PAD-VDD	–	–	–
16	A12	O	SDRAM address / static adr	Out
17	A11	O	SDRAM address / static adr	Out
18	CORE-VDD	–	–	–
19	CORE-GND	–	–	–
20	A10	O	SDRAM address / static adr	Out
21	A9	O	SDRAM address / static adr	Out
22	A8	O	SDRAM address / static adr	Out
23	A7	O	SDRAM address / static adr	Out
24	A6	O	SDRAM address / static adr	Out
25	A5	O	SDRAM address / static adr	Out
26	PAD-GND	–	PAD-GND	–
27	A4	O	SDRAM address / static adr	Out
28	A3	O	SDRAM address / static adr	Out
29	A2	O	SDRAM address / static adr	Out
30	A1	O	SDRAM address / static adr	Out
31	CS0/CS4	O	Static chip select 0 / static chip select 4	Out

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
32	RW	O	Bus write enable	Out
33	OSC PAD VDD	–	–	–
34	CRIN	I	Crystal / external clock input	X
35	CROUT	O	Crystal clock output	X
36	OSC PAD GND	–	OSC_PAD_GND	–
37	PLL CORE1 VDD	–	–	–
38	PLL CORE2 VDD	–	–	–
39	PLL CORE2 GND	–	–	–
40	PLL CORE1 GND	–	–	–
41	OE	O	Output Enable	Out
42	IDE-DIOW/GPIO32	I/O	IDE DIOW	Out / HIGH
43	IDE-IORDY/GPIO33	I/O	IDE interface IORDY	In / LOW
44	IDE-DIOR/GPIO31	I/O	IDE interface DIOR	Out / HIGH
45	BUFENB2/GPIO30	I/O	External buffer 2 enable	Out / HIGH
46	BUFENB1/GPIO29	I/O	External buffer 1 enable	Out / HIGH
47	TA/GPIO12	I/O	Transfer acknowledge	In (requires pull-up for normal operation)
48	WAKE_UP/GPIO21	I/O	Wake-up input	In (requires pull-up for normal operation)
49	EBUIN2/SCLK_OUT/ GPIO13	I/O	Audio interfaces EBU in 2 / FlashMedia Clock	In / LOW
50	EBUIN3/CMD_SDIO2/ GPIO14	I/O	Audio interfaces EBU in 3 / FlashMedia Command interface	In / LOW
51	PAD VDD	–	–	–
52	EBUIN1/GPIO36	I/O	Audio interfaces EBU in 1	In / LOW
53	EBUOUT1/GPIO37	I/O	Audio interfaces EBU out 1	Out / LOW
54	XTRIM/GPIO0	I/O	Audio interfaces X-tal trim	Out / clock out
55	CS1/QSPI_CS3/GPIO28	I/O	Chip select 1/ QSPI Chip Select 3	Out / HIGH
56	RCK/ QSPI_DIN/QSPI_DOUT/ GPIO26	I/O	Subcode RCK interface / QSPI Data In / Data Out	Out / LOW
57	QSPI_CLK/SUBR/GPIO25	I/O	QSPI clock pin / subcode interface	Out / LOW
58	QSPI_DOUT/SFSY/ GPIO27	I/O	QSPI Data Output / subcode interface SFSY	Out / LOW

Table 35. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description	Pin State After Reset
116	TEST1	I	Test	X
117	TEST0	I	Test	X
118	SDWE/GPIO38	I/O	SDRAM write enable	Out / HIGH
119	SDCAS/GPIO39	I/O	SDRAM CAS	Out / HIGH
120	PAD VDD	–	–	–
121	SDRAS/GPIO59	I/O	SDRAM RAS	Out / HIGH
122	SD_CS0/GPIO60	I/O	SDRAM chip select out 0	Out / HIGH
123	SDLDQM/GPO52	O	SDRAM LDQM	Out / HIGH
124	SDUDQM/GPO53	O	SDRAM UDQM	Out / HIGH
125	BCLKE/GPIO63	I/O	SDRAM clock enable output	Out / HIGH
126	BCLK/GPIO40	I/O	SDRAM clock output	Out / HIGH
127	DATA31	I/O	Data	X
128	DATA30	I/O	Data	X
129	PAD GND	–	–	–
130	DATA29	I/O	Data	X
131	DATA28	I/O	Data	X
132	DATA27	I/O	Data	X
133	DATA26	I/O	Data	X
134	DATA25	I/O	Data	X
135	PAD-VDD	–	–	–
136	DATA24	I/O	Data	X
137	DATA23	I/O	Data	X
138	DATA22	I/O	Data	X
139	DATA21	I/O	Data	X
140	DATA20	I/O	Data	X
141	PAD GND	–	–	–
142	DATA19	I/O	Data	X
143	DATA18	I/O	Data	X
144	DATA17	I/O	Data	X

5.2 144 QFP Package

The SCF5250 is available in a 144-pin QFP package. For the 144 QFP package drawings, refer to Figure 15 on page 42, Figure 16 on page 43, and Figure 17 on page 44.

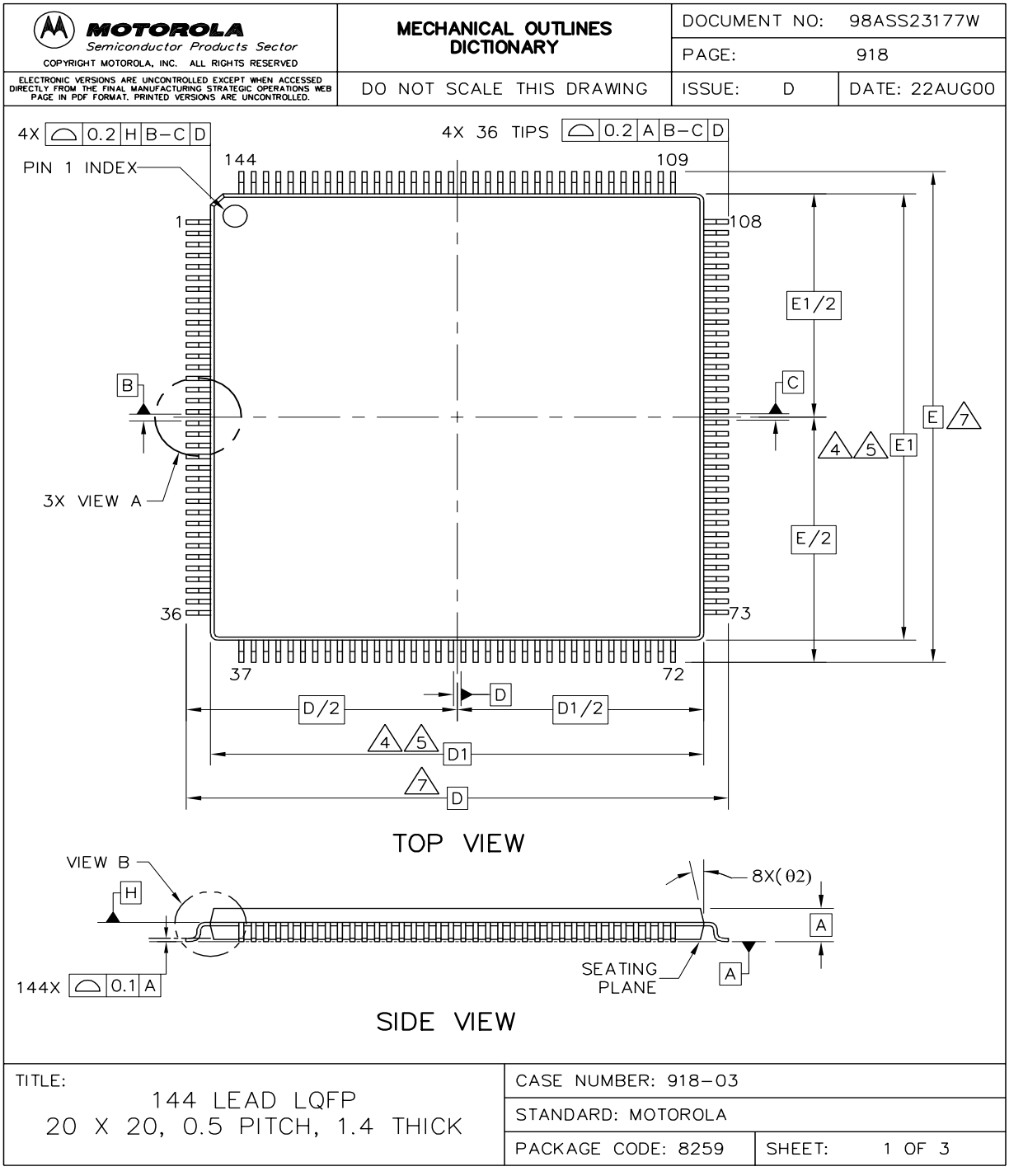

Figure 15. 144 QFP Package (1 of 3)

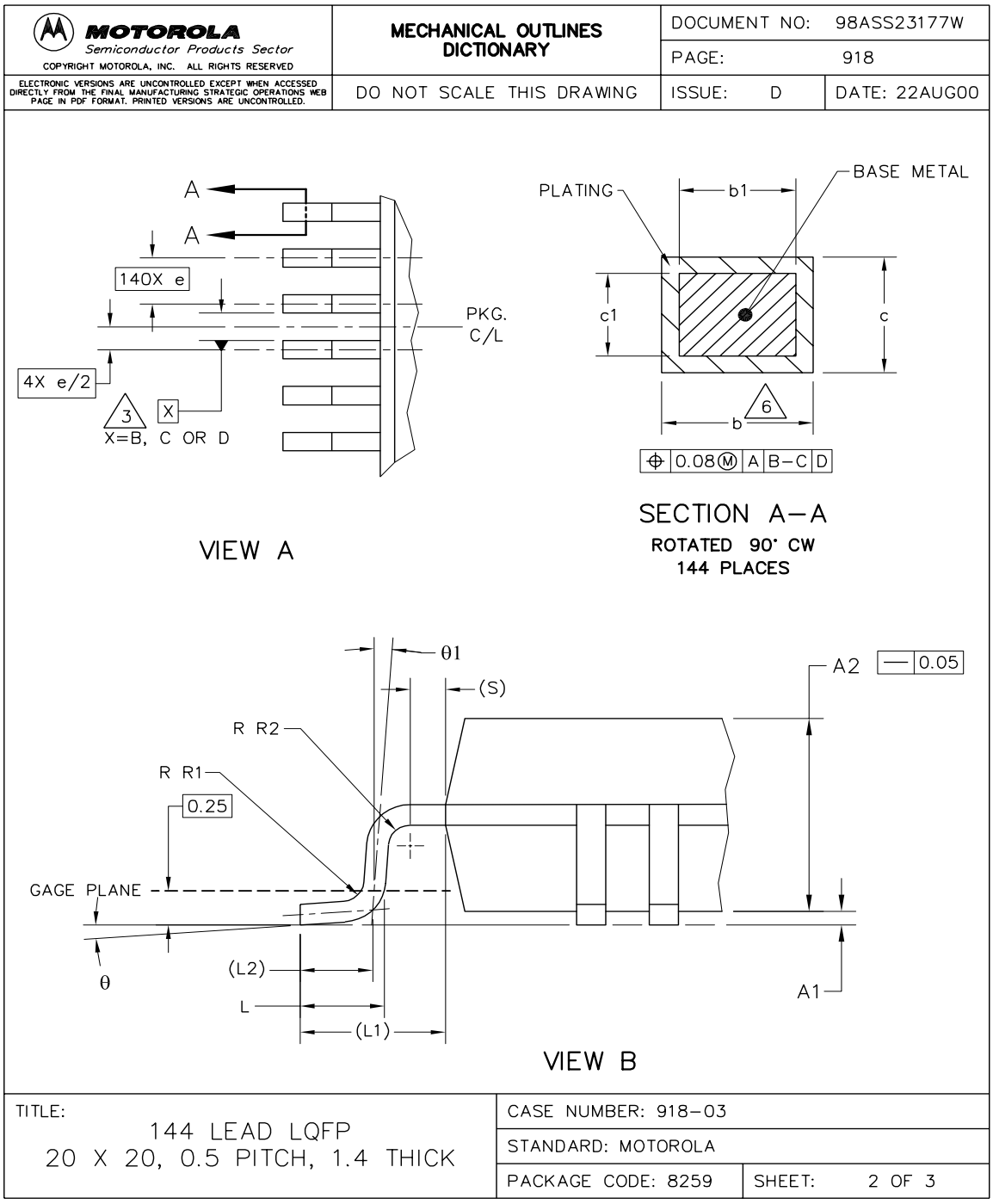

Figure 16. 144 QFP Package (2 of 3)

5.3 196 MAPBGA Pin Assignments

The SCF5250 can be assembled in a 196-pin MAPBGA package. Table 36 lists the 196 MAPBGA pin assignments.

Table 36. 196 MAPBGA Pin Assignments

MAPBGA Pin	Name	Type	Description	Pin State After Reset
B1	DATA16	I/O	Data	X
D3	A23_GPO54	I/O	SDRAM address / static adr	Out (requires pull up/down for boot-up selection
P_VDD	PST_VDD		PST_VDD	
C1	A22	O	SDRAM address / static adr	Out
D2	A21	O	SDRAM address / static adr	Out
E3	A20_A24	I/O	SDRAM address / static adr	Out (requires pull up/down for boot-up selection
D1	A19	O	SDRAM address / static adr	Out
E2	A18	O	SDRAM address / static adr	Out
P_GND	PST_GND		PST_GND	
F3	A17	O	SDRAM address / static adr	Out
E1	A16	O	SDRAM address / static adr	Out
F2	A15	O	SDRAM address / static adr	Out
F1	A14	O	SDRAM address / static adr	Out
G3	A13	O	SDRAM address / static adr	Out
P_VDD	PAD_VDD		PAD_VDD	
G2	A12	O	SDRAM address / static adr	Out
G1	A11	O	SDRAM address / static adr	Out
CORE_VDD	CORE_VDD		CORE_VDD	
C_GND	CORE_VSS		CORE_VSS	Out
H2	A10	O	SDRAM address / static adr	Out
J1	A9	O	SDRAM address / static adr	Out
H3	A8	O	SDRAM address / static adr	Out
K1	A7	O	SDRAM address / static adr	Out

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
J2	A6	O	SDRAM address / static adr	Out
L1	A5	O	SDRAM address / static adr	Out
P_GND	PAD_GND		PAD_GND	
J3	A4	O	SDRAM address / static adr	Out
K2	A3	O	SDRAM address / static adr	Out
L2	A2	O	SDRAM address / static adr	Out
M1	A1	O	SDRAM address / static adr	Out
K3	CS0	O	Static chip select 0	Out
L3	RWB	O	Bus write enable	Out
J5	OSCPAD_VDD		OSCPAD_VDD	
M2	CRIN		Crystal / external clock input	X
N1	CROUT		Crystal clock output	X
J6	OSCPAD_GND		OSCPAD_GND	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K5	PLLCORE_VDD		PLLCORE_VDD	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
K6	PLLCORE_GND		PLLCORE_GND	
M3	OE	O	Output enable	Out
M4	IDEDIOW_GP32	I/O	IDE DIOW	Out / High
M5	IDEIORDY_GP33	I/O	IDE interface IORDY	Out / Low
N3	IDEDIOR_GP31	I/O	IDE interface DIOR	Out / High
M6	BUFENB2_GP30	I/O	External Buffer 2 enable	Out / High
P2	BUFENB1_GP29	I/O	External Buffer 1 enable	Out / High
N4	TA_GP12	I/O	Transfer acknowledge	In (requires pull-up for normal operation)

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
N5	WAKEUP_GP21	I/O	Wake-up input	In (requires pull-up for normal operation)
P3	EBUIN2_SCLKOUT_GP13	I/O	Audio interfaces EBUIN2 / FlashMedia Clock	In / Low
P4	EBUIN3_CMDSDIO2_GP14	I/O	Audio interfaces EBUIN3 / FlashMedia Clock	In / Low
P_VDD	PAD_VDD	I/O	PAD_VDD	
N6	EBUIN1_GP36	I/O	Audio interfaces EBUIN1	In / Low
P5	EBUOUT1_GP37	I/O	Audio interfaces EBUOUT1	Out / Low
M7	XTRIM_GP0	I/O	Audio interfaces X-tal trim	Out / clock out
P6	QSPICS3_CS1_GP28	I/O	QSPI Chip select 3	Out / High
N7	RCK_QSPIDIN_QSPIDOUT_GP26	I/O	Subcode RCK interface / QSPI Data In / Data out	Out / Low
P7	QSPICLK_SUBR_GP25	I/O	QSPI clockpin / subcode interface	Out / Low
P8	QSPIDOUT_SFSY_GP27	I/O	QSPI Data Output / subcode interface SFSY	Out / Low
M8	QSPICS1_EBUOUT2_GP16	I/O	QSPI Chip select 1 output / audio interface EBU output 2	Out / Low
N8	QSPICS0_EBUIN4_GP15	I/O	QSPI Chip select 0 output / audio interface EBUIN4	Out / Low
P_GND	PAD_GND	I/O	PAD_GND	
P9	SCLK1_GP20	I/O	Audio interfaces serial clock 1	In / Low
M9	LRCK1_GP19	I/O	Audio interfaces word clock 1	In / Low
N9	SDATAO1_TOUT1_GP18	I/O	Audio interfaces serial data output 1 / Timer output 1	Out / Low
P10	SDATAI1_GP17	I/O	Audio interfaces serial data input 1	In / Low
N10	CFLG_GP5	I/O	CFLG input	In / Low
M10	EF_GP6	I/O	Error flag input	In / Low
P11	QSPICS2_MCLK2_GP24	I/O	QSPI Chip select output 2 / audio master clock output 2	Out / Low
N11	SDATAI3_GP8	I/O	Audio interfaces serial data input 3	In / Low

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
M11	ADIN0_GPI52	A	AD input 0	In only
P12	ADIN1_GPI53	A	AD input 1	In only
P13	ADIN2_GPI54	A	AD input 2	In only
N12	AD_VDD		AD_VDD	
M13	AD_GND		AD_GND	
M12	ADIN3_GPI55	A	AD input 3	In only
L12	ADIN4_GPI56	A	AD input 4	In only
K12	ADIN5_GPI57	A	AD input 5	In only
N13	ADREF	A	ADC reference input	In
N14	ADOUT_SCLK4_GP58	I/O	AD output / SCLK4 (for GPI function in low power applications	Out / clock output
L13	LRCK3_GP43	I/O	Audio interface LRCK3	In
M14	SCLK3_GP35	I/O	Audio interface SCLK3	In
J12	SCL_SDATA1BS1_GP41	I/O	I2C clock line / FlashMedia data interface	In / Low
L14	SDA_SDATA3_GP42	I/O	I2C data line / FlashMedia data interface	Hi-Z
J13	DDATA0_CTS2B_SDATA 0SDIO1_GP1	I/O	Debug / UART2 CTS / FlashMedia data interface	Out / High
K14	DDATA1_RTS2B_SDATA 2BS2_GP2	I/O	Debug / UART2 RTS / FlashMedia data interface	Out / High
H12	DDATA2_CTS1B_GP3	I/O	Debug / UART1 CTS	Out / High
J14	DDATA3_RTS1B_GP4	I/O	Debug / UART1 RTS	Out / High
H13	SCL2_TXD2_GP10	I/O	I2C2 clock line / second UART transmit data output	Out / Low
CORE_VDD	CORE_VDD	I/O	CORE_VDD	
C_GND	CORE_GND	I/O	CORE_GND	
H14	SDA2_RXD2_GP44	I/O	I2C2 data line / second UART2 receive data input	Hi-Z
P_VDD	PAD_VDD	I/O	PAD_VDD	
G14	TXD1_GP45	I/O	UART1 transmit data output	Out / High

Table 36. 196 MAPBGA Pin Assignments (continued)

MAPBGA Pin	Name	Type	Description	Pin State After Reset
G13	RXD1_GP46	I/O	UART1 receive data input	Out / Low
G12	PST3_INTMON1_GP47	I/O	Debug / interrupt monitor output 1	Out / High
F12	PST2_INTMON2_GP48	I/O	Debug / interrupt monitor output 2	Out / High
P_GND	PAD_GND	I/O	PAD_GND	
F14	PST1_GP49	I/O	Debug	Out / High
F13	PST0_GP50	I/O	Debug	Out / High
E14	PSTCLK_GP51	I/O	Debug	Out / clock output
E13	TDO_DSO	O	JTAG / Debug	BDM
D13	TDI_DSI	I	JTAG / Debug	BDM
E12	TCK	I	JTAG	BDM
C13	TMS_BKPT	I	JTAG / Debug	BDM
D12	TRST_DSCLK	I	JTAG / Debug	BDM
D14	RSTI	I	Reset	X
C14	SCLK2_GP22	I/O	Audio interfaces serial clock 2	In / Low
B14	LRCK2_GP23	I/O	Audio interfaces word clock 2	In / Low
C11	LINOUT	A	Linear regulator output	X
C11	LINOUT	A	Linear regulator output	X
B12	LININ	A	Linear regulator input	X
B12	LININ	A	Linear regulator input	X
P_GND	LIN_GND		Linear regulator ground	X
C10	SDATAO2_GP34	I/O	Audio interfaces serial data output 2	Out / Low
A12	MCLK1_GP11	I/O	Audio master clock output 1	Out / clock output
---	VBGT			
B11	HIZ_B	I	JTAG	X
B10	TEST2	I	Test	X
C9	TEST1	I	Test	X
A11	TEST0	I	Test	X

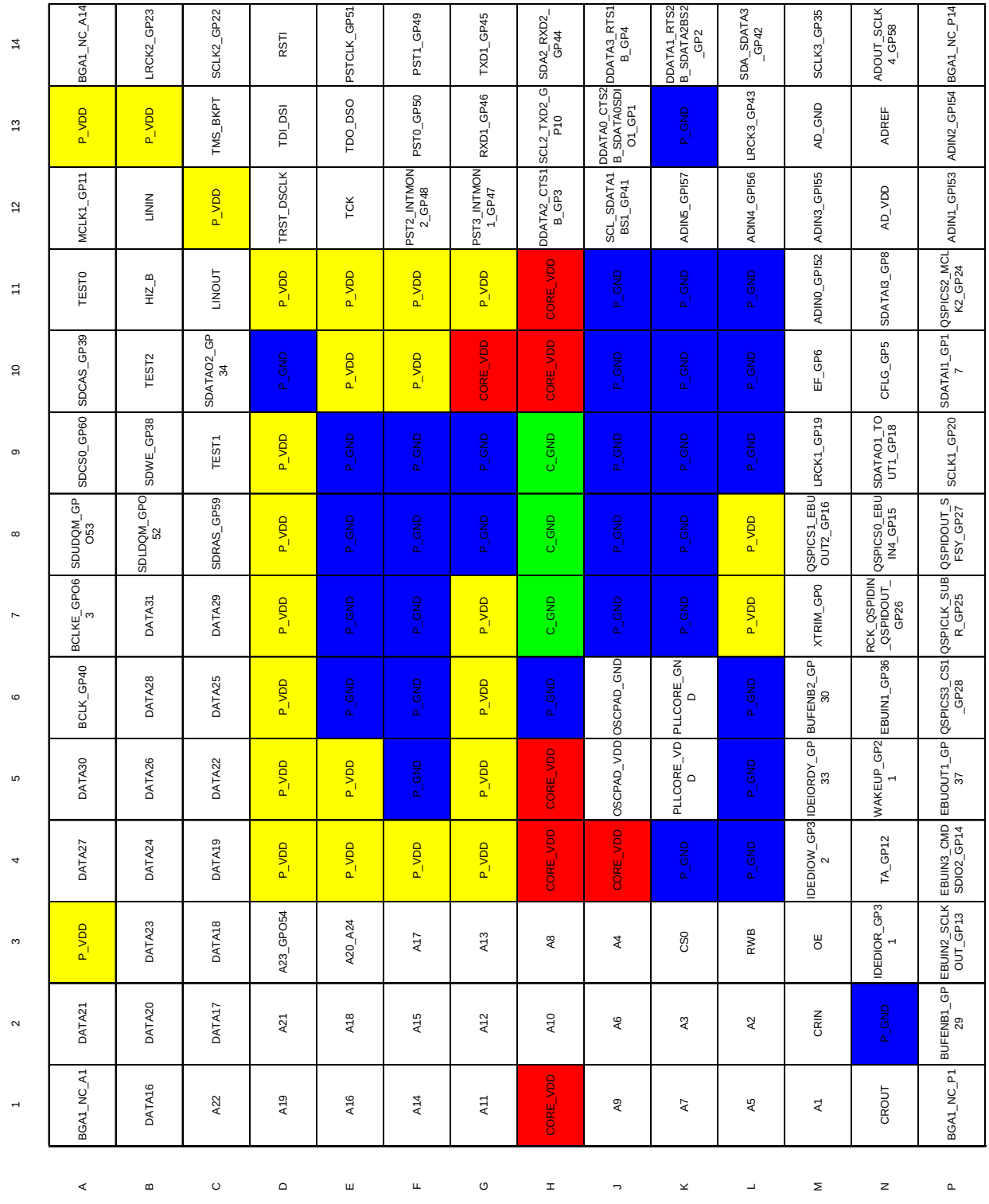

Figure 20. 196 MAPBGA Ball Map

How to Reach Us:

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E-mail:
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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
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