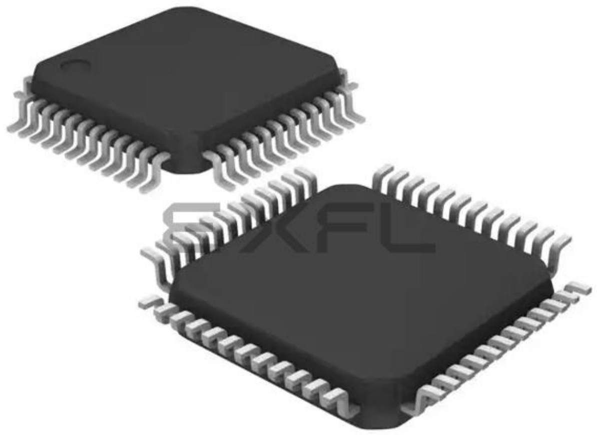

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

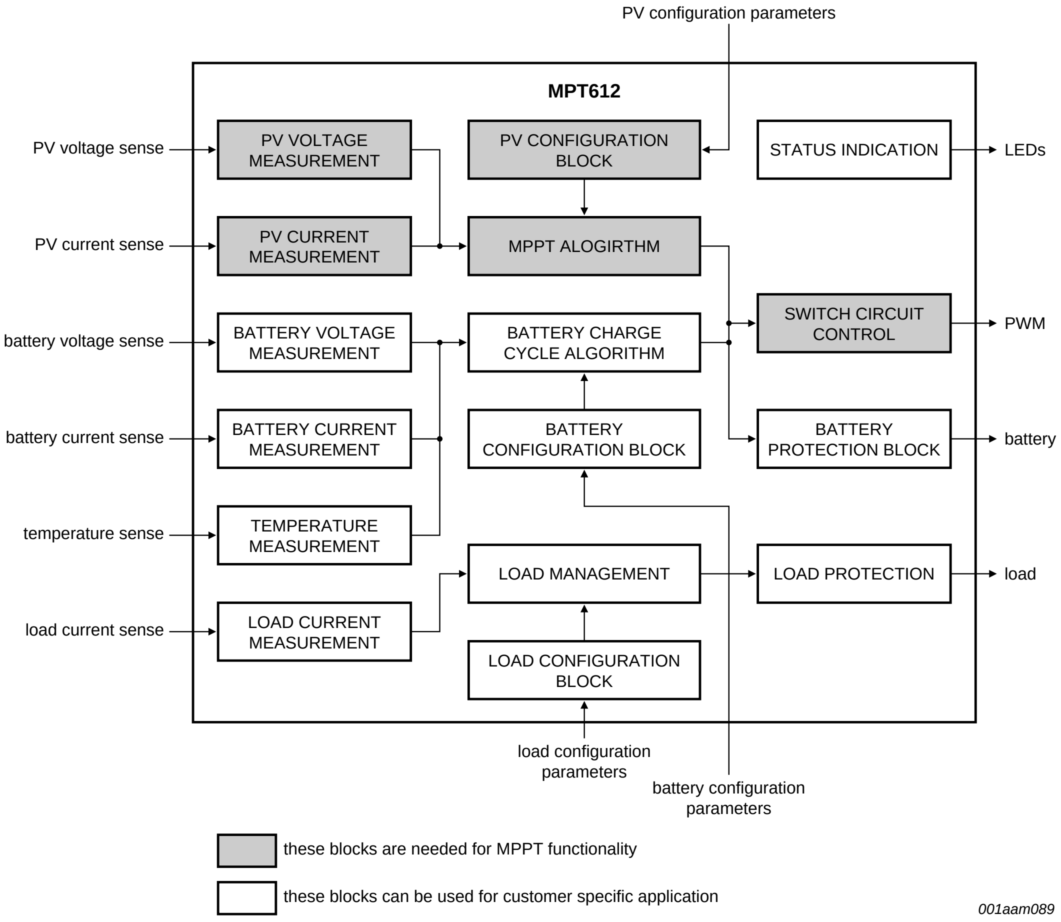
Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	70MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	PWM, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpt612fbd48-151

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MPT612FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5. Block diagram



The configuration parameters are determined using the software

Fig 1. Block diagram

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Symbol	Pin	Type	Description
PIO11/CTS1/CAP1_1/AD4	36[3]	I/O	**PIO11:** general purpose digital input and output pin
		I	**CTS1:** Clear To Send input for UART1
		I	**CAP1_1:** capture input for Timer 1, channel 1
		I	**AD4:** analog-to-digital converter input 4
PIO12/DSR1/MAT1_0/AD5	37[3]	I/O	**PIO12:** general purpose digital input and output pin
		I	**DSR1:** Data Set Ready input for UART1
		O	**MAT1_0:** PWM output for timer 1, channel 0
		I	**AD5:** analog-to-digital converter input 5
PIO13/DTR1/MAT1_1	41[1]	I/O	**PIO13:** general purpose digital input and output pin
		O	**DTR1:** Data Terminal Ready output for UART1
		O	**MAT1_1:** PWM output for timer 1, channel 1
PIO14/DCD1/SCK1/EINT1	44[4][5]	I/O	**PIO14:** general purpose digital input and output pin
		I	**DCD1:** Data Carrier Detect input for UART1
		I/O	**SCK1:** serial clock for SPI1; SPI clock output from master or input to slave
		I	**EINT1:** external interrupt input 1
PIO15/RI1/EINT2	45[4]	I/O	**PIO15:** general purpose digital input and output pin
		I	**RI1:** ring indicator input for UART1
		I	**EINT2:** external interrupt input 2
PIO16/EINT0	46[4]	I/O	**PIO16:** general purpose digital input and output pin
		I	**EINT0:** external interrupt input 0
PIO17/CAP1_2/SCL1	47[6]	I/O	**PIO17:** general purpose digital input and output pin; the output is not open-drain
		I	**CAP1_2:** capture input for timer 1, channel 2
		I/O	**SCL1:** I^{2}C-bus port 1 clock Input and output; open-drain output if I^{2}C1 function is selected on the pin connect block
PIO18/CAP1_3/SDA1	48[6]	I/O	**PIO18:** general purpose digital input and output pin; the output is not open-drain
		I	**CAP1_3:** capture input for timer 1, channel 3
		I/O	**SDA1:** I^{2}C-bus port 1 data Input and output; open-drain output if I^{2}C1 function is selected on the pin connect block
PIO19/MAT1_2/MISO1	1[1]	I/O	**PIO19:** general purpose digital input and output pin.
		O	**MAT1_2:** PWM output for timer 1, channel 2
		I/O	**MISO1:** Master In Slave Out for SSP; data input to SSP master or data output from SSP slave.
PIO20/MAT1_3/MOSI1	2[1]	I/O	**PIO20:** general purpose digital input and output pin
		O	**MAT1_3:** PWM output for timer 1, channel 3
		I/O	**MOSI1:** Master Out Slave for SSP; data output from SSP master or data input to SSP slave
PIO21/SSEL1/MAT3_0	3[1]	I/O	**PIO21:** general purpose digital input and output pin
		I	**SSEL1:** slave select for SPI1; selects the SPI interface as a slave
		O	**MAT3_0:** PWM output for timer 3, channel 0
PVVOLTSENSEBUCK	32[3]	I	PV Voltage sense for buck mode

Symbol	Pin	Type	Description
PVVOLTSENSEBOOST	33[3]	I	PV Voltage sense for boost mode; this pin is not connected when only buck mode is used
PVCURRENTSENSE	34[3]	I	PV Current sense.
PIO25/AD6	38[3]	I/O	**PIO25:** general purpose digital input and output pin.
		I	**AD6:** analog-to-digital converter input 6
PIO26/AD7	39[3]	I/O	**PIO26:** general purpose digital input and output pin
		I	**AD7:** analog-to-digital input 7
PIO27/ $\overline{\text{TRST}}$	8[1]	I/O	**PIO27:** general purpose digital input and output pin
		I	$\overline{\text{TRST}}$: Test Reset for the JTAG interface[6]
PIO28/TMS	9[1]	I/O	**PIO28:** general purpose digital input and output pin.
		I	**TMS:** Test Mode Select for the JTAG interface[6]
PIO29/TCK	10[1]	I/O	**PIO29:** General purpose input/output digital pin.
		I	**TCK:** Test Clock for the JTAG interface[6] This clock must be slower than $^{1}/_{6}$ of the CPU clock (CCLK) for the JTAG interface to operate
PIO30/TDI/MAT3_3	15[1]	I/O	**PIO30:** general purpose digital input and output pin
		I	**TDI:** Test Data In for JTAG interface[6]
		O	**MAT3_3:** PWM output 3 for timer 3
PIO31/TDO	16[1]	O	**PIO31:** general purpose digital output pin
		O	**TDO:** Test Data Out for JTAG interface[6]
RTCX1	20[8][9]	I	RTC oscillator circuit input; the input voltage must not exceed 1.8 V
RTCX2	25[8][9]	O	RTC oscillator circuit output
RTCK	26[8]	I/O	Returned test clock output; bidirectional pin with internal pull-up; extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies
XTAL1	11	I	oscillator and internal clock generator circuit input; the input voltage must not exceed 1.8 V
XTAL2	12	O	oscillator amplifier output
JTAGSEL	27	I	JTAG interface select; input with internal pull-down: when LOW, the device operates normally when externally pulled HIGH at reset, PIO27 to PIO31 are configured as JTAG port and the part is in Debug mode
$\overline{\text{RST}}$	6	I	external reset input; TTL with hysteresis; 5 V tolerant when LOW, this pin resets the device; all I/O ports and peripherals return to their default states and processor execution will begin at address 0x00
GND	7,19,43	I	ground; 0 V reference
GNDADC	31	I	analog ground 0 V reference; nominally the same voltage as GND but should be isolated to minimize noise and error
$V_{DD(ADC)}$	42	I	analog 3.3 V power supply; nominally the same voltage as $V_{DD(IO)}$ but should be isolated to minimize noise and error; the level on this pin provides the ADC voltage reference level
V_{DDC}	5	I	1.8 V core power supply; internal circuitry and on-chip PLL power supply voltage

7.4 Memory map

The MPT612 memory map incorporates several distinct regions, as shown in Fig 3. In addition, the CPU interrupt vectors can be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM.

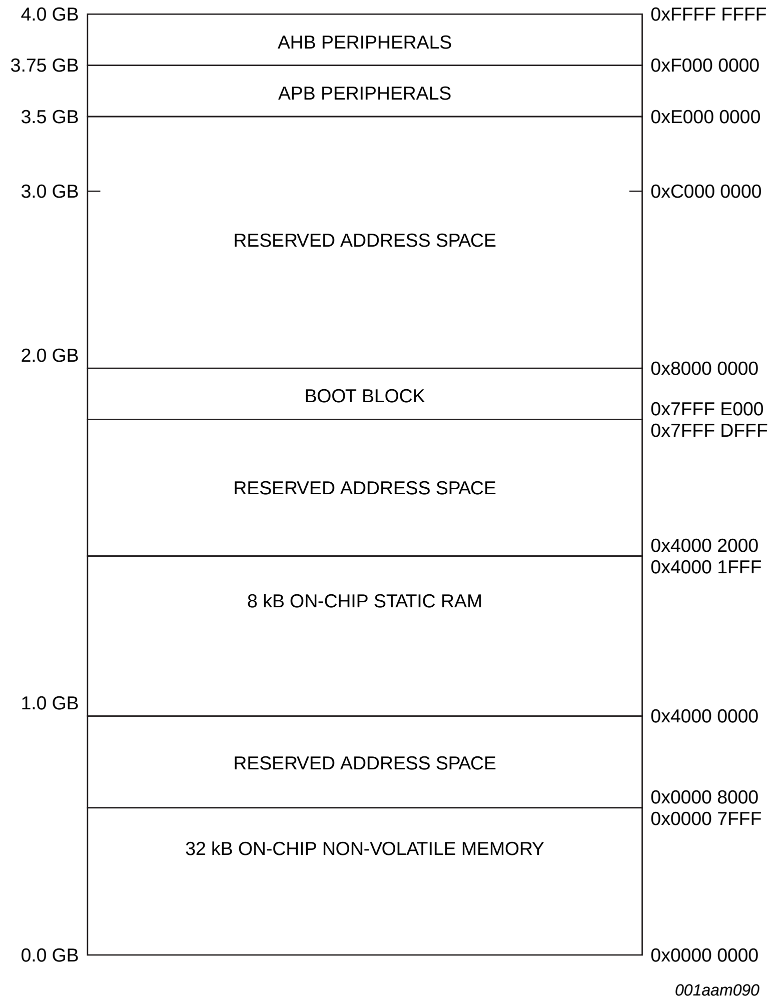

Fig 3. System Memory Map

7.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as FIQ, vectored IRQ and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ because the FIQ service routine does not need to branch into the interrupt service routine but can run

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from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine reads a word from the VIC that identifies which FIQ sources are requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots. Slot 0 has the highest priority and slot 15 has the lowest priority.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to generate the IRQ signal for the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping to it. If any vectored IRQs are pending, the VIC provides the address of the highest priority requesting IRQs service routine, otherwise it provides the address of a default routine which is shared by all the non-vectored IRQs. The default routine can read another VIC register to see which IRQs are active.

7.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the VIC which can contain several internal interrupt flags. Each individual interrupt flag can represent more than one interrupt source.

7.6 Pin connect block

The pin connect block enables selected device pins to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins before being activated and any related interrupt(s) are enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The pin control module with its pin select registers defines the functionality of the processor core in a given hardware environment.

After reset, all pins of PIO are configured as inputs with the following exception:

- If the JTAGSEL pin is HIGH (Debug mode enabled), the JTAG pins will assume their JTAG functionality for use with EmbeddedICE and cannot be configured via the pin connect block.

7.7 Fast general purpose parallel I/O

Pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins can be dynamically configured as inputs or outputs. Separate registers allow simultaneous setting or clearing any number of outputs. The value of the output register and the state of the port pins can be read back. The GPIO provides the following features:

- GPIO registers are relocated for the fastest possible I/O timing
- Mask registers allow sets of port bits to be treated as a group, leaving other bits unchanged
- All GPIO registers are byte addressable
- Entire port value can be written in one instruction
- Bit level set and clear registers allow a single instruction setting or clearing of any number of bits on one port
- Direction control of individual bits

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- Separate control of output set and clear
- All I/O default to inputs after reset

7.8 10-bit ADC

The MPT612 contains one Analog-to-Digital Converter (ADC). It is a single 10-bit successive approximation ADC with eight channels, three of which are used internally. The ADC provides the following features:

- Measurement range from 0 V to 3.3 V
- The converter can perform more than 400 000 10-bit samples per second
- Burst conversion mode for single or multiple inputs
- Optional conversion on input pin transition or Timer Match signal
- Every analog input has a dedicated result register to reduce interrupt overhead

7.9 UARTs

The MPT612 contain two UARTs. In addition to standard transmit and receive data lines UART1 also provides a full modem control handshake interface. The UARTs in MPT612 include a fractional baud rate generator for both UARTs. Standard baud rates such as 115200 can be achieved with any crystal frequency above 2 MHz. The UARTs provide the following features:

- 16-byte receive and transmit FIFOs
- Register locations conform to 16C550 industry standard
- Receiver FIFO trigger points at 1-byte, 4-byte, 8-byte and 14-byte
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals
- Transmission FIFO control enables implementation of software flow control (XON/XOFF) on both UARTs
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS)

7.10 I^{2}C-bus serial I/O controllers

The MPT612 contains two I^{2}C-bus controllers.

The I^{2}C-bus is bidirectional, 2-wire interface providing the Serial Clock Line (SCL) and the Serial DAta line (SDA). Each I^{2}C-bus device is recognized by a unique address and can operate as either a receiver-only device (e.g., LCD driver) or a transmitter with the capability to both receive and send information such as serial memory. Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus is a multi-master bus; it can be controlled by more than one bus master connected to it.

The I^{2}C-bus implemented in the MPT612 supports bit rates up to 400 kbit/s (Fast I^{2}C-bus). The controller provides the following features:

- Compliant with standard I^{2}C-bus interface specification
- Easy to configure as master, slave or master/slave
- Programmable clocks allow versatile rate control
- Bidirectional data transfer between masters and slaves

7.17.4 Code security (Code Read Protection)

The MPT612's Code Read Protection (CRP) feature allows users to restrict access to the on-board flash, JTAG and ISP using different levels of security. When needed, CRP is activated by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

Three levels of the CRP are implemented in boot loader code:

- **CRP1:** disables access to chip via the JTAG pins and allows partial flash updates (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased
- **CRP2:** disables access to chip via the JTAG pins and only allows full flash erase and update using a reduced set of the ISP commands
- **CRP3:** Running an application with this level fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using PIO14 pin. It is up to the user's application to provide a flash update mechanism (if needed) using IAP calls or call the re-invoke ISP command to enable flash update via pin UART0.

CAUTION

⚠ If Code Read Protection level three (CRP3) is selected, no future factory testing can be performed on the device.

7.17.5 External interrupt inputs

The MPT612 includes up to three edge or level sensitive external interrupt inputs as selectable pin functions. When the pins are combined, external events can be processed as three independent interrupt signals. Optionally, the external interrupt inputs can be used to wake-up the processor from Power-down mode and Deep power-down mode.

In additional, all 10 capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

7.17.6 Memory mapping control

The memory mapping control changes the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors can be mapped to the bottom of the on-chip flash memory or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

7.17.7 Power control

The MPT612 supports three reduced power modes: Idle mode, Power-down mode and Deep power-down mode.

In Idle mode, execution of instructions is suspended until a reset or interrupt is received. Peripheral functions continue operation in Idle mode and can generate interrupts which cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clock signals. The processor state and registers, peripheral registers and internal SRAM

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values are preserved throughout Power-down mode. In addition, the logic levels of chip output pins remain static. Power-down mode can be exited and normal operation resumed by either a reset or via specific interrupts that function without clock signals. Power-down mode reduces chip power consumption to nearly zero because all dynamic device operation is suspended.

Selecting an external 32 kHz clock instead of the PCLK as the clock-source for the on-chip RTC enables the core to keep the RTC active during Power-down mode. Power-down current is increased when the RTC is active. However, the current consumption is significantly lower than that in Idle mode.

In Deep-power down mode, all power is removed from the internal chip logic except for the RTC module, the I/O ports, the SRAM and the 32 kHz external oscillator. Additional power savings are provided when SRAM and the 32 kHz oscillator are powered down individually. Deep power-down mode has the lowest possible power consumption without removing power from the entire chip. In Deep power-down mode, the contents of registers and memory are not preserved except for SRAM (if selected) and three general purpose registers. To resume operation, a full chip reset is required.

To conserve battery power, a power selector module switches the RTC power supply from $V_{DD(RTC)}$ to V_{DDC} whenever the core voltage is present on pin V_{DDC}.

A power control feature for peripherals enables individual peripherals to be turned off when they are not needed in the application. This results in additional power savings during Active and Idle modes.

7.17.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used for peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via the APB divider so that they can operate at the chosen ARM processor speed. In order to achieve this, the APB divider may be slowed down to between 50 % and 25 % of the processor clock rate. The default condition on reset is the APB divider running at 25 % of the processor clock rate. This is because the APB divider must work correctly during power-up (and its timing cannot be altered if it does not work since its control registers reside on the APB). The second purpose of the APB divider is to allow power saving when an application does not require any peripherals running at the full processor rate. The PLL remains active (if it was running) during Idle mode because the APB divider is connected to the PLL output.

7.17.9 Emulation and debugging

The MPT612 supports emulation and debugging using the JTAG serial port.

7.17.10 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. Debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the remote debug protocol commands to the JTAG data needed for accessing the ARM core.

The ARM core contains a built-in a debug communication channel function. The debug communication channel allows a program running on the target system to communicate with the host debugger/another host without stopping the program flow or entering the debug state.

The debug communication channel is accessed as coprocessor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic. The JTAG clock (TCK) must be slower than $^1/_6$ of the CPU clock (CCLK) to enable the JTAG interface to operate.

7.17.11 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc. which enables real time debugging. It is a lightweight debug monitor that runs in the background while users debug the foreground application. It communicates with the host using DCC which is present in the EmbeddedICE logic. The MPT612 contain a specific configuration of RealMonitor software programmed into the on-chip boot ROM memory.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDC}	core supply voltage	typical: 1.8 V	[1]b)	–0.5	+2.5	V
$V_{DD(IO)}$	input/output supply voltage	typical: 3.3 V	[2]	–0.5	+4.6	V
$V_{DD(ADC)}$	ADC supply voltage	pad supply: 3.3 V		–0.5	+4.6	V
$V_{DD(RTC)}$	RTC supply voltage			–0.5	+4.6	V
V_{IA}	analog input voltage		[3]	–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][5]	–0.5	$V_{DD(IO)}$ + 0.5[6]	V
I_{DD}	supply current		[7]	-	100[8]	mA
I_{SS}	ground current		[9]	-	100[8]	mA
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)	[[11]	–4000	+4000	V
		Machine Model (MM)	[12]	–200	+200	V
		Charged Device Model (CDM)	[13]	–800	+800	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

b) Core and internal rail

[2] External rail

[3] On ADC related pins

[4] Including voltage on outputs in 3-state mode

[5] Only valid when the $V_{DD(IO)}$ supply voltage is present

[6] Not to exceed 4.6 V

[7] Per supply pin

[8] The peak current is limited to 25 times the corresponding maximum current

[9] Per ground pin

[10] Dependent on package type

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[11] Performed per AEC-Q100-002

[12] Performed per AEC-Q100-003

[13] Performed per AEC-Q100-011

9. Static characteristics

Table 4. Static characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDC}	core supply voltage		[2]	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage		[3]	2.6[4]	3.3	3.6	V
$V_{DD(ADC)}$	ADC supply voltage	pad supply		2.6[5]	3.3	3.6	V
$V_{DD(RTC)}$	RTC supply voltage			2.0[6]	3.3	3.6	V
Standard port pins, $\overline{\text{RST}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	mA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; no pull-down		-	-	3	mA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(IO)}$; no pull-up or pull-down		-	-	3	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)}$ and $V_{DD(ADC)} \geq 3$ V	[7][8][9]	0	-	5.5	V
		pin configured to provide a digital function; $V_{DD(IO)}$ and $V_{DD(ADC)} < 3$ V	[7][8][9]	0	-	$V_{DD(IO)}$	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			2	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -4$ mA		$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = -4$ mA	[10]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V	[10]	–4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[11]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(ADC)}$	[11]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[12]	10	50	150	mA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		0	-	1.8	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and internal rail.

[3] External rail.

[4] If $V_{DD(IO)} < 3.0$ V, the I/O pins are not 5 V tolerant and the ADC input voltage is limited to $V_{DD(ADC)} = 3.0$ V.

[5] If $V_{DD(ADC)} < 3.0$ V, the I/O pins are not 5 V tolerant.

[6] The RTC typically fails when $V_{DD(RTC)}$ drops below 1.6 V.

[7] Including voltage on outputs in 3-state mode.

[8] $V_{DD(IO)}$ supply voltages must be present.

[9] 3-state outputs go into 3-state mode when $V_{DD(IO)}$ is grounded.

[10] Accounts for 100 mV voltage drop in all supply lines.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] Minimum condition for $V_I = 4.5$ V, maximum condition for $V_I = 5.5$ V. $V_{DD(ADC)} \geqq 3.0$ V and $V_{DD(IO)} \geqq 3.0$ V.

[13] Applies to PIO25:16.

[14] Battery supply current on pin $V_{DD(RTC)}$.

[15] Input leakage current to GND.

Table 5. ADC Static Characteristics

$V_{DD(ADC)} = 2.5$ V to 3.6 V; $T_{amb} = -40$ °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	$V_{DD(ADC)}$	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	[1][2][4]	-	-	±2	LSB
E_O	offset error	[1][5]	-	-	±3	LSB
E_G	gain error	[1][6]	-	-	±0.5	%
E_T	absolute error	[1][7]	-	-	±4	LSB

[1] Conditions: GNDADC = 0 V, $V_{DD(ADC)} = 3.3$ V and $V_{DD(IO)} = 3.3$ V for 10-bit resolution at full speed; $V_{DD(ADC)} = 2.6$ V, $V_{DD(IO)} = 2.6$ V for 8-bit resolution at full speed.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Fig 4.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Fig 4.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Fig 4.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error and the straight line which fits the ideal transfer curve. See Fig 4.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Fig 4.

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10. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 0 ℃ to 70 ℃ for commercial applications, -40 ℃ to +85 °℃ for industrial applications, V_{DDC}, $V_{DD(IO)}$ over ranges[1]

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
External clock							
f_{osc}	oscillator frequency			10	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	100	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns
Port pins (except PIO2 and PIO3)							
$t_{r(o)}$	output rise time			-	10	-	ns
$t_{f(o)}$	output fall time			-	10	-	ns
I^2C-bus pins (PIO2 and PIO3)							
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	[1][2][3]	$20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

11. Application information

11.1 XTAL1 input

The input voltage to the on-chip oscillators is limited to 1.8 V. When the oscillator is driven by a clock in slave mode, it is recommended that the input is coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, an additional capacitor connected to ground (C_g), attenuates the input voltage by a factor C_i / (C_i + C_g). In slave mode, a minimum input voltage of 200 mV (RMS) is needed.

11.1.1 XTAL and RTC Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the device’s oscillator input and output pins. The load capacitors Cx1 and Cx2 and Cx3, in case of third overtone crystal usage, must have a common ground plane. In addition, the external components must also be connected to the ground plain.

Any loops must be made as small as possible to keep the noise coupled and parasitics in via the PCB as small as possible. The values of Cx1 and Cx2 should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

The MPT612 IC can be used with accompanying software only. The MPT612 software stack is designed to cater to different types of applications in the solar PV domain ranging from simple MPPT charge controller to advanced systems on street lighting applications to micro-inverters and DC-DC converters per panel.

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12. MPT612 software overview

The MPT612 IC can only be used with accompanying software. The MPT612 software stack is designed to meet the needs of different solar PV domain applications ranging from MPPT charge controllers to advanced street lighting system applications.

- Scalable software modules. Only those modules that are developed and tested are included in the final application image
- Implementation of the MPPT algorithm (patent pending) for generating maximum power from photovoltaic panel
- Easy to implement APIs for use with a range of peripherals ensure fast application programming
- Easy configuration for use with any PV panel
- Easy configuration for use with any battery (up to 4 stage charging cycle)
- Available for different IDE tools
- Up to 15 kB of flash memory available for application software
- Data logging capability through external memory
- Complies with industry standard MISRA guidelines
- Context-based API reference manual (included in the MPT612 user manual)
- Distributed as libraries (object files) can be linked to application

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12.1 Architecture

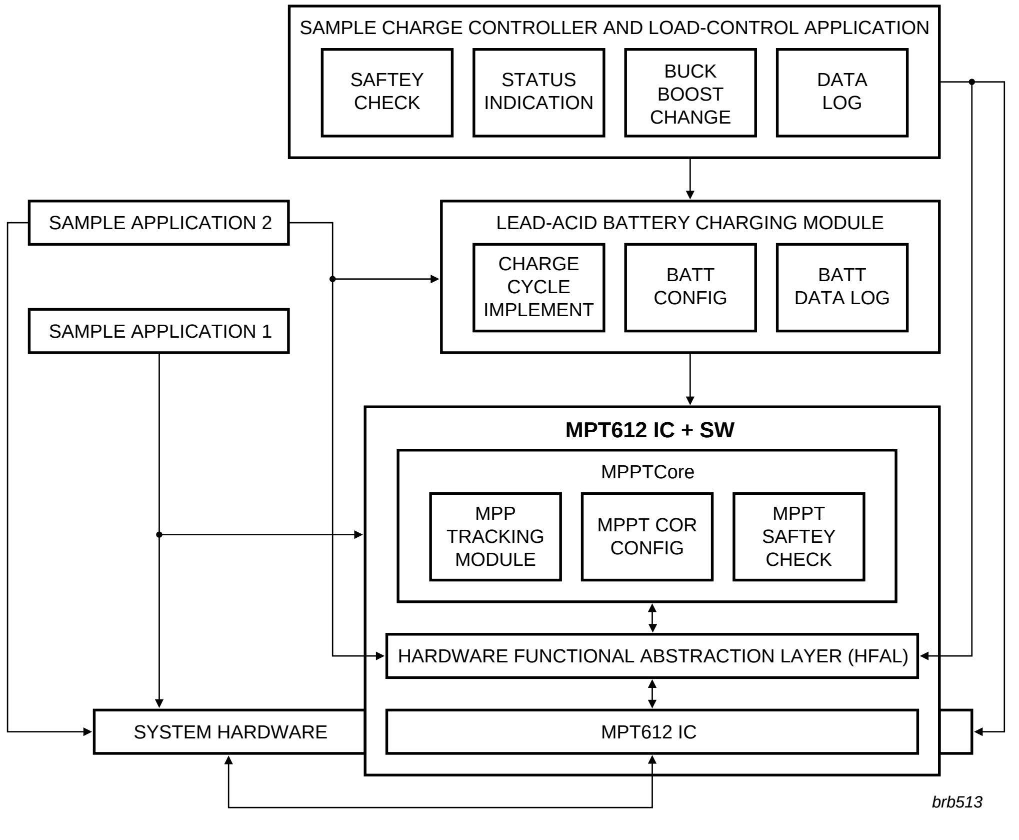

Fig 5. MPT612SW Architecture

12.2 MPT612 software modules

This module consists of two sub modules: Hardware Functional Abstraction Layer (HFAL) and MPPTCore. Both these sub modules are delivered as software libraries together with the MPT612 IC. It is mandatory to use these modules to access the MPT612’s MPPT functionality.

12.2.1 Hardware Functional Abstraction Layer (HFAL)

This module contains the functional abstraction of different peripherals that are of interest to the application layer as well as different modules of MPT612 software. This layer contains mini kernel functionality such as implementations of a round-robin scheduler, task creation and software timers. These functions are useful during development of applications based on the MPT612.

A range of different peripherals used in the application, such as PWM, Interrupts, software timers, GPIO, UART and Flash can be accessed using this module. In addition, utilities for logging the data onto the flash and printing the messages onto the console screen are accessed from this layer.

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12.2.2 MPPTCore module

This module contains the Maximum PowerPoint Tracking (MPPT) algorithm. This algorithm continuously tracks the maximum power point of the PV panel and makes the system to operate at the MPP which ensures the maximum power is generated from the PV. This module supports the well documented APIs that aid in application programming. Typical module functionality includes, starting the MPP tracking algorithm, enabling/disabling the MPP tracking algorithm and retrieving logged parameters from the MPPTCore module.

12.3 Lead-Acid battery charging module

This is an optional software library provided along with the MPT612 IC. This module implements the lead-acid battery charge cycle for 2-stage, 3-stage and 4-stage batteries. Using the easy configuration for the battery parameters and well documented APIs, the user can design an application with ease. This module together with the MPT612SW will help in the creation of power management systems for battery charging for home and street lighting applications.

12.4 Sample charge controller and load control application

This module implements the sample charge controller and load control application for the specification of the MPT612 reference board. It uses features of the MPT612SW and lead-acid battery charging module to implement a typical charge controller application.

12.5 Sample applications

Using MPT612SW and lead-acid battery charging module, solutions for several applications can be generated such as:

- dusk-to-dawn lighting applications
- street lighting applications
- traffic lighting applications
- solar based mobile chargers
- DC-DC converters in panels
- micro inverters.

In the SW architecture diagram shown in Fig 5, SampleApplication1 will interact directly with MPPTCore module to extract the maximum power which can use a micro-inverter, to feed it to the grid. SampleApplication2 utilizes the services of the battery charging algorithm to charge the battery and can be used to control different lighting applications.

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13. MPT612SW interfaces

13.1 Hardware Functional Abstraction Layer interfaces

Table 7. HFAL Interfaces

Interface	Description
nxLibMpt_Hfal_Irq_InstallHandler	installs the interrupt handler for the IRQ mentioned
nxLibMpt_Hfal_Irq_FreeHandler	frees the interrupt handler installed using nxLibMpt_Hfal_Irq_InstallHandler
nxLibMpt_Hfal_Irq_Enable	enables the interrupt associated with an IRQ
nxLibMpt_Hfal_Irq_Disable	disables the interrupt associated with an IRQ
nxLibMpt_Hfal_Irq_SetPriority	sets the priority of the interrupt associated with an IRQ
nxLibMpt_Hfal_Irq_GetPriority	reads the priority of the interrupt associated with an IRQ
nxLibMpt_Hfal_Irq_SaveFlags	saves the current interrupt enable state and disables the interrupts
nxLibMpt_Hfal_Irq_RestoreFlags	restores the previous interrupt state (enable/disable)
nxLibMpt_Hfal_Schedular_RestoreFlags	restores the previous scheduler state (enable/disable)
nxLibMpt_Hfal_Schedular_SaveFlags	saves the current scheduler state and then disables the scheduler
nxLibMpt_Hfal_Task_Create	creates a task with given round-robin time slice in ticks
nxLibMpt_Hfal_Timer_Create	creates a software timer and returns the timer ID
nxLibMpt_Hfal_Timer_Delete	deletes the created software timer
nxLibMpt_Hfal_Timer_CheckTimeOut	checks if the software timer is running and triggers it, when necessary
nxLibMpt_Hfal_Timer_Start	starts the software timer
nxLibMpt_Hfal_Timer_Stop	stops the software timer
nxLibMpt_Hfal_Timer_Delay	delays the execution till the specified timeout elapses
nxLibMpt_Hfal_Timer_SetTimeOut	sets the timeout value for the software timer
nxLibMpt_Hfal_Timer_GetTimeOut	reads the current timeout value of the software timer
nxLibMpt_Hfal_Pwm_Init	initializes the PWM unit
nxLibMpt_Hfal_Pwm_SetDutyCycle	sets the duty cycle of the PWM pin
nxLibMpt_Hfal_Pwm_GetDutyCycle	reads the current duty cycle of the PWM pin
nxLibMpt_Hfal_Pwm_SetCount	sets the duty cycle count of the specified PWM pin
nxLibMpt_Hfal_Pwm_GetCount	reads the current duty cycle count of the specified PWM pin
nxLibMpt_Hfal_Gpio_Init	initializes the GPIO pin direction (input/output)
nxLibMpt_Hfal_Gpio_SetValue	sets the value of the GPIO pin to the entered value
nxLibMpt_Hfal_Gpio_GetValue	reads the current value of the GPIO pin
nxLibMpt_Hfal_Flash_Erase	erases the flash blocks
nxLibMpt_Hfal_Flash_Read	reads the data from the specified flash address
nxLibMpt_Hfal_Flash_Write	data is written to the specified flash address
nxLibMpt_Hfal_DataLog_Init	initializes the data logging module
nxLibMpt_Hfal_DataLog_ReadData_Latest	reads the recent data that is logged
nxLibMpt_Hfal_DataLog_WriteData	writes the log data to the flash
nxLibMpt_Hfal_Adc_ReadCounts	reads the ADC channel and returns the counts corresponding to the incoming signal
nxLibMpt_Hfal_Uart_Init	initializes the console UART port at the specified frequency
nxLibMpt_Hfal_Uart_WriteByte	writes a byte to the UART console

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13.3 Lead-acid battery charging module interfaces

Table 9. MPPTCore Interfaces

Interface	Description
nxLibMpt_Batla_Init	initializes the lead-acid battery charging module with the battery configuration parameters
nxLibMpt_Batla_SetParams	sets the parameters required in lead-acid battery charging module
nxLibMpt_Batla_GetParams	reads the current parameters stored in lead-acid battery charging module
nxLibMpt_Batla_GetLogParams	reads the logged parameters in lead-acid battery charging module
nxLibMpt_Batla_Start	starts the lead-acid battery charging algorithm
nxLibMpt_Batla_Enable	enables the lead-acid battery charging algorithm
nxLibMpt_Batla_Disable	disables the lead-acid battery charging algorithm
nxLibMpt_Batla_IsEnabled	returns the status of lead-acid battery charging algorithm enabled or disabled
nxLibMpt_Batla_GetStatus	reads the status of the lead-acid battery charging module

13.4 Interfaces to be implemented by application

Table 10. MPPTCore Interfaces

Interface	Description
nxLibMpt_Hfal_SysParams_Init	called during system initialization. Typically this API should be implemented to store any initialized system parameters data
nxLibMpt_Hfal_SysParams_ReadPVParams	returns the PV voltage and current values
nxLibMpt_Hfal_SysParams_ReadBatVoltage	returns the lead-acid battery voltage
nxLibMpt_Hfal_SysParams_ReadBatCurrent	returns the lead-acid battery current
nxLibMpt_Hfal_SysParams_ReadLoadCurrent	returns the load current
nxLibMpt_Hfal_SysParams_ReadBatTemperature	returns the battery temperature
nxLibMpt_Hfal_SysParams_GetPVOpenCkt_Voltage	returns the PV open circuit voltage
nxLibMpt_Hfal_SysParams_BringPVVG_ToNewLevel	sets the PV voltage to a new voltage specified
nxLibMpt_Hfal_SysParams_SwitchLED_ON	switches on the specified LED
nxLibMpt_Hfal_SysParams_SwitchLED_OFF	switches off the specified LED

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19. List of figures

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