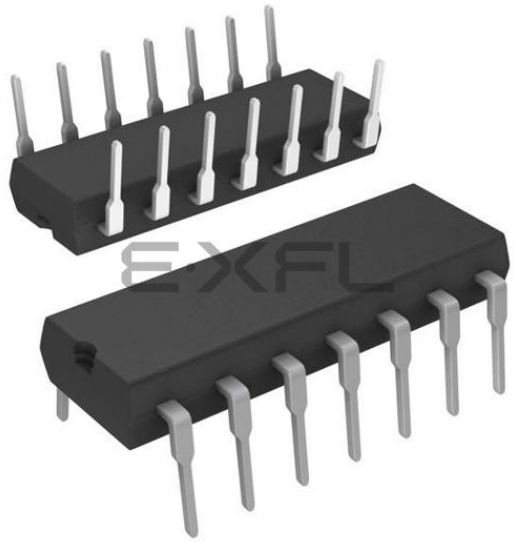

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15325-e-p

TABLE 4-2: MEMORY ACCESS PARTITION

REG	Address	Partition			
		$\overline{\text{BBEN}}$ = 1 SAFEN = 1	$\overline{\text{BBEN}}$ = 1 SAFEN = 0	$\overline{\text{BBEN}}$ = 0 SAFEN = 1	$\overline{\text{BBEN}}$ = 0 SAFEN = 0
PFM	00 0000h • • • Last Boot Block Memory Address	APPLICATION BLOCK(4)	APPLICATION BLOCK(4)	BOOT BLOCK(4)	BOOT BLOCK(4)
	Last Boot Block Memory Address + 1(1) • • • Last Program Memory Address - 80h			APPLICATION BLOCK(4)	APPLICATION BLOCK(4)
	Last Program Memory Address - 7Fh(2) • • • Last Program Memory Address		SAF(4)		SAF(4)
CONF IG	Config Memory Address(3)	CONFIG			

Note 1: Last Boot Block Memory Address is based on BBSIZE<2:0> given in Table 5-1.

2: Last Program Memory Address is the Flash size given in Table 4-1.

3: Config Memory Address are the address locations of the Configuration Words given in Table 13-2.

4: Each memory block has a corresponding write protection fuse defined by the $\overline{\text{WRTAPP}}$, $\overline{\text{WRTB}}$ and $\overline{\text{WRTC}}$ bits in the Configuration Word (Register 5-4).

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 0											
	CPU CORE REGISTERS; see Table 4-9 for specifics										
00Ch	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
00Dh	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	uuuu ----
00Eh	PORTC	RC7(1)	RC6(1)	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
00Fh	—	Unimplemented								—	—
010h	—	Unimplemented								—	—
011h	—	Unimplemented								---- ----	---- ----
012h	TRISA	—	—	TRISA5	TRISA4	—	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
013h	TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	xxxx ----	uuuu ----
014h	TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
015h	—	Unimplemented								—	—
016h	—	Unimplemented								—	—
017h	—	Unimplemented								—	—
018h	LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	--xx xxxx	--uu uuuu
019h	LATB(1)	LATB7	LATB6	LATB5	LATB4	—	—	—	—	xxxx ----	uuuu ----
01Ah	LATC	LATC7(1)	LATC6(1)	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx	uuuu uuuu
01Eh	—	Unimplemented								—	—
01Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Present only in PIC16(L)F15345.

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 61											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1E8Ch	—	Unimplemented								—	—
1E8Dh	—	Unimplemented								—	—
1E8Eh	—	Unimplemented								—	—
1E8Fh	PPSLOCK	—	—	—	—	—	—	—	PPSLOCKED	---- ---0	---- ---0
1E90h	INTPPS	—	—	INTPPS<5:0>						--00 1000	--uu uuuu
1E91h	T0CKIPPS	—	—	T0CKIPPS<5:0>						--00 0100	--uu uuuu
1E92h	T1CKIPPS	—	—	T1CKIPPS<5:0>						--01 0000	--uu uuuu
1E93h	T1GPPS	—	—	T1GPPS<5:0>						--00 1101	--uu uuuu
1E94h — 1E9Bh	—	Unimplemented								—	—
1E9Ch	T2INPPS	—	—	T2INPPS<5:0>						--01 0011	--uu uuuu
1E9Dh — 1EA0h	—	Unimplemented								—	—
1EA1h	CCP1PPS	—	—	CCP1PPS<5:0>						--01 0010	--uu uuuu
1EA2h	CCP2PPS	—	—	CCP2PPS<5:0>						--01 0001	--uu uuuu
1EA3h — 1EB0h	—	Unimplemented								—	—
1EB1h	CWG1PPS	—	—	CWG1PPS<5:0>						--00 1000	--uu uuuu
1EB2h — 1EBAh	—	Unimplemented								—	—
1EBBh	CLCIN0PPS	—	—	CLCIN0PPS<5:0>						--00 0000	--uu uuuu
1EBCh	CLCIN1PPS	—	—	CLCIN1PPS<5:0>						--00 0001	--uu uuuu
1EBDh	CLCIN2PPS	—	—	CLCIN2PPS<5:0>						--00 1110	--uu uuuu
1EBEh	CLCIN3PPS	—	—	CLCIN3PPS<5:0>						--00 1111	--uu uuuu
1EBFh — 1EC2h	—	Unimplemented								—	—
1EC3h	ADACTPPS	—	—	CLCIN3PPS<5:0>						--001100	--uuuuuu
1EC4h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

8.3 Register Definitions: Brown-out Reset Control

REGISTER 8-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN(1)	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit(1)
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

8.13 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON registers are updated to indicate the cause of the Reset. Table 8-3 and Table 8-4 show the Reset conditions of these registers.

TABLE 8-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

STOVF	STKUNF	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{MEMV}}$	Condition
0	0	1	1	1	0	x	1	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	u	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	0	1	1	1	0	x	x	0	u	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
0	0	u	1	1	u	0	1	1	u	Brown-out Reset
u	u	0	u	u	u	u	0	u	u	WWDT Reset
u	u	u	u	u	u	u	0	0	u	WWDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	u	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	1	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	u	0	u	u	u	1	0	u	$\overline{\text{MCLR}}$ Reset during Sleep
u	u	u	u	0	u	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)
u	u	u	u	u	u	u	u	u	0	Memory violation Reset

TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON0 Register	PCON1 Register
Power-on Reset	0000h	---1 1000	0011 110x	---- --1-
$\overline{\text{MCLR}}$ Reset during normal operation	0000h	---u uuuu	uuuu 0uuu	---- --1-
$\overline{\text{MCLR}}$ Reset during Sleep	0000h	---1 0uuu	uuuu 0uuu	---- --u-
WWDT Timeout Reset	0000h	---0 uuuu	uuu0 uuuu	---- --u-
WWDT Wake-up from Sleep	PC + 1	---0 0uuu	uuuu uuuu	---- --u-
WWDT Window Violation	0000h	---u uuuu	uu0u uuuu	---- --u-
Brown-out Reset	0000h	---1 1000	0011 11u0	---- --u-
Interrupt Wake-up from Sleep	PC + 1(1)	---1 0uuu	uuuu uuuu	---- --u-
RESET Instruction Executed	0000h	---u uuuu	uuuu u0uu	---- --u-
Stack Overflow Reset (STVREN = 1)	0000h	---u uuuu	1uuu uuuu	---- --u-
Stack Underflow Reset (STVREN = 1)	0000h	---u uuuu	u1uu uuuu	---- --u-
Memory Violation Reset ($\overline{\text{MEMV}}$ = 0)	0	-uuu uuuu	uuuu uuuu	---- --0-

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

REGISTER 16-2: PMD1: PMD CONTROL REGISTER 1

R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
NCO1MD	—	—	—	—	TMR2MD	TMR1MD	TMR0MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **NCO1MD:** Disable Numerically Control Oscillator bit
1 = NCO1 module disabled
0 = NCO1 module enabled

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **TMR2MD:** Disable Timer TMR2 bit
1 = Timer2 module disabled
0 = Timer2 module enabled

bit 1 **TMR1MD:** Disable Timer TMR1 bit
1 = Timer1 module disabled
0 = Timer1 module enabled

bit 0 **TMR0MD:** Disable Timer TMR0 bit
1 = Timer0 module disabled
0 = Timer0 module enabled

REGISTER 17-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **IOCBF<7:4>:** Interrupt-on-Change PORTB Flag bits
1 = An enabled change was detected on the associated pin.
Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.
0 = No change was detected, or the user cleared the detected change.

bit 3-0 **Unimplemented:** read as ‘0’

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		220
ADCON0	CHS<5:0>						GO/$\overline{\text{DONE}}$	ADON	233
ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		234
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	242

Legend: – = unimplemented locations read as '0'. Shaded cells are not used with the Fixed Voltage Reference.

TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TMR0L	Holding Register for the Least Significant Byte of the 16-bit TMR0 Register								270*
TMR0H	Holding Register for the Most Significant Byte of the 16-bit TMR0 Register								270*
T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				273
T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				274
T0CKIPPS	—	—	T0CKIPPS<5:0>						199
TMR0PPS	—	—	TMR0PPS<5:0>						199
T1GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	285
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	124
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	133
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	125

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.

* Page with Register information.

27.5.2 HARDWARE GATE MODE

The Hardware Gate modes operate the same as the Software Gate mode except the TMRx_ers external signal gates the timer. When used with the CCP the gating extends the PWM period. If the timer is stopped when the PWM output is high then the duty cycle is also extended.

When MODE<4:0> = 00001 then the timer is stopped when the external signal is high. When MODE<4:0> = 00010 then the timer is stopped when the external signal is low.

Figure 27-5 illustrates the Hardware Gating mode for MODE<4:0> = 00001 in which a high input level starts the counter.

FIGURE 27-5: HARDWARE GATE MODE TIMING DIAGRAM (MODE = 00001)

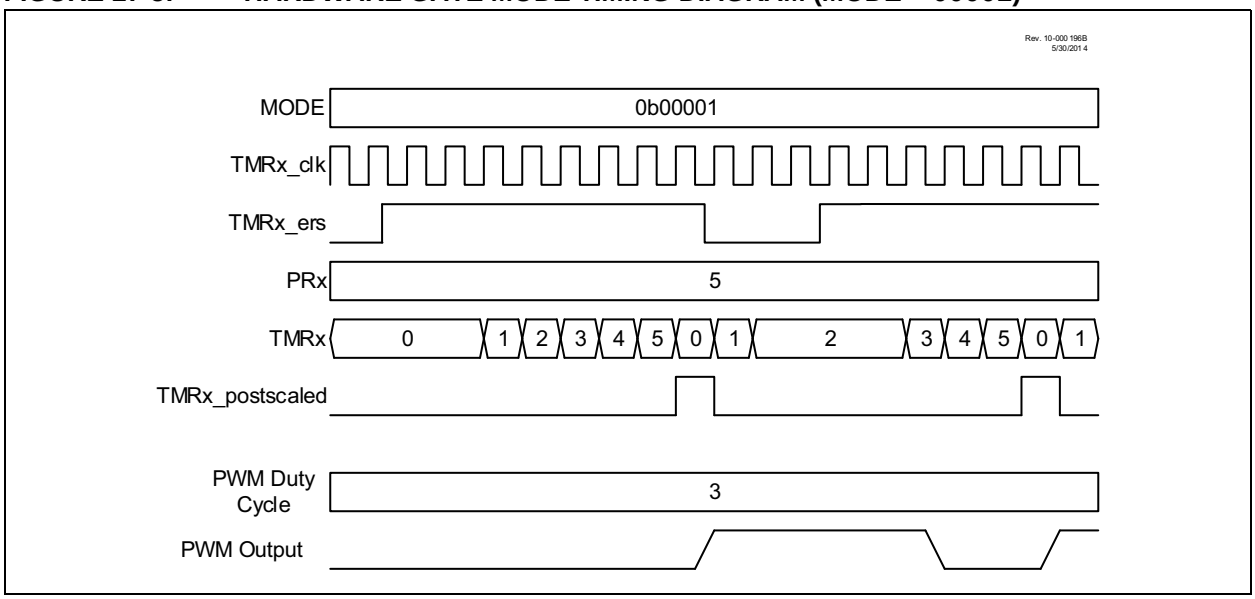
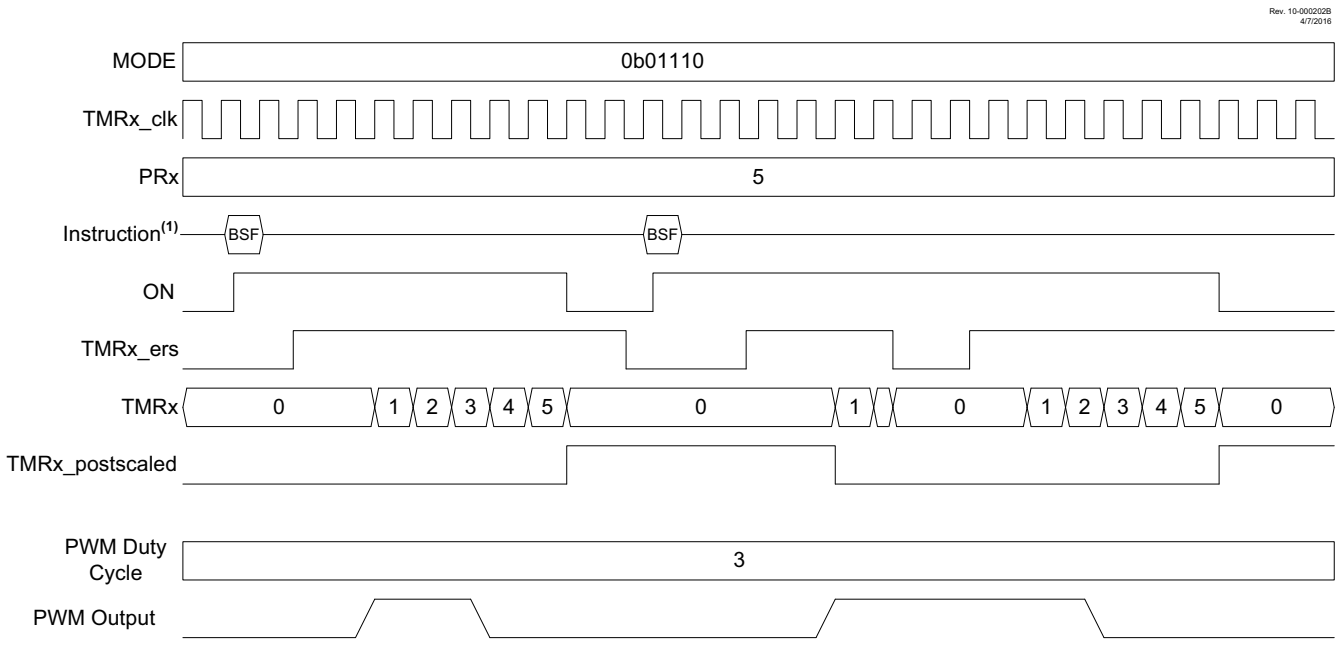


FIGURE 27-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01110)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

TABLE 28-5: SUMMARY OF REGISTERS ASSOCIATED WITH CCPx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	124
PIR4	—	—	—	—	—	—	TMR2IF	TMR1IF	137
PIE4	—	—	—	—	—	—	TMR2IE	TMR1IE	129
CCP1CON	EN	—	OUT	FMT	MODE<3:0>				321
CCP1CAP	—	—	—	—	—	CTS<2:0>			323
CCPR1L	Capture/Compare/PWM Register 1 (LSB)								323
CCPR1H	Capture/Compare/PWM Register 1 (MSB)								324
CCP2CON	EN	—	OUT	FMT	MODE<3:0>				321
CCP2CAP	—	—	—	—	—	CTS<2:0>			323
CCPR2L	Capture/Compare/PWM Register 1 (LSB)								323
CCPR2H	Capture/Compare/PWM Register 1 (MSB)								323
CCP1PPS	—	—	CCP1PPS<5:0>						199
CCP2PPS	—	—	CCP2PPS<5:0>						199
RxyPPS	—	—	—	RxyPPS<4:0>					200
ADACT	—	—	—	—	ADACT<3:0>				235
CLCxSELy	—	—	—	LCxDyS<4:0>					367
CWG1ISM	—	—	—	—	IS<3:0>				356

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the CCP module.

REGISTER 31-2: CLCxPOL: SIGNAL POLARITY CONTROL REGISTER

R/W-0/0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxPOL	—	—	—	LCxG4POL	LCxG3POL	LCxG2POL	LCxG1POL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **LCxPOL:** CLCxOUT Output Polarity Control bit
1 = The output of the logic cell is inverted
0 = The output of the logic cell is not inverted

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **LCxG4POL:** Gate 3 Output Polarity Control bit
1 = The output of gate 3 is inverted when applied to the logic cell
0 = The output of gate 3 is not inverted

bit 2 **LCxG3POL:** Gate 2 Output Polarity Control bit
1 = The output of gate 2 is inverted when applied to the logic cell
0 = The output of gate 2 is not inverted

bit 1 **LCxG2POL:** Gate 1 Output Polarity Control bit
1 = The output of gate 1 is inverted when applied to the logic cell
0 = The output of gate 1 is not inverted

bit 0 **LCxG1POL:** Gate 0 Output Polarity Control bit
1 = The output of gate 0 is inverted when applied to the logic cell
0 = The output of gate 0 is not inverted

32.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allows time for the slave software to decide whether it wants to $\overline{ACK}$ the receive address or data byte.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 32-16 displays a module using both address and data holding. Figure 32-17 includes the operation with the SEN bit of the SSP1CON2 register set.

1. S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
2. Matching address with R/$\overline{W}$ bit clear is clocked in. SSP1IF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSP1IF.
4. Slave can look at the ACKTIM bit of the SSP1CON3 register to determine if the SSP1IF was after or before the $\overline{ACK}$.
5. Slave reads the address value from SSP1BUF, clearing the BF flag.
6. Slave sets $\overline{ACK}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSP1IF is set after an $\overline{ACK}$, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the $\overline{ACK}$.
10. Slave clears SSP1IF.

Note:	SSP1IF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSP1IF not set

11. SSP1IF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSP1CON3 to determine the source of the interrupt.
13. Slave reads the received data from SSP1BUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{ACK}$ = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSP1STAT register.

33.4.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXxSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

33.4.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see **Section 33.4.1.3 "Synchronous Master Transmission")**, except in the case of the Sleep mode.

If two words are written to the TXxREG and then the SLEEP instruction is executed, the following will occur:

1. The first character will immediately transfer to the TSR register and transmit.
2. The second word will remain in the TXxREG register.
3. The TXxIF bit will not be set.
4. After the first character has been shifted out of TSR, the TXxREG register will transfer the second character to the TSR and the TXxIF bit will now be set.
5. If the PEIE and TXxIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.

33.4.2.2 Synchronous Slave Transmission Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for the CK pin (if applicable).
3. Clear the CREN and SREN bits.
4. If interrupts are desired, set the TXxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit transmission is desired, set the TX9 bit.
6. Enable transmission by setting the TXEN bit.
7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
8. Start transmission by writing the Least Significant eight bits to the TXxREG register.

REGISTER 34-2: CLKRCLK: CLOCK REFERENCE CLOCK SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	CLKRCLK<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **CLKRCLK<3:0>:** CLKR Input bits

Clock Selection
1111 = Reserved
•
•
•
1011 = Reserved
1010 = LC4_out
1001 = LC3_out
1000 = LC2_out
0111 = LC1_out
0110 = NCO1_out
0101 = SOSC
0100 = MFINTOSC (31.25 kHz)
0011 = MFINTOSC (500 kHz)
0010 = LFINTOSC
0001 = HFINTOSC
0000 = FOSC

TABLE 34-1: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK REFERENCE OUTPUT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CLKRCON	CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>			456
CLKRCLK	—	—	—	—	CLKRCLK<3:0>				457
CLCxSELy	—	—	LCxDyS<5:0>						367
RxyPPS	—	—	—	RxyPPS<4:0>					200

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used by the CLKR module.

FIGURE 37-7: CLKOUT AND I/O TIMING

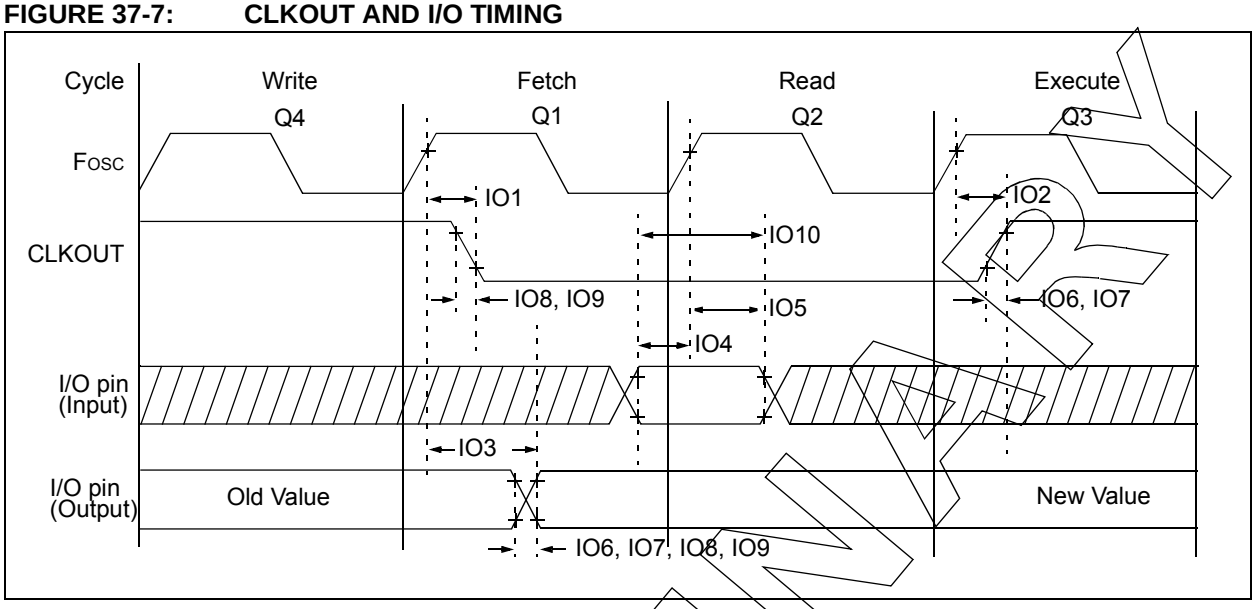


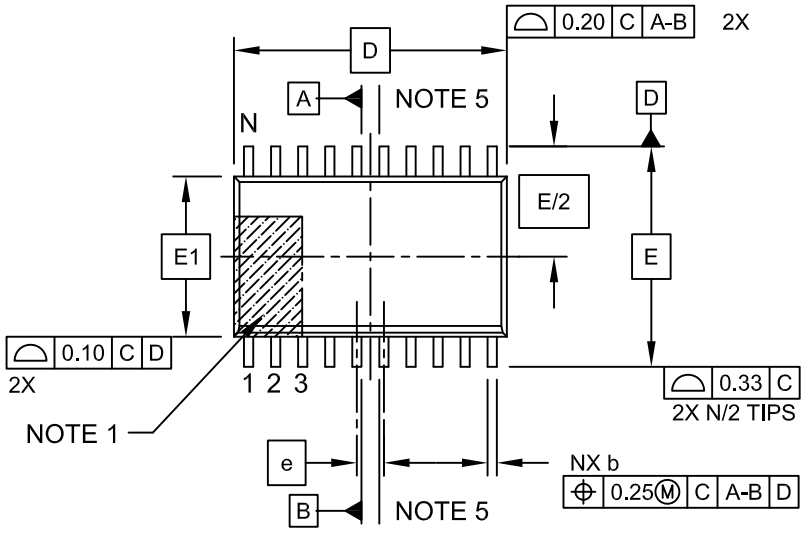
TABLE 37-10: I/O AND CLKOUT TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
IO1*	$T_{CLKOUTH}$	CLKOUT rising edge delay (rising edge Fosc (Q1 cycle) to falling edge CLKOUT	—	—	70	ns	
IO2*	$T_{CLKOUTL}$	CLKOUT falling edge delay (rising edge Fosc (Q3 cycle) to rising edge CLKOUT	—	—	72	ns	
IO3*	T_{IO_VALID}	Port output valid time (rising edge Fosc (Q1 cycle) to port valid)	—	50	70	ns	
IO4*	T_{IO_SETUP}	Port input setup time (Setup time before rising edge Fosc – Q2 cycle)	20	—	—	ns	
IO5*	T_{IO_HOLD}	Port input hold time (Hold time after rising edge Fosc – Q2 cycle)	50	—	—	ns	
IO6*	T_{IOR_SLREN}	Port I/O rise time, slew rate enabled	—	25	—	ns	V_{DD} = 3.0V
IO7*	T_{IOR_SLRDIS}	Port I/O rise time, slew rate disabled	—	5	—	ns	V_{DD} = 3.0V
IO8*	T_{IOF_SLREN}	Port I/O fall time, slew rate enabled	—	25	—	ns	V_{DD} = 3.0V
IO9*	T_{IOF_SLRDIS}	Port I/O fall time, slew rate disabled	—	5	—	ns	V_{DD} = 3.0V
IO10*	T_{INT}	INT pin high or low time to trigger an interrupt	25	—	—	ns	
IO11*	T_{IOC}	Interrupt-on-Change minimum high or low time to trigger interrupt	25	—	—	ns	

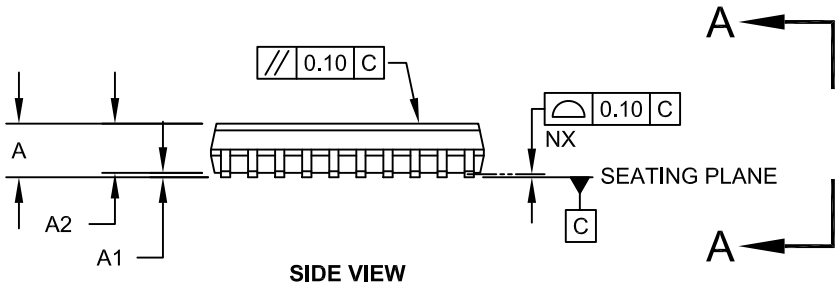
*These parameters are characterized but not tested.

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

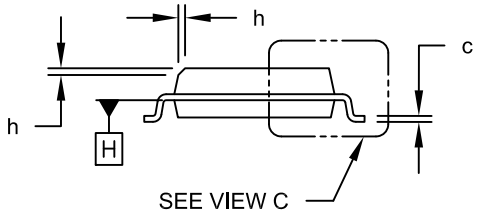
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2

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ISBN: 978-1-5224-1220-5