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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15345-e-so

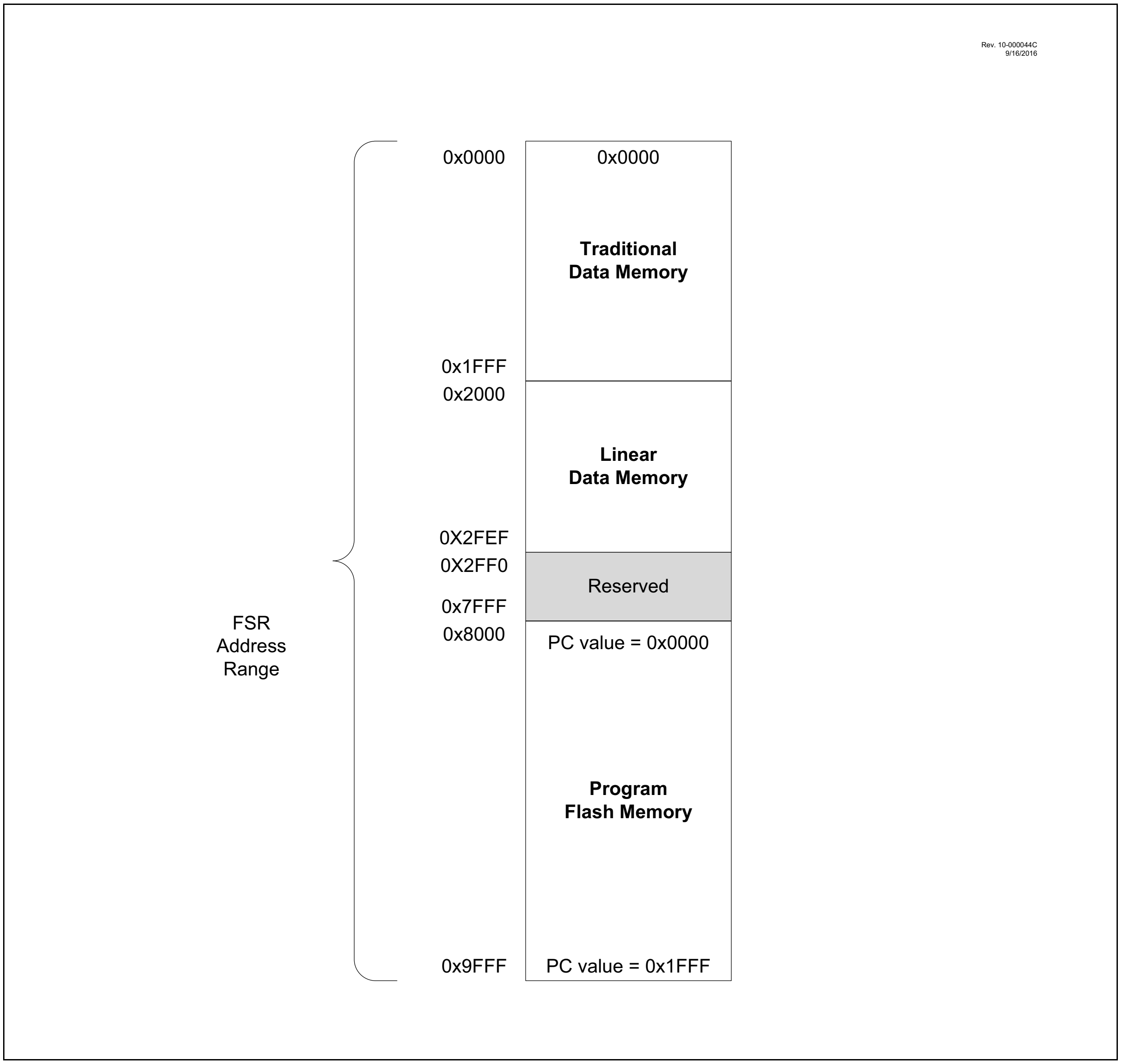
TABLE 4-7: PIC16(L)F15325/45 MEMORY MAP, BANKS 56-63

	BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63
1C00h–1C0Bh	Core Register (Table 4-3)	1C80h–1C8Bh	Core Register (Table 4-3)	1D00h–1D0Bh	Core Register (Table 4-3)	1D80h–1D8Bh	Core Register (Table 4-3)	1E00h–1E0Bh	Core Register (Table 4-3)	1E80h–1E8Bh	Core Register (Table 4-3)	1F00h–1F0Bh	Core Register (Table 4-3)	1F80h–1F8Bh	Core Register (Table 4-3)
1C0Ch	—	1C8Ch	—	1D0Ch	—	1D8Ch	—	1E0Ch	CLC Controls (See Table 4-8 for register mapping details)	1E8Ch	nnnPPS Controls (See Table 4-8 for register mapping details)	1F0Ch	RxyPPS Controls (See Table 4-8 for register mapping details)	1F8Ch	(See Table 4-8 for register mapping details)
1C0Dh	—	1C8Dh	—	1D0Dh	—	D8Dh1	—	1E0Dh		1E8Dh		1F0Dh		1F8Dh	
1C0Eh	—	1C8Eh	—	1D0Eh	—	1D8Eh	—	1E0Eh		1E8Eh		1F0Eh		1F8Eh	
1C0Fh	—	1C8Fh	—	1D0Fh	—	1D8Fh	—	1E0Fh		1E8Fh		1F0Fh		1F8Fh	
1C10h	—	1C90h	—	1D10h	—	1D90h	—	1E10h		1E90h		1F10h		1F90h	
1C11h	—	1C91h	—	1D11h	—	1D91h	—	1E11h		1E91h		1F11h		1F91h	
1C12h	—	1C92h	—	1D12h	—	1D92h	—	1E12h		1E92h		1F12h		1F92h	
1C13h	—	1C93h	—	1D13h	—	1D93h	—	1E13h		1E93h		1F13h		1F93h	
1C14h	—	1C94h	—	1D14h	—	1D94h	—	1E14h		1E94h		1F14h		1F94h	
1C15h	—	1C95h	—	1D15h	—	1D95h	—	1E15h		1E95h		1F15h		1F95h	
1C16h	—	1C96h	—	1D16h	—	1D96h	—	1E16h		1E96h		1F16h		1F96h	
1C17h	—	1C97h	—	1D17h	—	1D97h	—	1E17h		1E97h		1F17h		1F97h	
1C18h	—	1C98h	—	1D18h	—	1D98h	—	1E18h		1E98h		1F18h		1F98h	
1C19h	—	1C99h	—	1D19h	—	1D99h	—	1E19h		1E99h		1F19h		1F99h	
1C1Ah	—	1C9Ah	—	1D1Ah	—	1D9Ah	—	1E1Ah		1E9Ah		1F1Ah		1F9Ah	
1C1Bh	—	1C9Bh	—	1D1Bh	—	1D9Bh	—	1E1Bh		1E9Bh		1F1Bh		1F9Bh	
1C1Ch	—	1C9Ch	—	1D1Ch	—	1D9Ch	—	1E1Ch		1E9Ch		1F1Ch		1F9Ch	
1C1Dh	—	1C9Dh	—	1D1Dh	—	1D9Dh	—	1E1Dh		1E9Dh		1F1Dh		1F9Dh	
1C1Eh	—	1C9Eh	—	1D1Eh	—	1D9Eh	—	1E1Eh		1E9Eh		1F1Eh		1F9Eh	
1C1Fh	—	1C9Fh	—	1D1Fh	—	1D9Fh	—	1E1Fh		1E9Fh		1F1Fh		1F9Fh	
1C20h–1C6Fh	Unimplemented Read as ‘0’	1CA0h–1CEFh	Unimplemented Read as ‘0’	1D20h–1D6Fh	Unimplemented Read as ‘0’	1DA0h–1DEFh	Unimplemented Read as ‘0’	1E20h–1E6Fh		1EA0h–1EEFh		1F20h–1F6Fh		1FA0h–1FEFh	
1C70h–1C7Fh	Common RAM Accesses 70h-7Fh	1CF0h–1CFFh	Common RAM Accesses 70h-7Fh	1D70h–1D7Fh	Common RAM Accesses 70h-7Fh	1DF0h–1DFFh	Common RAM Accesses 70h-7Fh	1E70h–1E7Fh	Common RAM Accesses 70h-7Fh	1EF0h–1EFFh	Common RAM Accesses 70h-7Fh	1F70h–1F7Fh	Common RAM Accesses 70h-7Fh	1FF0h–1FFFh	Common RAM Accesses 70h-7Fh

Note 1: Unimplemented locations read as ‘0’.

2: The banks 24-55 have been omitted from the tables in the data sheet since the banks have unimplemented registers.

FIGURE 4-8: INDIRECT ADDRESSING PIC16(L)F15325/45



8.3 Register Definitions: Brown-out Reset Control

REGISTER 8-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN(1)	—	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **SBOREN:** Software Brown-out Reset Enable bit(1)
If BOREN <1:0> in Configuration Words ≠ 01:
SBOREN is read/write, but has no effect on the BOR.
If BOREN <1:0> in Configuration Words = 01:
1 = BOR Enabled
0 = BOR Disabled

bit 6-1 **Unimplemented:** Read as '0'

bit 0 **BORRDY:** Brown-out Reset Circuit Ready Status bit
1 = The Brown-out Reset circuit is active
0 = The Brown-out Reset circuit is inactive

Note 1: BOREN<1:0> bits are located in Configuration Words.

14.2.6 ANALOG CONTROL

The ANSELA register (Register 14-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as ‘0’ and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to ‘0’ by user software.

14.2.7 WEAK PULL-UP CONTROL

The WPUA register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.2.8 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

TABLE 14-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	178
TRISA	—	—	TRISA5	TRISA4	—	TRISA2	TRISA1	TRISA0	178
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	179
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	179
WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	180
ODCONA	—	—	ODCA5	ODCA4	—	ODCA2	ODCA1	ODCA0	180
SLRCONA	—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0	181
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	181

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

14.4 PORTB Registers (PIC16(L)F15345 only)

14.4.1 DATA REGISTER

PORTB is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 14-10). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., disable the output driver). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Figure 14-1 shows how to initialize PORTB.

Reading the PORTB register (Register 14-9) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

The PORT data latch LATB (Register 14-11) holds the output port data, and contains the latest value of a LATB or PORTB write.

14.4.2 DIRECTION CONTROL

The TRISB register (Register 14-10) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

14.4.3 OPEN-DRAIN CONTROL

The ODCONB register (Register 14-14) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONB bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONB bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note:	It is not necessary to set open-drain control when using the pin for I^2C; the I^2C module controls the pin and makes the pin open-drain.

14.4.4 SLEW RATE CONTROL

The SLRCONB register (Register 14-15) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONB bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONB bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

14.4.5 INPUT THRESHOLD CONTROL

The INLVLB register (Register 14-8) controls the input voltage threshold for each of the available PORTB input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTB register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 37-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

14.4.6 ANALOG CONTROL

The ANSELB register (Register 14-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

14.4.7 WEAK PULL-UP CONTROL

The WPUB register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.4.8 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

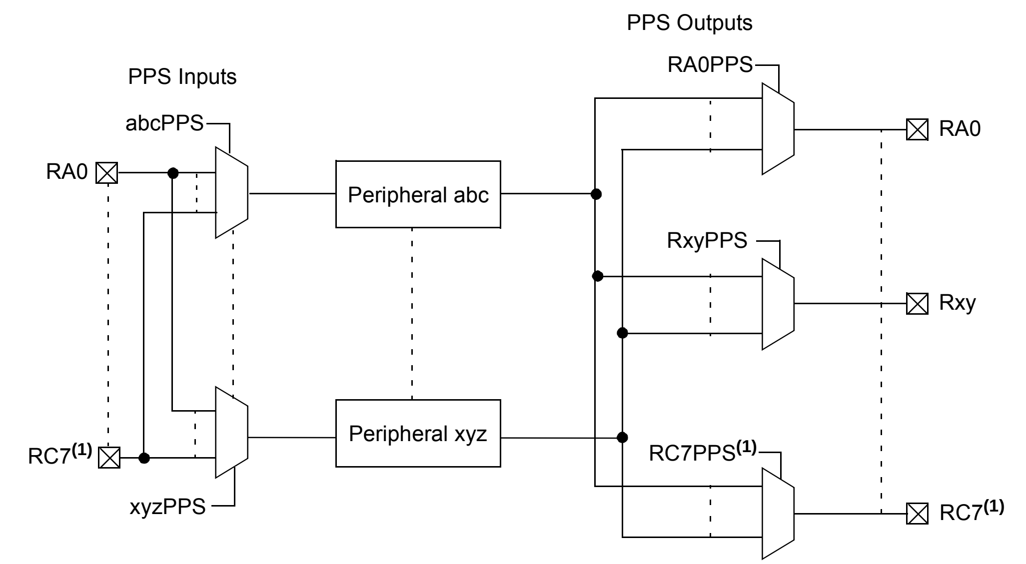
Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

15.0 PERIPHERAL PIN SELECT (PPS) MODULE

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections.

All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the simplified block diagram Figure 15-1.

FIGURE 15-1: SIMPLIFIED PPS BLOCK DIAGRAM



Note: Not available on 14-Pin devices.

15.1 PPS Inputs

Each peripheral has a PPS register with which the inputs to the peripheral are selected. Inputs include the device pins.

Although every peripheral has its own PPS input selection register, the selections are identical for every peripheral as shown in Register 15-1.

Note:	The notation “xxx” in the register name is a place holder for the peripheral identifier. For example, CLC1PPS.

15.2 PPS Outputs

Each I/O pin has a PPS register with which the pin output source is selected. With few exceptions, the port TRIS control associated with that pin retains control over the pin output driver. Peripherals that control the pin output driver as part of the peripheral operation will override the TRIS control as needed. These peripherals are (See **Section 15.3 “Bidirectional Pins”**):

- EUSART (synchronous operation)
- MSSP (I^2C)

Although every pin has its own PPS peripheral selection register, the selections are identical for every pin as shown in Register 15-2.

Note:	The notation “Rxy” is a place holder for the pin port and bit identifiers. For example, x and y for PORTA bit 0 would be A and 0, respectively, resulting in the pin PPS output selection register RA0PPS.

TABLE 15-1: PPS INPUT SIGNAL ROUTING OPTIONS (PIC16(L)F15325)

INPUT SIGNAL NAME	Input Register Name	Default Location at POR	Reset Value (xxxPPS<4:0>)	Remappable to Pins of PORTx PIC16(L)F15325 PORTA	PORTC
INT	INTPPS	RA2	00010	●	●
T0CKI	T0CKIPPS	RA2	00010	●	●
T1CKI	T1CKIPSS	RA5	00101	●	●
T1G	T1GPPS	RA4	00100	●	●
T2IN	T2INPPS	RA5	00101	●	●
CCP1	CCP1PPS	RC5	10101	●	●
CCP2	CCP2PPS	RC3	10011	●	●
CWG1IN	CWG1INPPS	RA2	00010	●	●
CLCIN0	CLCIN0PPS	RC3	10011	●	●
CLCIN1	CLCIN1PPS	RC4	10100	●	●
CLCIN2	CLCIN2PPS	RC1	10001	●	●
CLCIN3	CLCIN3PPS	RA5	00101	●	●
ADACT	ADACTPPS	RC2	10010	●	●
SCK1/SCL1	SSP1CLKPPS	RC0	10000	●	●
SDI1/SDA1	SSP1DATPPS	RC1	10001	●	●
SS1	SSP1SS1PPS	RC3	10011	●	●
RX1/DT1	RX1PPS	RC5	10101	●	●
CK1	TX1PPS	RC4	10100	●	●
RX2/DT2	RX2PPS	RC1	10001	●	●
CK2	TX2PPS	RC0	10000	●	●

TABLE 15-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PPSLOCK	—	—	—	—	—	—	—	PPSLOCKED	200
INTPPS	—	—	INTPPS<5:0>						199
T0CKIPPS	—	—	T0CKIPPS<5:0>						199
T1CKIPPS	—	—	T1CKIPPS<5:0>						199
T1GPPS	—	—	T1GPPS<5:0>						199
T2AINPPS			T2AINPPS<5:0>						199
CCP1PPS	—	—	CCP1PPS<5:0>						199
CCP2PPS	—	—	CCP2PPS<5:0>						199
CWG1PPS	—	—	CWG1PPS<5:0>						199
SSP1CLKPPS	—	—	SSP1CLKPPS<5:0>						199
SSP1DATPPS	—	—	SSP1DATPPS<5:0>						199
SSP1SSPPS	—	—	SSP1SSPPS<5:0>						199
RX1PPS	—	—	RXPPS<5:0>						200
TX1PPS	—	—	TXPPS<5:0>						199
CLCIN0PPS	—	—	CLCIN0PPS<5:0>						199
CLCIN1PPS	—	—	CLCIN1PPS<5:0>						199
CLCIN2PPS	—	—	CLCIN2PPS<5:0>						199
CLCIN3PPS	—	—	CLCIN3PPS<5:0>						199
RX2PPS	—	—	RX2PPS<5:0>						199
TX2PPS	—	—	TX2PPS<5:0>						199
ADACTPPS	—	—	ADACTPPS<5:0>						199
RA0PPS	—	—	—	RA0PPS<4:0>					200
RA1PPS	—	—	—	RA1PPS<4:0>					200
RA2PPS	—	—	—	RA2PPS<4:0>					200
RA3PPS	—	—	—	RA3PPS<4:0>					200
RA4PPS	—	—	—	RA4PPS<4:0>					200
RA5PPS	—	—	—	RA5PPS<4:0>					200
RB4PPS(1)	—	—	—	RB4PPS<4:0>					200
RB5PPS(1)	—	—	—	RB5PPS<4:0>					200
RB6PPS(1)	—	—	—	RB6PPS<4:0>					200
RB7PPS(1)	—	—	—	RB7PPS<4:0>					200
RC0PPS	—	—	—	RC0PPS<4:0>					200

Legend: — = unimplemented, read as ‘0’. Shaded cells are unused by the PPS module.
Note 1: Present on PIC16(L)F15345 only.

20.3 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 20-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 20-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 20-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 20-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}\\
&= T_{AMP} + T_C + T_{COFF}\\
&= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)]
\end{aligned}
$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \qquad ;[1]\ V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad ;[2]\ V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \qquad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for T_C:

$$
\begin{aligned}
T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047)\\
&= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885)\\
&= 1.37\mu s
\end{aligned}
$$

Therefore:

$$
\begin{aligned}
T_{ACQ} &= 2\mu s + 1.37 + [(50°C - 25°C)(0.05\mu s/°C)]\\
&= 4.62\mu s
\end{aligned}
$$

Note 1: The VAPPLIED has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

REGISTER 20-3: ADACT: A/D AUTO-CONVERSION TRIGGER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	ADACT<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **ADACT<3:0>:** Auto-Conversion Trigger Selection bits(1) (see Table 20-2)

Note 1: This is a rising edge sensitive input for all sources.

27.5.7 EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

In Edge-Triggered Hardware Limit One-Shot modes the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge start and Reset (MODE<4:0> = `01100`)
- Falling edge start and Reset (MODE<4:0> = `01101`)

The timer resets and clears the ON bit when the timer value matches the PRx period value. External signal edges will have no effect until after software sets the ON bit. Figure 27-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse-width value and stay deactivated until the timer halts at the PRx period match unless an external signal edge resets the timer before the match occurs.

29.0 PULSE-WIDTH MODULATION (PWM)

The PWMx modules generate Pulse-Width Modulated (PWM) signals of varying frequency and duty cycle.

In addition to the CCP modules, the PIC16(L)F15325/45 devices contain four 10-bit PWM modules (PWM3, PWM4, PWM5 and PWM6). The PWM modules reproduce the PWM capability of the CCP modules.

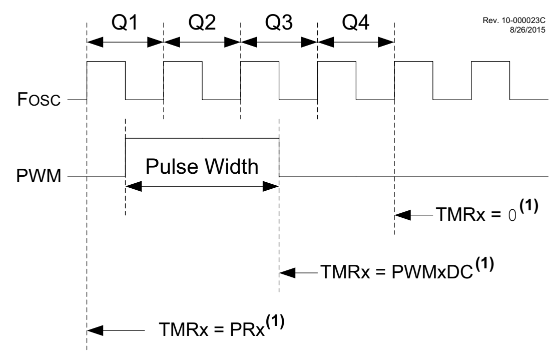
Note:	The PWM3/4/5/6 modules are four instances of the same PWM module design. Throughout this section, the lower case 'x' in register and bit names is a generic reference to the PWM module number (which should be substituted with 3, or 4, or, 5 or 6 during code development). For example, the control register is generically described in this chapter as PWMxCON, but the actual device registers are PWM3CON, PWM4CON, PWM5CON and PWM6CON. Similarly, the PWMxEN bit represents the PWM3EN, PWM4EN, PWM5EN and PWM6EN bits.

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the 'on' state (pulse width), and the low portion of the signal is considered the 'off' state. The term duty cycle describes the proportion of the 'on' time to the 'off' time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and, in turn, the power that is applied to the load.

Figure 29-1 shows a typical waveform of the PWM signal.

FIGURE 29-1: PWM OUTPUT



Note 1: Timer dependent on PWMTMRS register settings.

FIGURE 30-2: SIMPLIFIED CWG BLOCK DIAGRAM (PUSH-PULL MODE)

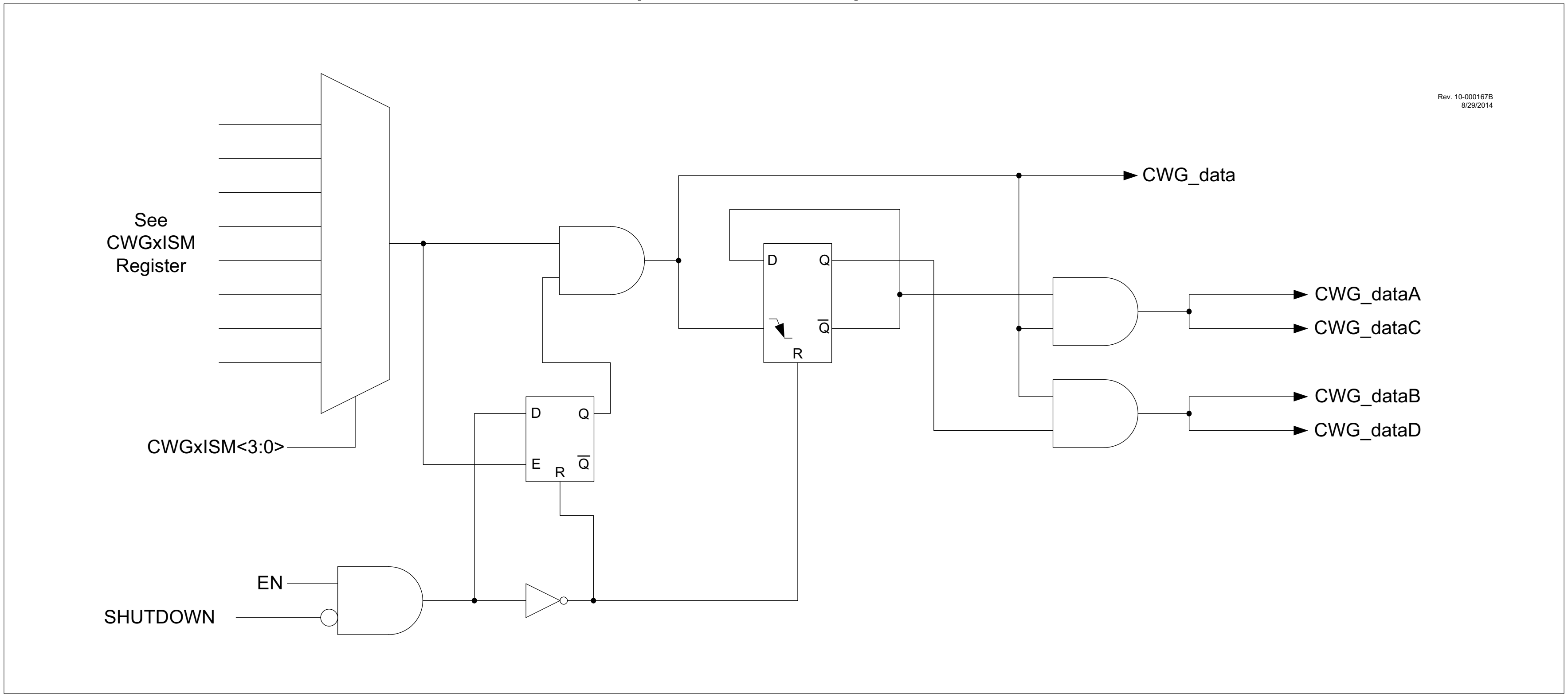


FIGURE 31-3: PROGRAMMABLE LOGIC FUNCTIONS

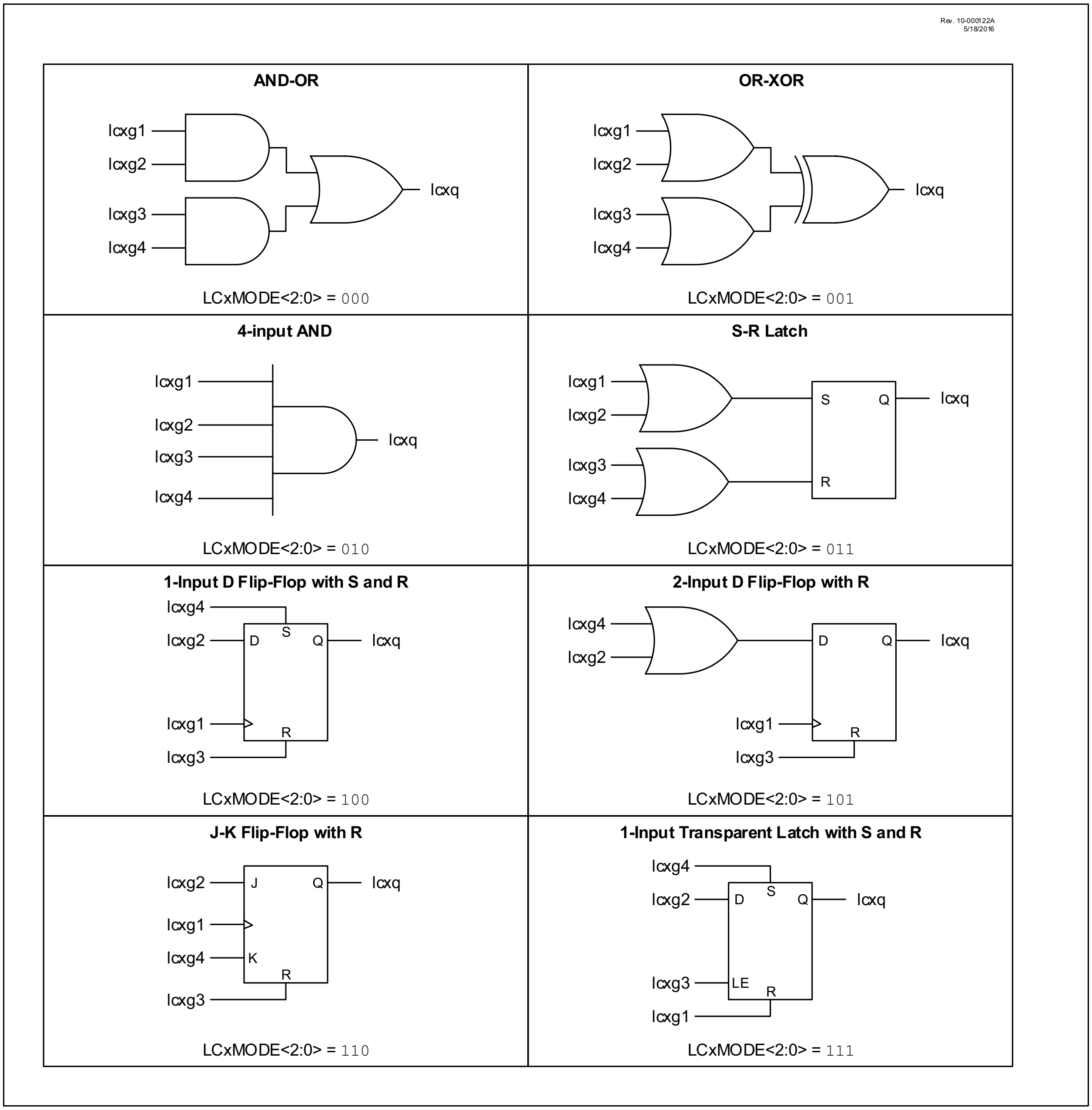


FIGURE 32-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)

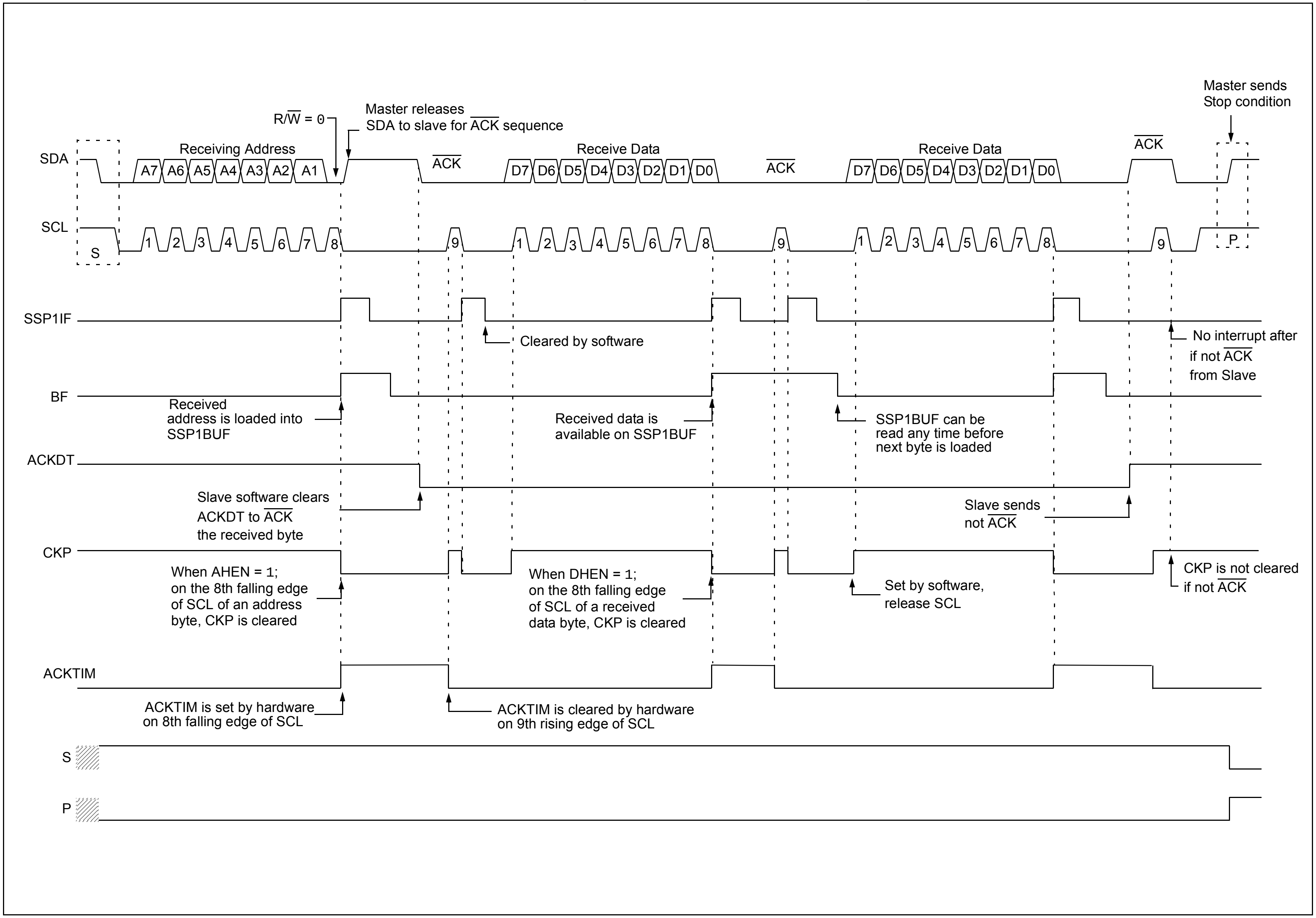


TABLE 37-5: MEMORY PROGRAMMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
High Voltage Entry Programming Mode Specifications							
MEM01	V_{IHH}	Voltage on $\overline{MCLR}$/VPP pin to enter programming mode	8	—	9	V	**(Note 2, Note 3)**
MEM02	I_{PPGM}	Current on $\overline{MCLR}$/VPP pin during programming mode	—	1	—	mA	**(Note 2)**
Programming Mode Specifications							
MEM10	V_{BE}	VDD for Bulk Erase	—	2.7	—	V	
MEM11	I_{DDPGM}	Supply Current during Programming operation	—	—	10	mA	
Program Flash Memory Specifications							
MEM30	E_P	Flash Memory Cell Endurance	10k	—	—	E/W	-40°C ≤ TA ≤ +85°C (**Note 1**)
MEM32	T_{P_RET}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
MEM33	V_{P_RD}	VDD for Read operation	VDDMIN	—	VDDMAX	V	
MEM34	V_{P_REW}	VDD for Row Erase or Write operation	VDDMIN	—	VDDMAX	V	
MEM35	T_{P_REW}	Self-Timed Row Erase or Self-Timed Write	—	2.0	2.5	ms	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Write.

2: Required only if CONFIG4, bit LVP is disabled.

3: The MPLAB® ICD2 does not support variable VPP output. Circuitry to limit the ICD2 VPP voltage must be placed between the ICD2 and target system when programming or debugging with the ICD2.

FIGURE 37-19: SPI SLAVE MODE TIMING (CKE = 0)

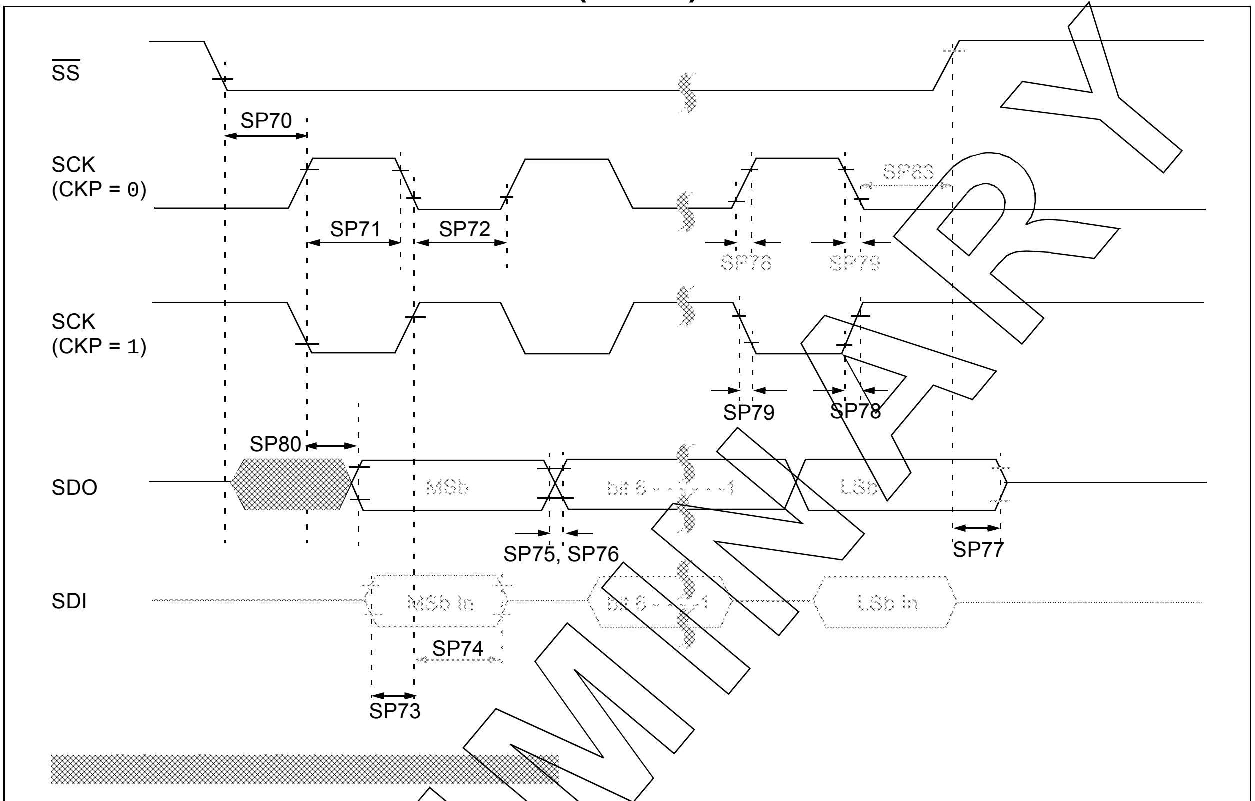
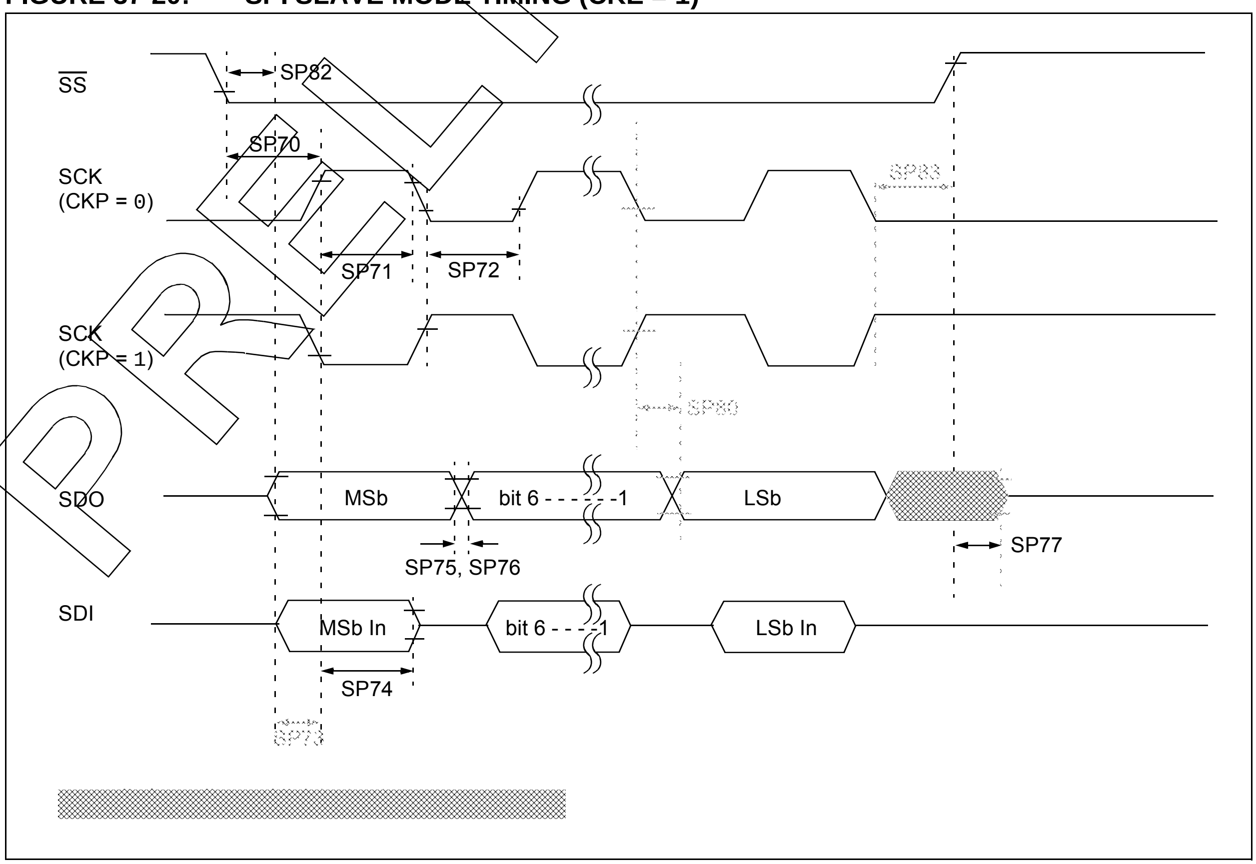


FIGURE 37-20: SPI SLAVE MODE TIMING (CKE = 1)



38.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the L and LF devices.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

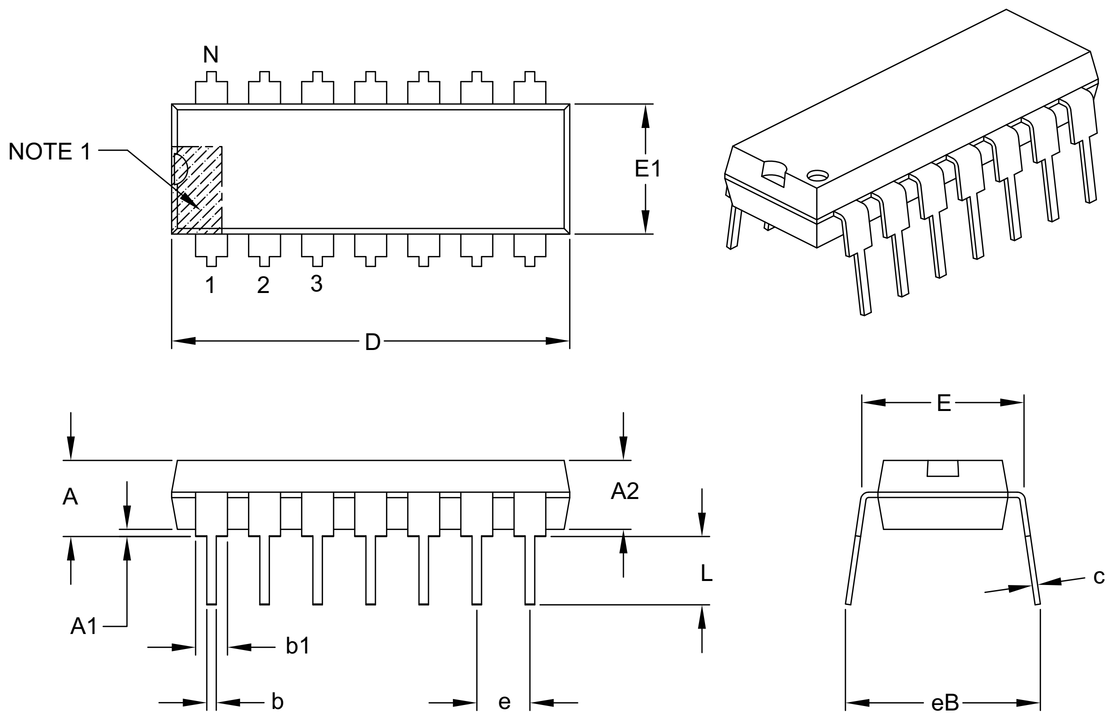
“Typical” represents the mean of the distribution at 25°C. “Maximum”, “Max.”, “Minimum” or “Min.” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

Charts and graphs are not available at this time.

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

