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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I ² C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 224 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 11x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 14-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15325-e-st |

TABLE 4-2: MEMORY ACCESS PARTITION

| REG | Address | Partition | | | |
|---------|---|---|---|---|---|
| | | $\overline{\text{BBEN}} = 1$ $\overline{\text{SAFEN}} = 1$ | $\overline{\text{BBEN}} = 1$ $\overline{\text{SAFEN}} = 0$ | $\overline{\text{BBEN}} = 0$ $\overline{\text{SAFEN}} = 1$ | $\overline{\text{BBEN}} = 0$ $\overline{\text{SAFEN}} = 0$ |
| PFM | 00 0000h ... Last Boot Block Memory Address | APPLICATION BLOCK ⁽⁴⁾ | APPLICATION BLOCK ⁽⁴⁾ | BOOT BLOCK ⁽⁴⁾ | BOOT BLOCK ⁽⁴⁾ |
| | Last Boot Block Memory Address + 1 ⁽¹⁾ ... Last Program Memory Address - 80h | | | APPLICATION BLOCK ⁽⁴⁾ | APPLICATION BLOCK ⁽⁴⁾ |
| | Last Program Memory Address - 7Fh ⁽²⁾ ... Last Program Memory Address | | SAF ⁽⁴⁾ | | SAF ⁽⁴⁾ |
| | | | | | |
| CONF IG | Config Memory Address ⁽³⁾ | CONFIG | | | |

- Note 1:** Last Boot Block Memory Address is based on BBSIZE<2:0> given in Table 5-1.
Note 2: Last Program Memory Address is the Flash size given in Table 4-1.
Note 3: Config Memory Address are the address locations of the Configuration Words given in Table 13-2.
Note 4: Each memory block has a corresponding write protection fuse defined by the $\overline{\text{WRTAPP}}$, $\overline{\text{WRTB}}$ and $\overline{\text{WRTC}}$ bits in the Configuration Word (Register 5-4).

REGISTER 5-3: CONFIGURATION WORD 3: WINDOWED WATCHDOG

| | | | | | |
|---------|---------|---------|--------|--------|--------|
| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| WDTCCS2 | WDTCCS1 | WDTCCS0 | WDCWS2 | WDCWS1 | WDCWS0 |
| bit 13 | | | bit 8 | | |

| | | | | | | | |
|-------|-------|-------|--------|--------|--------|--------|--------|
| U-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
| — | WDTE1 | WDTE0 | WDTCP4 | WDTCP3 | WDTCP2 | WDTCP1 | WDTCP0 |
| bit 7 | | | bit 0 | | | | |

Legend:

R = Readable bit

P = Programmable bit

x = Bit is unknown

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

W = Writable bit

n = Value when blank or after Bulk Erase

bit 13-11 **WDTCCS<2:0>**: WDT Input Clock Selector bits

111 = Software Control

110 = Reserved

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010 = SOSC 32 kHz

001 = WDT reference clock is the 31.0 kHz LFINTOSC

000 = WDT reference clock is the 31.25 kHz HFINTOSC (MFINTOSC) output

bit 10-8 **WDCWS<2:0>**: WDT Window Select bits

| WDCWS | WDTWS at POR | | | Software control of WDTWS? | Keyed access required? |
|-------|--------------|------------------------------|--------------------------------|----------------------------|------------------------|
| | Value | Window delay Percent of time | Window opening Percent of time | | |
| 111 | 111 | n/a | 100 | Yes | No |
| 110 | 111 | n/a | 100 | No | Yes |
| 101 | 101 | 25 | 75 | | |
| 100 | 100 | 37.5 | 62.5 | | |
| 011 | 011 | 50 | 50 | | |
| 010 | 010 | 62.5 | 37.5 | | |
| 001 | 001 | 75 | 25 | | |
| 000 | 000 | 87.5 | 12.5 | | |

bit 7 **Unimplemented**: Read as '1'

bit 6-5 **WDTE<1:0>**: WDT Operating mode:

11 =WDT enabled regardless of Sleep; SWDTEN is ignored

10 =WDT enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN ignored

01 =WDT enabled/disabled by SWDTEN bit in WDTCON0

00 =WDT disabled, SWDTEN is ignored

10.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

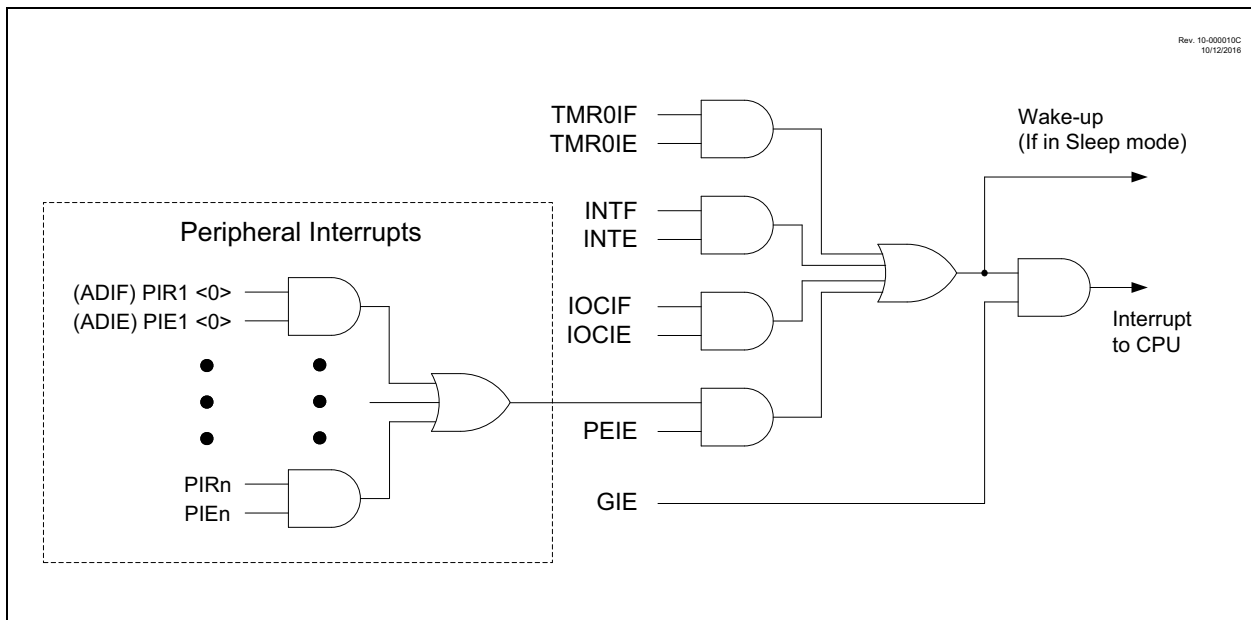
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 10-1.

FIGURE 10-1: INTERRUPT LOGIC



REGISTER 10-2: PIE0: PERIPHERAL INTERRUPT ENABLE REGISTER 0

| | | | | | | | |
|-------|-----|---------|---------|-----|-----|-----|---------|
| U-0 | U-0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | R/W-0/0 |
| — | — | TMR0IE | IOCIE | — | — | — | INTE |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HS = Hardware set

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TMR0IE:** Timer0 Overflow Interrupt Enable bit

1 = Enables the Timer0 interrupt

0 = Disables the Timer0 interrupt

bit 4 **IOCIE:** Interrupt-on-Change Interrupt Enable bit

1 = Enables the IOC change interrupt

0 = Disables the IOC change interrupt

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **INTE:** INT External Interrupt Flag bit⁽¹⁾

1 = Enables the INT external interrupt

0 = Disables the INT external interrupt

Note 1: The External Interrupt GPIO pin is selected by INTPPS (Register 15-1).

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by PIE1-PIE7. Interrupt sources controlled by the PIE0 register do not require PEIE to be set in order to allow interrupt vectoring (when GIE is set).

11.0 POWER-SAVING OPERATION MODES

The purpose of the Power-Down modes is to reduce power consumption. There are three Power-Down modes: DOZE mode, IDLE mode, and SLEEP mode.

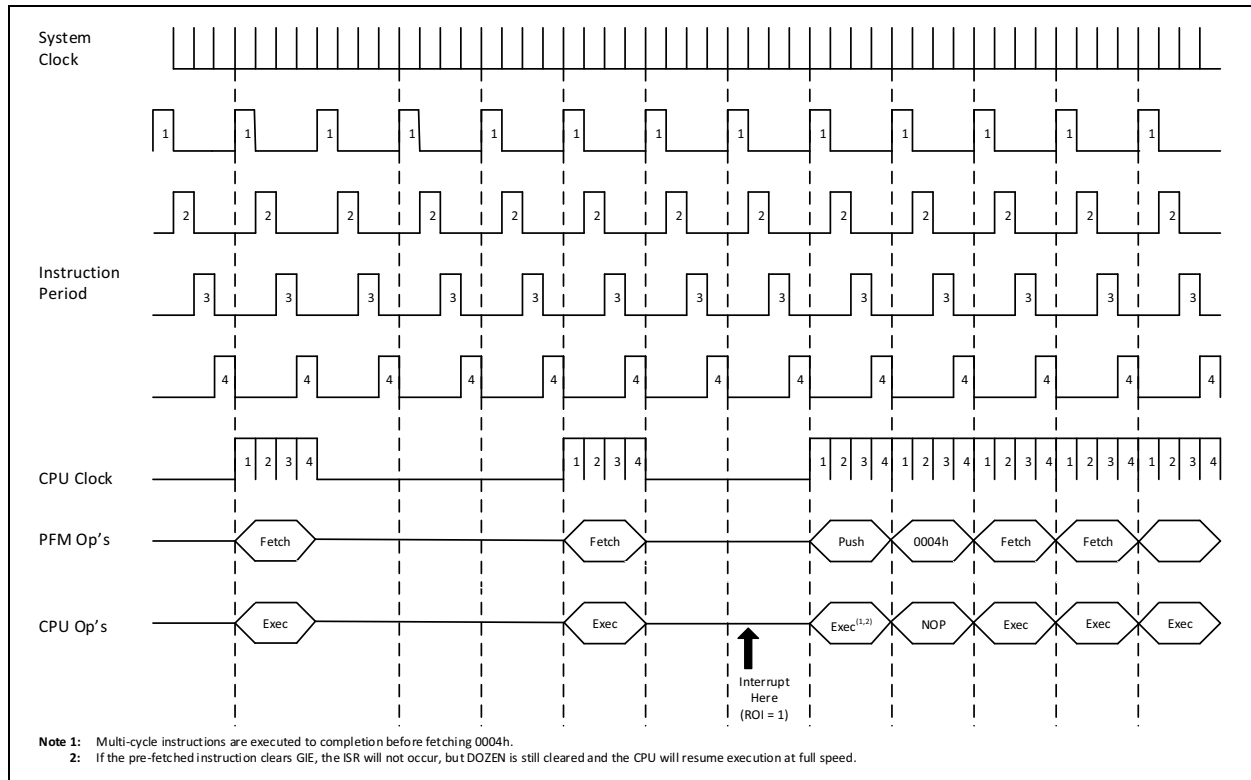
11.1 DOZE Mode

DOZE mode allows for power saving by reducing CPU operation and program memory (PFM) access, without affecting peripheral operation. DOZE mode differs from Sleep mode because the system oscillators continue to

operate, while only the CPU and PFM are affected. The reduced execution saves power by eliminating unnecessary operations within the CPU and memory.

When the Doze Enable (DOZEN) bit is set (DOZEN = 1), the CPU executes only one instruction cycle out of every N cycles as defined by the DOZE<2:0> bits of the CPUDOZE register. For example, if DOZE<2:0> = 100, the instruction cycle ratio is 1:32. The CPU and memory execute for one instruction cycle and then lay idle for 31 instruction cycles. During the unused cycles, the peripherals continue to operate at the system clock speed.

FIGURE 11-1: DOZE MODE OPERATION EXAMPLE



11.1.1 DOZE OPERATION

The Doze operation is illustrated in Figure 11-1. For this example:

- Doze enable (DOZEN) bit set (DOZEN = 1)
- DOZE<2:0> = 001 (1:4) ratio
- Recover-on-Interrupt (ROI) bit set (ROI = 1)

As with normal operation, the PFM fetches for the next instruction cycle. The Q-clocks to the peripherals continue throughout.

REGISTER 12-2: WDTCON1: WATCHDOG TIMER CONTROL REGISTER 1

| | | | | | | | |
|-------|--|--|--|-------|--|--|--|
| U-0 | R/W ⁽³⁾ -q/q ⁽¹⁾ | R/W ⁽³⁾ -q/q ⁽¹⁾ | R/W ⁽³⁾ -q/q ⁽¹⁾ | U-0 | R/W ⁽⁴⁾ -q/q ⁽²⁾ | R/W ⁽⁴⁾ -q/q ⁽²⁾ | R/W ⁽⁴⁾ -q/q ⁽²⁾ |
| — | WDTCS<2:0> | | | — | WINDOW<2:0> | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **WDTCS<2:0>:** Watchdog Timer Clock Select bits

111 = Reserved

•

•

•

010 = SOSC 32 kHz

001 = MFINTOSC 31.25 kHz

000 = LFINTOSC 31 kHz

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WINDOW<2:0>:** Watchdog Timer Window Select bits

| WINDOW<2:0> | Window delay Percent of time | Window opening Percent of time |
|-------------|---------------------------------|-----------------------------------|
| 111 | N/A | 100 |
| 110 | 12.5 | 87.5 |
| 101 | 25 | 75 |
| 100 | 37.5 | 62.5 |
| 011 | 50 | 50 |
| 010 | 62.5 | 37.5 |
| 001 | 75 | 25 |
| 000 | 87.5 | 12.5 |

Note 1: If WDTCCS <2:0> in CONFIG3 = 111, the Reset value of WDTCS<2:0> is 000.

2: The Reset value of WINDOW<2:0> is determined by the value of WDTCCS<2:0> in the CONFIG3 register.

3: If WDTCCS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

4: If WDTCCS<2:0> in CONFIG3 ≠ 111, these bits are read-only.

13.0 NONVOLATILE MEMORY (NVM) CONTROL

NVM consists of the Program Flash Memory (PFM).

NVM is accessible by using both the FSR and INDF registers, or through the NVMREG register interface.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

NVM can be protected in two ways; by either code protection or write protection.

Code protection (\overline{CP} bit in Configuration Word 5) disables access, reading and writing, to the PFM via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be Reset by a device programmer performing a Bulk Erase to the device, clearing all nonvolatile memory, Configuration bits, and User IDs.

Write protection prohibits self-write and erase to a portion or all of the PFM, as defined by the WRT<1:0> bits of Configuration Word 4. Write protection does not affect a device programmer's ability to read, write, or erase the device.

13.1 Program Flash Memory (PFM)

PFM consists of an array of 14-bit words as user memory, with additional words for User ID information, Configuration words, and interrupt vectors. PFM provides storage locations for:

- User program instructions
- User defined data

PFM data can be read and/or written to through:

- CPU instruction fetch (read-only)
- FSR/INDF indirect access (read-only)
(Section 13.2 "FSR and INDF Access")
- NVMREG access (Section 13.3 "NVMREG Access")
- In-Circuit Serial Programming™ (ICSP™)

Read operations return a single word of memory. When write and erase operations are done on a row basis, the row size is defined in Table 13-1. PFM will erase to a logic '1' and program to a logic '0'.

TABLE 13-1: FLASH MEMORY ORGANIZATION BY DEVICE

| Device | Row Erase (words) | Write Latches (words) | Total Program Flash (words) |
|----------------|-------------------|-----------------------|-----------------------------|
| PIC16(L)F15325 | 32 | 32 | 8192 |
| PIC16(L)F15345 | | | 8192 |

It is important to understand the PFM memory structure for erase and programming operations. PFM is arranged in rows. A row consists of 32 14-bit program memory words. A row is the minimum size that can be erased by user software.

All or a portion of this row can be programmed. Data to be written into the program memory row is written to 14-bit wide data write latches. These latches are not directly accessible, but may be loaded via sequential writes to the NVMDATH:NVMDATL register pair.

Note: To modify only a portion of a previously programmed row, the contents of the entire row must be read. Then, the new data and retained data can be written into the write latches to reprogram the row of PFM. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations

13.1.1 PROGRAM MEMORY VOLTAGES

The PFM is readable and writable during normal operation over the full VDD range.

13.1.1.1 Programming Externally

The program memory cell and control logic support write and Bulk Erase operations down to the minimum device operating voltage. Special BOR operation is enabled during Bulk Erase (Section 8.2.4 "BOR is always OFF").

13.1.1.2 Self-programming

The program memory cell and control logic will support write and row erase operations across the entire VDD range. Bulk Erase is not available when self-programming.

REGISTER 14-13: WPUB: WEAK PULL-UP PORTB REGISTER

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | U-0 |
|---------|---------|---------|---------|-------|-----|-----|-----|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | — | — | — | — |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **WPUB<7:4>**: Weak Pull-up Register bits

1 = Pull-up enabled

0 = Pull-up disabled

bit 3-0 **Unimplemented**: Read as '0'

REGISTER 14-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | U-0 |
|---------|---------|---------|---------|-------|-----|-----|-----|
| ODCB7 | ODCB6 | ODCB5 | ODCB4 | — | — | — | — |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **ODCB<7:4>**: PORTB Open-Drain Enable bits

For RB<7:4> pins, respectively

1 = Port pin operates as open-drain drive (sink current only)

0 = Port pin operates as standard push-pull drive (source and sink current)

bit 3-0 **Unimplemented**: Read as '0'

20.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
 - Disable pin output driver (Refer to the TRIS register)
 - Configure pin as analog (Refer to the ANSEL register)
2. Configure the ADC module:
 - Select ADC conversion clock
 - Select voltage reference
 - Select ADC input channel
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

EXAMPLE 20-1: ADC CONVERSION

```

;This code block configures the ADC
;for polling, Vdd and Vss references, ADCRC
;oscillator and AN0 input.
;
;Conversion start & polling for completion ;
;are included.
;
BANKSEL    ADCON1        ;
MOVLW      B'11110000'    ;Right justify, ADCRC
                                ;oscillator
MOVWF      ADCON1        ;Vdd and Vss Vref
BANKSEL    TRISA         ;
BSF        TRISA,0        ;Set RA0 to input
BANKSEL    ANSEL         ;
BSF        ANSEL,0        ;Set RA0 to analog
BANKSEL    ADCON0        ;
MOVLW      B'00000001'    ;Select channel AN0
MOVWF      ADCON0        ;Turn ADC On
CALL       SampleTime     ;Acquisiton delay
BSF        ADCON0,ADGO    ;Start conversion
BTFSC      ADCON0,ADGO    ;Is conversion done?
GOTO       $-1            ;No, test again
BANKSEL    ADRESH        ;
MOV        ADRESH,W       ;Read upper 2 bits
MOVWF      RESULTHI       ;store in GPR space
BANKSEL    ADRESL        ;
MOV        ADRESL,W       ;Read lower 8 bits
MOVWF      RESULTLO       ;Store in GPR space

```

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 20.3 “ADC Acquisition Requirements”**.

21.4 Operation During Sleep

The DAC continues to function during Sleep. When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DAC1CON0 register are not affected.

21.5 Effects of a Reset

A device Reset affects the following:

- DAC is disabled.
- DAC output voltage is removed from the DAC1OUT1/2 pins.
- The DAC1R<4:0> range select bits are cleared.

22.0 NUMERICALLY CONTROLLED OSCILLATOR (NCO) MODULE

The Numerically Controlled Oscillator (NCO) module is a timer that uses overflow from the addition of an increment value to divide the input frequency. The advantage of the addition method over simple counter driven timer is that the output frequency resolution does not vary with the divider value. The NCO is most useful for application that requires frequency accuracy and fine resolution at a fixed duty cycle.

Features of the NCO include:

- 20-bit Increment Function
- Fixed Duty Cycle mode (FDC) mode
- Pulse Frequency (PF) mode
- Output Pulse Width Control
- Multiple Clock Input Sources
- Output Polarity Control
- Interrupt Capability

Figure 22-1 is a simplified block diagram of the NCO module.

25.2 Clock Source Selection

The T0CS<2:0> bits of the T0CON1 register are used to select the clock source for Timer0. Register 25-2 displays the clock source selections.

25.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, Timer0 operates as a timer and will increment on multiples of the clock source, as determined by the Timer0 prescaler.

25.2.2 EXTERNAL CLOCK SOURCE

When an external clock source is selected, Timer0 can operate as either a timer or a counter. Timer0 will increment on multiples of the rising edge of the external clock source, as determined by the Timer0 prescaler.

25.3 Programmable Prescaler

A software programmable prescaler is available for exclusive use with Timer0. There are 16 prescaler options for Timer0 ranging in powers of two from 1:1 to 1:32768. The prescaler values are selected using the T0CKPS<3:0> bits of the T0CON1 register.

The prescaler is not directly readable or writable. Clearing the prescaler register can be done by writing to the TMR0L register or the T0CON1 register.

25.4 Programmable Postscaler

A software programmable postscaler (output divider) is available for exclusive use with Timer0. There are 16 postscaler options for Timer0 ranging from 1:1 to 1:16. The postscaler values are selected using the T0OUTPS<3:0> bits of the T0CON0 register.

The postscaler is not directly readable or writable. Clearing the postscaler register can be done by writing to the TMR0L register or the T0CON0 register.

25.5 Operation during Sleep

When operating synchronously, Timer0 will halt. When operating asynchronously, Timer0 will continue to increment and wake the device from Sleep (if Timer0 interrupts are enabled) provided that the input clock source is active.

25.6 Timer0 Interrupts

The Timer0 interrupt flag bit (TMR0IF) is set when either of the following conditions occur:

- 8-bit TMR0L matches the TMR0H value
- 16-bit TMR0 rolls over from 'FFFFh'

When the postscaler bits (T0OUTPS<3:0>) are set to 1:1 operation (no division), the T0IF flag bit will be set with every TMR0 match or rollover. In general, the TMR0IF flag bit will be set every T0OUTPS + 1 matches or rollovers.

If Timer0 interrupts are enabled (TMR0IE bit of the PIE0 register = 1), the CPU will be interrupted and the device may wake from sleep (see **Section 25.2 “Clock Source Selection”** for more details).

25.7 Timer0 Output

The Timer0 output can be routed to any I/O pin via the RxyPPS output selection register (see **Section 15.0 “Peripheral Pin Select (PPS) Module”** for additional information). The Timer0 output can also be used by other peripherals, such as the Auto-conversion Trigger of the Analog-to-Digital Converter. Finally, the Timer0 output can be monitored through software via the Timer0 output bit (T0OUT) of the T0CON0 register (Register 25-1).

TMR0_out will be one postscaled clock period when a match occurs between TMR0L and TMR0H in 8-bit mode, or when TMR0 rolls over in 16-bit mode. The Timer0 output is a 50% duty cycle that toggles on each TMR0_out rising clock edge.

28.2.1 CCPX PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 15.0 “Peripheral Pin Select (PPS) Module”** for more details.

The CCP output can also be used as an input for other peripherals.

Note: Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

28.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 26.0 “Timer1 Module with Gate Control”** for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

28.2.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxFIF). When this flag is set and a match occurs, an Auto-conversion Trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to **Section 20.2.5 “Auto-Conversion Trigger”** for more information.

Note: Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring

28.2.4 COMPARE DURING SLEEP

Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

28.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 28-3 shows a typical waveform of the PWM signal.

28.3.1 STANDARD PWM OPERATION

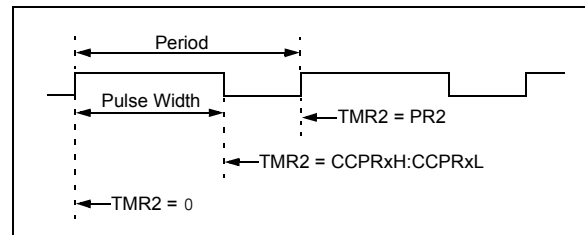
The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 28-4 shows a simplified block diagram of PWM operation.

Note: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

FIGURE 28-3: CCP PWM OUTPUT SIGNAL



30.1.2 PUSH-PULL MODE

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 30-2. This alternation creates the push-pull effect required for driving some transformer-based power supply designs.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWG1A.

The unused outputs CWG1C and CWG1D drive copies of CWG1A and CWG1B, respectively, but with polarity controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

30.1.3 FULL-BRIDGE MODES

In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth is modulated by the input data signal. In Forward Full-Bridge mode, CWG1A is driven to its active state, CWG1B and CWG1C are driven to their inactive state, and CWG1D is modulated by the input signal. In Reverse Full-Bridge mode, CWG1C is driven to its active state, CWG1A and CWG1D are driven to their inactive states, and CWG1B is modulated by the input signal. In Full-Bridge mode, the dead-band period is used when there is a switch from forward to reverse or vice-versa. This dead-band control is described in **Section 30.5 “Dead-Band Control”**, with additional details in **Section 30.6 “Rising Edge and Reverse Dead Band”** and **Section 30.7 “Falling Edge and Forward Dead Band”**.

The mode selection may be toggled between forward and reverse toggling the MODE<0> bit of the CWG1CON0 while keeping MODE<2:1> static, without disabling the CWG module.

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FIGURE 30-12: CWG SHUTDOWN BLOCK DIAGRAM

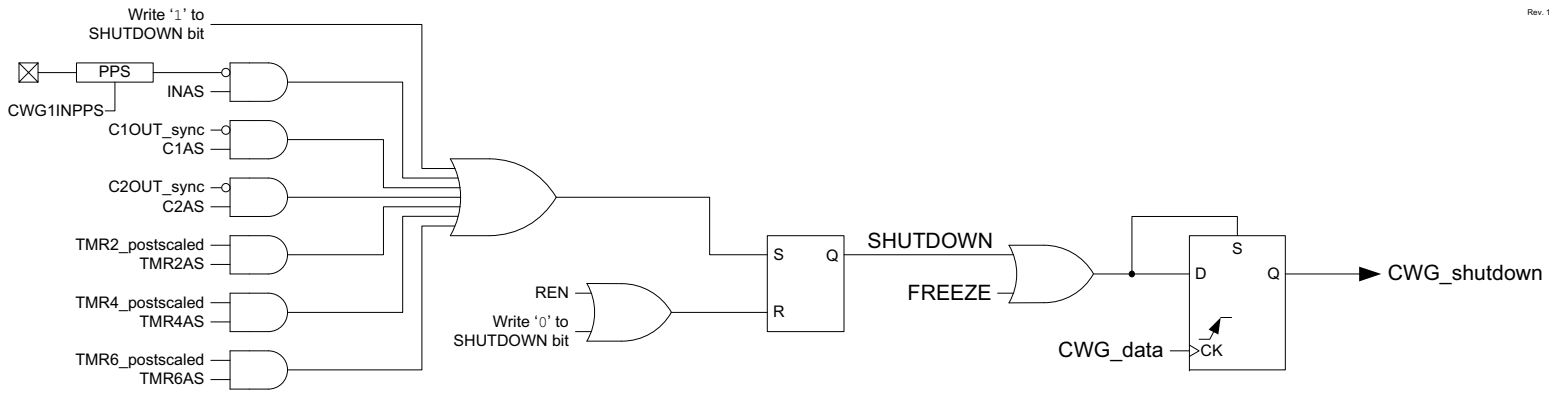


TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH CWG

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|------------|----------|-------|-----------|-------|-----------|-----------|-------|-------|------------------|
| CWG1CLKCON | — | — | — | — | — | — | — | CS | 356 |
| CWG1ISM | — | — | — | — | IS<3:0> | | | | 356 |
| CWG1DBR | — | — | DBR<5:0> | | | | | | 352 |
| CWG1DBF | — | — | DBF<5:0> | | | | | | 352 |
| CWG1CON0 | EN | LD | — | — | — | MODE<2:0> | | | 355 |
| CWG1CON1 | — | — | IN | — | POLD | POLC | POLB | POLA | 351 |
| CWG1AS0 | SHUTDOWN | REN | LSBD<1:0> | | LSAC<1:0> | | — | — | 353 |
| CWG1AS1 | — | — | — | AS4E | AS3E | AS2E | AS1E | AS0E | 354 |
| CWG1STR | OVRD | OVRC | OVRB | OVRA | STRD | STRC | STRB | STRA | 355 |

Legend: — = unimplemented locations read as '0'. Shaded cells are not used by CWG.

32.5.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSP module configured as an I²C slave in 10-bit Addressing mode.

Figure 32-20 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I²C communication.

1. Bus starts Idle.
2. Master sends Start condition; S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Master sends matching high address with R/W bit clear; UA bit of the SSP1STAT register is set.
4. Slave sends \overline{ACK} and SSP1IF is set.
5. Software clears the SSP1IF bit.
6. Software reads received address from SSP1BUF clearing the BF flag.
7. Slave loads low address into SSP1ADD, releasing SCL.
8. Master sends matching low address byte to the slave; UA bit is set.

Note: Updates to the SSP1ADD register are not allowed until after the ACK sequence.

9. Slave sends \overline{ACK} and SSP1IF is set.

Note: If the low address does not match, SSP1IF and UA are still set so that the slave software can set SSP1ADD back to the high address. BF is not set because there is no match. CKP is unaffected.

10. Slave clears SSP1IF.
11. Slave reads the received matching address from SSP1BUF clearing BF.
12. Slave loads high address into SSP1ADD.
13. Master clocks a data byte to the slave and clocks out the slaves ACK on the ninth SCL pulse; SSP1IF is set.
14. If SEN bit of SSP1CON2 is set, CKP is cleared by hardware and the clock is stretched.
15. Slave clears SSP1IF.
16. Slave reads the received byte from SSP1BUF clearing BF.
17. If SEN is set the slave sets CKP to release the SCL.
18. Steps 13-17 repeat for each received byte.
19. Master sends Stop to end the transmission.

32.5.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSP1ADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCL line is held low are the same. Figure 32-21 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 32-22 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.

REGISTER 32-3: SSP1CON2: SSP1 CONTROL REGISTER 2 (I²C MODE ONLY)⁽¹⁾

| | | | | | | | |
|---------|-----------|---------|------------|------------|------------|------------|------------|
| R/W-0/0 | R/HS/HC-0 | R/W-0/0 | R/S/HC-0/0 | R/S/HC-0/0 | R/S/HC-0/0 | R/S/HC-0/0 | R/S/HC-0/0 |
| GCEN | ACKSTAT | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|----------------------|----------------------|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HC = Cleared by hardware S = User set |

- bit 7 **GCEN:** General Call Enable bit (in I²C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSP1SR
0 = General call address disabled
- bit 6 **ACKSTAT:** Acknowledge Status bit (in I²C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received
- bit 5 **ACKDT:** Acknowledge Data bit (in I²C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I²C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit.
Automatically cleared by hardware.
0 = Acknowledge sequence idle
- bit 3 **RCEN:** Receive Enable bit (in I²C Master mode only)
1 = Enables Receive mode for I²C
0 = Receive idle
- bit 2 **PEN:** Stop Condition Enable bit (in I²C Master mode only)
SCKMSSP Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle
- bit 1 **RSEN:** Repeated Start Condition Enable bit (in I²C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle
- bit 0 **SEN:** Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the IDLE mode, this bit may not be set (no spooling) and the SSP1BUF may not be written (or writes to the SSP1BUF are disabled).

37.0 ELECTRICAL SPECIFICATIONS

37.1 Absolute Maximum Ratings^(†)

| | |
|---|-----------------------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on pins with respect to V _{SS} | |
| on V _{DD} pin | |
| PIC16F15325/45 | -0.3V to +6.5V |
| PIC16LF15325/45 | -0.3V to +4.0V |
| on MCLR pin | -0.3V to +9.0V |
| on all other pins | -0.3V to (V _{DD} + 0.3V) |
| Maximum current | |
| on V _{SS} pin ⁽¹⁾ | |
| -40°C ≤ T _A ≤ +85°C | 250 mA |
| 85°C < T _A ≤ +125°C | 85 mA |
| on V _{DD} pin ⁽¹⁾ | |
| -40°C ≤ T _A ≤ +85°C | 250 mA |
| 85°C < T _A ≤ +125°C | 85 mA |
| on any standard I/O pin | ±50 mA |
| Clamp current, I _K (V _{PIN} < 0 or V _{PIN} > V _{DD}) | ±20 mA |
| Total power dissipation ⁽²⁾ | 800 mW |

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 37-6 to calculate device specifications.

2: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OI} \times I_{OL})$$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.