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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15345-e-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15345-e-so</a>

**TABLE 1-3: PIC16(L)F15345 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
OUT <sup>(2)</sup>	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	DT1 <sup>(3)</sup>	—	CMOS/OD	EUSART Synchronous mode data output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	DT2 <sup>(3)</sup>	—	CMOS/OD	EUSART Synchronous mode data output.
	TX2	—	CMOS/OD	EUSART2 Asynchronous mode transmitter data output.
	CK2	—	CMOS/OD	EUSART2 Synchronous mode clock output.
	SCL1 <sup>(3,4)</sup>	—	CMOS/OD	MSSP1 I <sup>2</sup> C output.
	SDA1 <sup>(3,4)</sup>	—	CMOS/OD	MSSP1 I <sup>2</sup> C output.
	DT1 <sup>(3)</sup>	—	CMOS/OD	EUSART Synchronous mode data output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP1 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
	NCO1OUT	—	CMOS/OD	Numerically Controller Oscillator output.
	CLKR	—	CMOS/OD	Clock Reference module output.

**Legend:** AN = Analog input or output      CMOS = CMOS compatible input or output      OD = Open-Drain  
TTL = TTL compatible input      ST = Schmitt Trigger input with CMOS levels      I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage      XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.
  - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBus input buffer thresholds.
  - 5: For 14/16-pin package only.
  - 6: For 20-pin package only.

**TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
<b>Bank 60</b>											
CPU CORE REGISTERS; see Table 4-3 for specifics											
1E0Ch	—	Unimplemented								—	—
1E0Dh	—	Unimplemented								—	—
1E0Eh	—	Unimplemented								—	—
1E0Fh	CLCDATA	—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT	---- xxxx	---- uuuu
1E10h	CLCCON	LC1EN	—	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			0-00 0000	0-00 0000
1E11h	CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	0--- xxxx	0--- uuuu
1E12h	CLC1SEL0	—	—	LC1D1S<5:0>						--xx xxxx	--uu uuuu
1E13h	CLC1SEL1	—	—	LC1D2S<5:0>						--xx xxxx	--uu uuuu
1E14h	CLC1SEL2	—	—	LC1D3S<5:0>						--xx xxxx	--uu uuuu
1E15h	CLC1SEL3	—	—	LC1D4S<5:0>						--xx xxxx	--uu uuuu
1E16h	CLC1GLS0	LC1G1D4T	LC1G4D3N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	xxxx xxxx	uuuu uuuu
1E17h	CLC1GLS1	LC1G2D4T	LC1G4D3N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	xxxx xxxx	uuuu uuuu
1E18h	CLC1GLS2	LC1G3D4T	LC1G4D3N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	xxxx xxxx	uuuu uuuu
1E19h	CLC1GLS3	LC1G4D4T	LC1G4D3N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	xxxx xxxx	uuuu uuuu
1E1Ah	CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	LC2MODE<2:0>			0-00 0000	0-00 0000
1E1Bh	CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	0--- xxxx	0--- uuuu
1E1Ch	CLC2SEL0	—	—	LC2D1S<5:0>						--xx xxxx	--uu uuuu
1E1Dh	CLC2SEL1	—	—	LC2D2S<5:0>						--xx xxxx	--uu uuuu
1E1Eh	CLC2SEL2	—	—	LC2D3S<5:0>						--xx xxxx	--uu uuuu
1E1Fh	CLC2SEL3	—	—	LC2D4S<5:0>						--xx xxxx	--uu uuuu
1E20h	CLC2GLS0	LC2G1D4T	LC2G4D3N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	xxxx xxxx	uuuu uuuu
1E21h	CLC2GLS1	LC2G2D4T	LC2G4D3N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	xxxx xxxx	uuuu uuuu
1E22h	CLC2GLS2	LC2G3D4T	LC2G4D3N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	xxxx xxxx	uuuu uuuu
1E23h	CLC2GLS3	LC2G4D4T	LC2G4D3N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	xxxx xxxx	uuuu uuuu
1E24h	CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE			0-00 0000	0-00 0000
1E25h	CLC3POL	LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	0--- xxxx	0--- uuuu
1E26h	CLC3SEL0	—	—	LC3D1S<5:0>						--xx xxxx	--uu uuuu
1E27h	CLC3SEL1	—	—	LC3D2S<5:0>						--xx xxxx	--uu uuuu
1E28h	CLC3SEL2	—	—	LC3D3S<5:0>						--xx xxxx	--uu uuuu
1E29h	CLC3SEL3	—	—	LC3D4S<5:0>						--xx xxxx	--uu uuuu
1E2Ah	CLC3GLS0	LC3G1D4T	LC3G4D3N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	xxxx xxxx	uuuu uuuu

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

## REGISTER 5-7: REVISIONID: REVISION ID REGISTER

R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
1	0	MJRREV<5:0>							MNRREV<5:0>						
bit 13															bit 0

### Legend:

R = Readable bit

'0' = Bit is cleared

'1' = Bit is set

x = Bit is unknown

bit 13-12 **Fixed Value:** Read-only bits

These bits are fixed with value '10' for all devices included in this data sheet.

bit 11-6 **MJRREV<5:0>:** Major Revision ID bits

These bits are used to identify a major revision.

bit 5-0 **MNRREV<5:0>:** Minor Revision ID bits

These bits are used to identify a minor revision.

## 8.3 Register Definitions: Brown-out Reset Control

**REGISTER 8-1: BORCON: BROWN-OUT RESET CONTROL REGISTER**

R/W-1/u	U-0	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN <sup>(1)</sup>	—	—	—	—	—	—	BORRDY
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

- bit 7      **SBOREN:** Software Brown-out Reset Enable bit<sup>(1)</sup>  
             If BOREN <1:0> in Configuration Words ≠ 01:  
             SBOREN is read/write, but has no effect on the BOR.  
             If BOREN <1:0> in Configuration Words = 01:  
             1 = BOR Enabled  
             0 = BOR Disabled
- bit 6-1    **Unimplemented:** Read as '0'
- bit 0      **BORRDY:** Brown-out Reset Circuit Ready Status bit  
             1 = The Brown-out Reset circuit is active  
             0 = The Brown-out Reset circuit is inactive

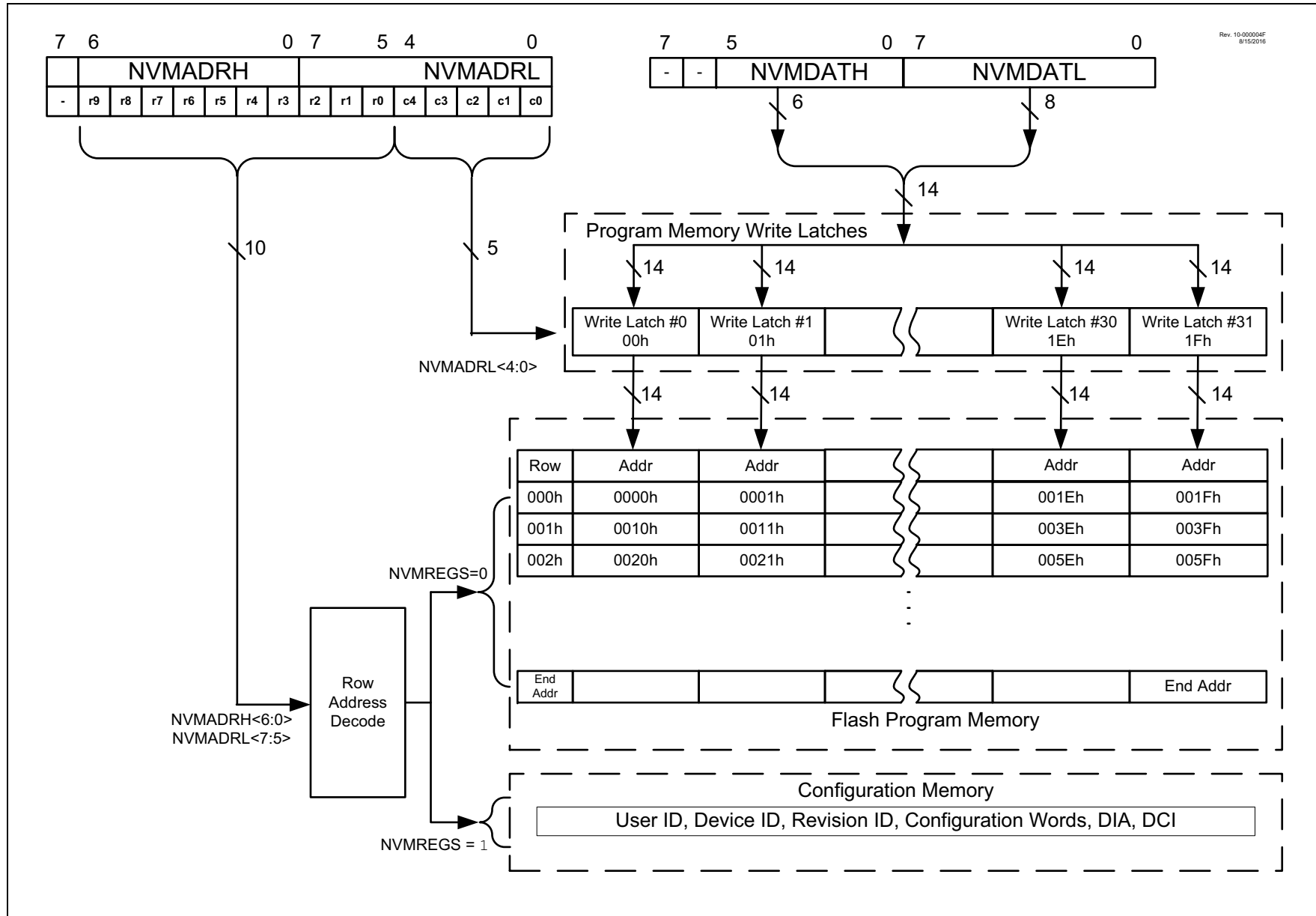
**Note 1:** BOREN<1:0> bits are located in Configuration Words.

## 8.12 Memory Execution Violation

A Memory Execution Violation Reset occurs if executing an instruction being fetched from outside the valid execution area. The different valid execution areas are defined as follows:

- Flash Memory: Table 4-1 shows the addresses available on the PIC16(L)F15325/45 devices based on user Flash size. Execution outside this region generates a memory execution violation.
- Storage Area Flash (SAF): If Storage Area Flash (SAF) is enabled (**Section 4.2.3 “Storage Area Flash”**), the SAF area (Table 4-2) is not a valid execution area.

Prefetched instructions that are not executed do not cause memory execution violations. For example, a GOTO instruction in the last memory location will prefetch from an invalid location; this is not an error. If an instruction from an invalid location tries to execute, the memory violation is generated immediately, and any concurrent interrupt requests are ignored. When a memory execution violation is generated, the device is reset and flag MEMV is cleared in PCON1 (Register 8-3) to signal the cause. The flag needs to be set in code after a memory execution violation.

**FIGURE 13-4: NVMREGS WRITES TO PROGRAM FLASH MEMORY WITH 32 WRITE LATCHES**

**TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	124
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	125
IOCAP	IOCAP7 <sup>(1)</sup>	IOCAP6 <sup>(1)</sup>	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	213
IOCAN	IOCAN7 <sup>(1)</sup>	IOCAN6 <sup>(1)</sup>	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	213
IOCAF	IOCAF7 <sup>(1)</sup>	IOCAF6 <sup>(1)</sup>	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	214
IOCBP <sup>(1)</sup>	IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—	215
IOCBN <sup>(1)</sup>	IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—	215
IOCBF <sup>(1)</sup>	IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	—	216
IOCCP	IOCCP7 <sup>(1)</sup>	IOCCP6 <sup>(1)</sup>	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	217
IOCCN	IOCCN7 <sup>(1)</sup>	IOCCN6 <sup>(1)</sup>	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	217
IOCCF	IOCCF7 <sup>(1)</sup>	IOCCF6 <sup>(1)</sup>	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	217

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.

**Note 1:** Present only in PIC16(L)F15345.



## 23.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See Comparator Specifications in Table 37-14 for more information.

## 23.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 26.6 “Timer Gate”** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

### 23.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the CxSYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 23-2) and the Timer1 Block Diagram (Figure 26-1) for more information.

## 23.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- CxON, CxPOL and CxSP bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- CxINTP bit of the CMxCON1 register (for a rising edge detection)
- CxINTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

**Note:** Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit of the CMxCON0 register, or by switching the comparator on or off with the CxON bit of the CMxCON0 register.

## 23.6 Comparator Positive Input Selection

Configuring the CxPCH<2:0> bits of the CMxPSEL register directs an internal voltage reference or an analog pin to the noninverting input of the comparator:

- CxIN0+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- Vss (Ground)

See **Section 18.0 “Fixed Voltage Reference (FVR)”** for more information on the Fixed Voltage Reference module.

See **Section 21.0 “5-Bit Digital-to-Analog Converter (DAC1) Module”** for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

## 23.7 Comparator Negative Input Selection

The CxNCH<2:0> bits of the CMxCON1 register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- CxIN- pin
- FVR (Fixed Voltage Reference)
- Analog Ground

**Note:** To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

## EXAMPLE 24-1:

$V_{RMS} = 120$   
 $V_{PEAK} = V_{RMS} \cdot \sqrt{2} = 169.7$   
 $f = 60 \text{ Hz}$   
 $C = 0.1 \text{ }\mu\text{F}$   
 $Z = V_{PEAK} / (3 \times 10^{-4}) = 169.7 / (3 \times 10^{-4}) = 565.7 \text{ k}\Omega$   
 $X_C = 1 / (2\pi f C) = 1 / (2\pi \cdot 60 \cdot 1 \times 10^{-7}) = 26.53 \text{ k}\Omega$   
 $R = \sqrt{Z^2 - X_C^2} = 565.1 \text{ k}\Omega$  (computed)  
 $R = 560 \text{ k}\Omega$  (used)  
 $Z_R = \sqrt{R^2 + X_C^2} = 560.6 \text{ k}\Omega$  (using actual resistor)  
 $I_{PEAK} = V_{PEAK} / Z_R = 302.7 \times 10^{-6}$   
 $V_C = X_C \cdot I_{PEAK} = 8.0 \text{ V}$   
 $\Phi = \tan^{-1}(X_C / R) = 0.047 \text{ radians}$   
 $T_\Phi = \Phi / (2\pi f) = 125.6 \text{ }\mu\text{s}$

## 24.5.2 CORRECTION BY OFFSET CURRENT

When the waveform is varying relative to V<sub>SS</sub>, then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to V<sub>DD</sub>, then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 24-3.

### EQUATION 24-3: ZCD EVENT OFFSET

When External Voltage Source is relative to V<sub>SS</sub>:

$$T_{OFFSET} = \frac{\arcsin\left(\frac{V_{cpinv}}{V_{PEAK}}\right)}{2\pi \cdot Freq}$$

When External Voltage Source is relative to V<sub>DD</sub>:

$$T_{OFFSET} = \frac{\arcsin\left(\frac{V_{DD} - V_{cpinv}}{V_{PEAK}}\right)}{2\pi \cdot Freq}$$

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to V<sub>SS</sub>. A pull-down resistor is used when the voltage is varying relative to V<sub>DD</sub>. The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the V<sub>CPINV</sub> switching voltage. The pull-up or pull-down value can be determined with the equation shown in Equation 24-4.

### EQUATION 24-4: ZCD PULL-UP/DOWN

When External Signal is relative to V<sub>SS</sub>:

$$R_{PULLUP} = \frac{R_{SERIES}(V_{PULLUP} - V_{cpinv})}{V_{cpinv}}$$

When External Signal is relative to V<sub>DD</sub>:

$$\left( R_{PULLDOWN} = \frac{R_{SERIES} \times (V_{cpinv})}{(V_{DD} - V_{cpinv})} \right)$$

## 24.6 Handling V<sub>PEAK</sub> variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of  $\pm 600 \text{ }\mu\text{A}$  and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed  $\pm 600 \text{ }\mu\text{A}$  and the minimum is at least  $\pm 100 \text{ }\mu\text{A}$ , compute the series resistance as shown in Equation 24-5. The compensating pull-up for this series resistance can be determined with Equation 24-4 because the pull-up value is not dependent from the peak voltage.

### EQUATION 24-5: SERIES R FOR V RANGE

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

## 26.3 Timer Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

## 26.4 Secondary Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins SOSC1 (input) and SOSCO (amplifier output). This internal circuit is designed to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the SOSSEN bit of the OSCEN register. The oscillator will continue to run during Sleep.

**Note:** The oscillator requires a start-up and stabilization time before use. Thus, SOSSEN should be set and a suitable delay observed prior to using Timer1 with the SOSC source. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

## 26.5 Timer Operation in Asynchronous Counter Mode

If the control bit SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 26.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”**).

**Note:** When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

### 26.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

## 26.6 Timer Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using the time gate circuitry. This is also referred to as Timer Gate Enable.

The timer gate can also be driven by multiple selectable sources.

### 26.6.1 TIMER GATE ENABLE

The Timer Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer Gate Enable signal is enabled, the timer will increment on the rising edge of the Timer1 clock source. When Timer Gate Enable signal is disabled, the timer always increments, regardless of the GE bit. See Figure 26-3 for timing details.

**TABLE 26-2: TIMER GATE ENABLE SELECTIONS**

T1CLK	T1GPOL	T1G	Timer Operation
↑	1	1	Counts
↑	1	0	Holds Count
↑	0	1	Holds Count
↑	0	0	Counts

## REGISTER 27-4: T2RST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	RSEL<3:0>			
bit 7				bit 0			

### Legend:

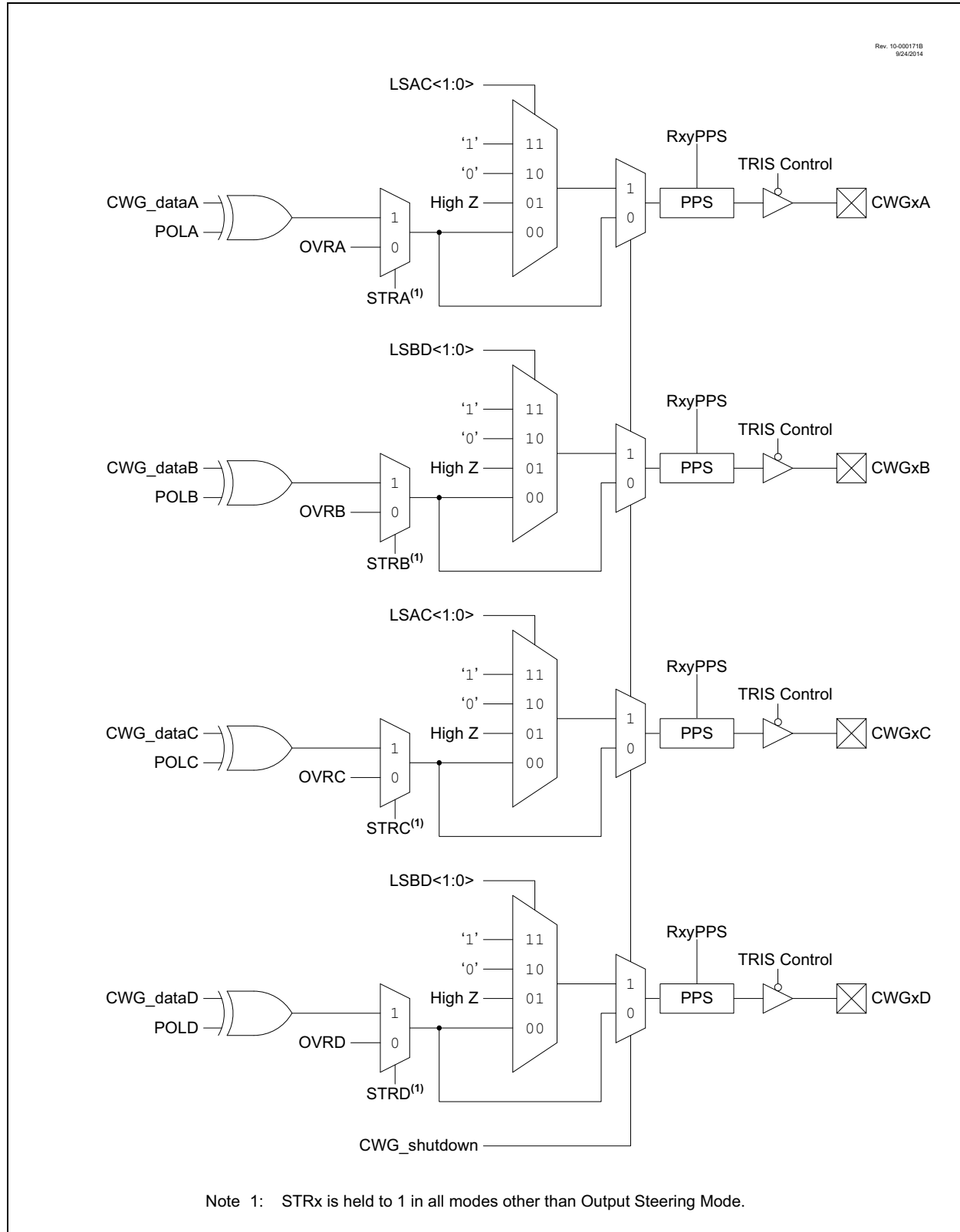
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RSEL<3:0>:** Timer2 External Reset Signal Source Selection bits

1111 = Reserved  
 1101 = LC4\_out  
 1100 = LC3\_out  
 1011 = LC2\_out  
 1010 = LC1\_out  
 1001 = ZCD1\_output  
 1000 = C2OUT\_sync  
 0111 = C1OUT\_sync  
 0110 = PWM6\_out  
 0101 = PWM5\_out  
 0100 = PWM4\_out  
 0011 = PWM3\_out  
 0010 = CCP2\_out  
 0001 = CCP1\_out  
 0000 = T2INPPS

**FIGURE 30-5: CWG OUTPUT BLOCK DIAGRAM**



## 32.6.10 SLEEP OPERATION

While in Sleep mode, the I<sup>2</sup>C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

## 32.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

## 32.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I<sup>2</sup>C bus may be taken when the P bit of the SSP1STAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

## 32.6.13 MULTI-MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I<sup>2</sup>C port to its Idle state (Figure 32-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSP1BUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a Start condition.

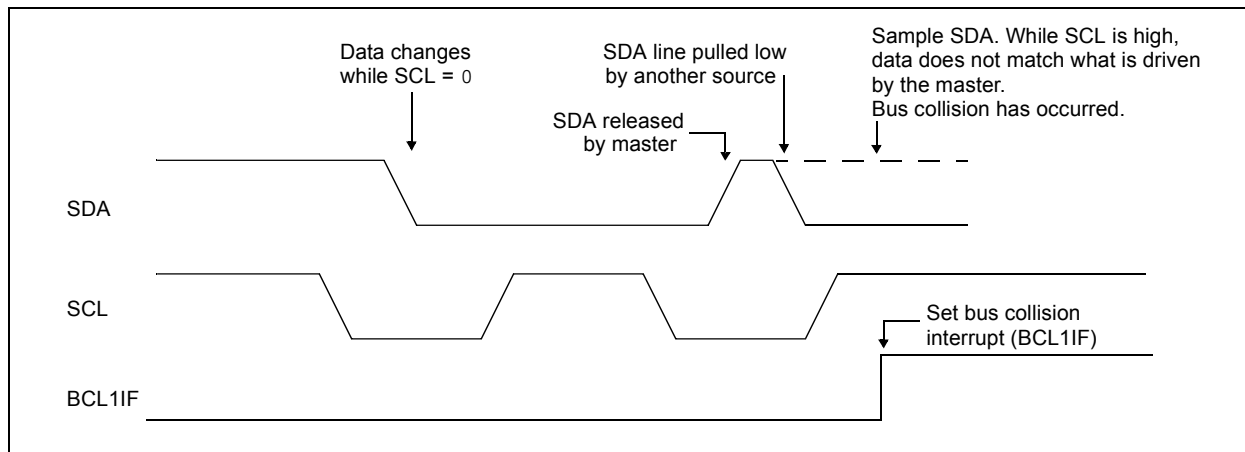
If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSP1CON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I<sup>2</sup>C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSP1IF bit will be set.

A write to the SSP1BUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I<sup>2</sup>C bus can be taken when the P bit is set in the SSP1STAT register, or the bus is Idle and the S and P bits are cleared.

**FIGURE 32-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE**



## REGISTER 32-5: SSP1MSK: SSP1 MASK REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SSP1MSK<7:0>							
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7-1 **SSP1MSK<7:1>**: Mask bits  
 1 = The received address bit n is compared to SSP1ADD<n> to detect I<sup>2</sup>C address match  
 0 = The received address bit n is not used to detect I<sup>2</sup>C address match
- bit 0 **SSP1MSK<0>**: Mask bit for I<sup>2</sup>C Slave mode, 10-bit Address  
I<sup>2</sup>C Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):  
 1 = The received address bit 0 is compared to SSP1ADD<0> to detect I<sup>2</sup>C address match  
 0 = The received address bit 0 is not used to detect I<sup>2</sup>C address match  
I<sup>2</sup>C Slave mode, 7-bit address:  
 MSK0 bit is ignored.

## REGISTER 32-6: SSP1ADD: MSSP1 ADDRESS AND BAUD RATE REGISTER (I<sup>2</sup>C MODE)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SSP1ADD<7:0>							
bit 7				bit 0			

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

### Master mode:

- bit 7-0 **SSP1ADD<7:0>**: Baud Rate Clock Divider bits  

$$\text{SCL pin clock period} = ((\text{ADD}<7:0> + 1) * 4) / \text{Fosc}$$

### 10-Bit Slave mode – Most Significant Address Byte:

- bit 7-3 **Not used**: Unused for Most Significant Address Byte. Bit state of this register is a “don't care”. Bit pattern sent by master is fixed by I<sup>2</sup>C specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.
- bit 2-1 **SSP1ADD<2:1>**: Two Most Significant bits of 10-bit address
- bit 0 **Not used**: Unused in this mode. Bit state is a “don't care”.

### 10-Bit Slave mode – Least Significant Address Byte:

- bit 7-0 **SSP1ADD<7:0>**: Eight Least Significant bits of 10-bit address

### 7-Bit Slave mode:

- bit 7-1 **SSP1ADD<7:1>**: 7-bit address
- bit 0 **Not used**: Unused in this mode. Bit state is a “don't care”.

## 36.2 General Format for Instructions

**TABLE 36-3: INSTRUCTION SET**

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	—	Clear W	1	00	0001	0000	00xx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	2
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	2
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		2
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	2
SUBWFB	f, d	Subtract with Borrow W from f	1	11	1011	dfff	ffff	C, DC, Z	2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	2
BYTE ORIENTED SKIP OPERATIONS									
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		2
BIT-ORIENTED SKIP OPERATIONS									
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
LITERAL OPERATIONS									
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	000	0k	kkkk		
MOVLPL	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

- Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.



## DECFSZ Decrement f, Skip if 0

**Syntax:** [ *label* ] DECFSZ f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) - 1 \rightarrow (\text{destination})$ ;  
skip if result = 0

**Status Affected:** None

**Description:** The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

## INCFSZ Increment f, Skip if 0

**Syntax:** [ *label* ] INCFSZ f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) + 1 \rightarrow (\text{destination})$ ,  
skip if result = 0

**Status Affected:** None

**Description:** The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

## GOTO Unconditional Branch

**Syntax:** [ *label* ] GOTO k

**Operands:**  $0 \leq k \leq 2047$

**Operation:**  $k \rightarrow PC<10:0>$   
 $PCLATH<6:3> \rightarrow PC<14:11>$

**Status Affected:** None

**Description:** GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

## IORLW Inclusive OR literal with W

**Syntax:** [ *label* ] IORLW k

**Operands:**  $0 \leq k \leq 255$

**Operation:**  $(W) .OR. k \rightarrow (W)$

**Status Affected:** Z

**Description:** The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

## INCF Increment f

**Syntax:** [ *label* ] INCF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(f) + 1 \rightarrow (\text{destination})$

**Status Affected:** Z

**Description:** The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

## IORWF Inclusive OR W with f

**Syntax:** [ *label* ] IORWF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**  $(W) .OR. (f) \rightarrow (\text{destination})$

**Status Affected:** Z

**Description:** Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

## MOVWI Move W to INDFn

**Syntax:** [ *label* ] MOVWI ++FSRn  
[ *label* ] MOVWI --FSRn  
[ *label* ] MOVWI FSRn++  
[ *label* ] MOVWI FSRn--  
[ *label* ] MOVWI k[FSRn]

**Operands:** n ∈ [0,1]  
mm ∈ [00,01, 10, 11]  
-32 ≤ k ≤ 31

**Operation:** W → INDFn  
Effective address is determined by

- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:

- FSR + 1 (all increments)
- FSR - 1 (all decrements)

Unchanged

**Status Affected:** None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

**Description:** This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

**Note:** The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

## NOP No Operation

**Syntax:** [ *label* ] NOP

**Operands:** None

**Operation:** No operation

**Status Affected:** None

**Description:** No operation.

**Words:** 1

**Cycles:** 1

**Example:** NOP

## RESET Software Reset

**Syntax:** [ *label* ] RESET

**Operands:** None

**Operation:** Execute a device Reset. Resets the RI flag of the PCON register.

**Status Affected:** None

**Description:** This instruction provides a way to execute a hardware Reset by software.

## RETFIE Return from Interrupt

**Syntax:** [ *label* ] RETFIE k

**Operands:** None

**Operation:** TOS → PC,  
1 → GIE

**Status Affected:** None

**Description:** Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.

**Words:** 1

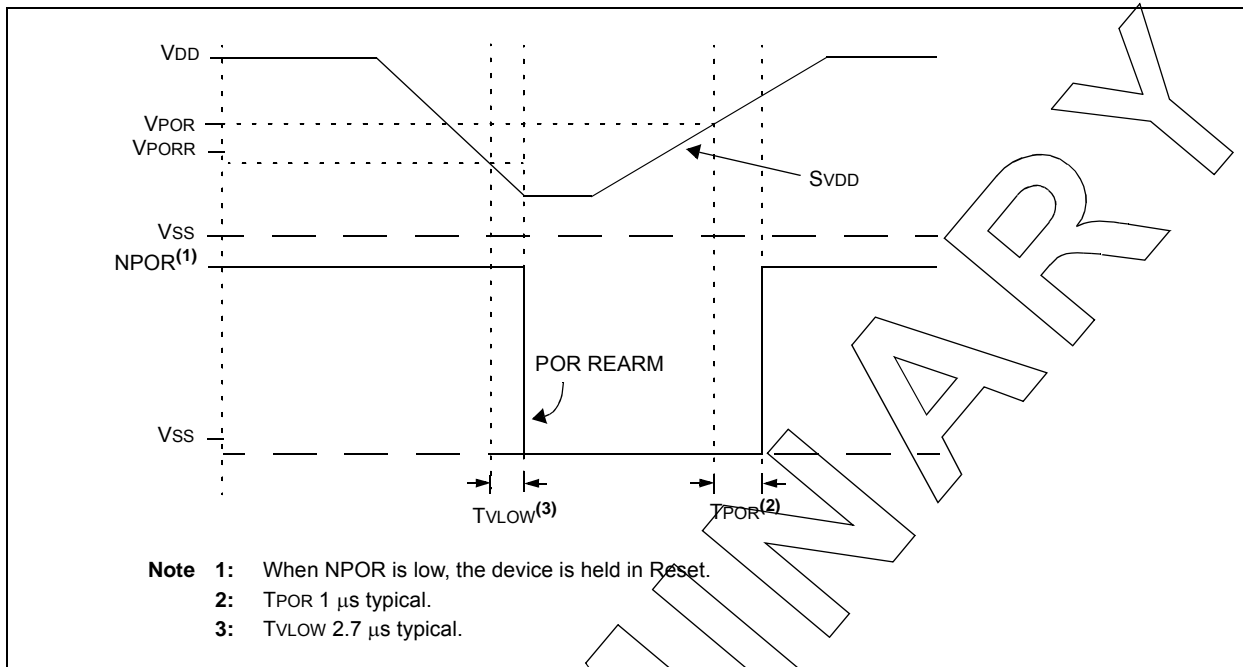
**Cycles:** 2

**Example:** RETFIE

After Interrupt

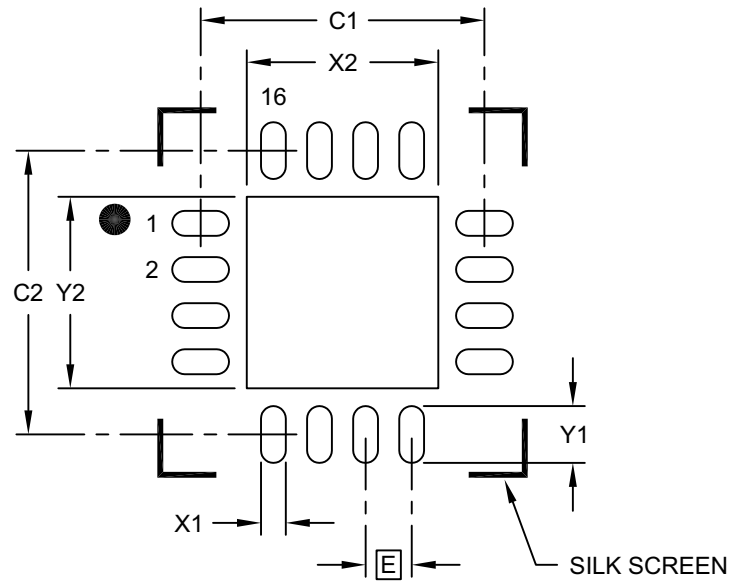
PC =	TOS
GIE =	1

**FIGURE 37-3: POR AND POR REARM WITH SLOW RISING V<sub>DD</sub>**



## 16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80

**Notes:**

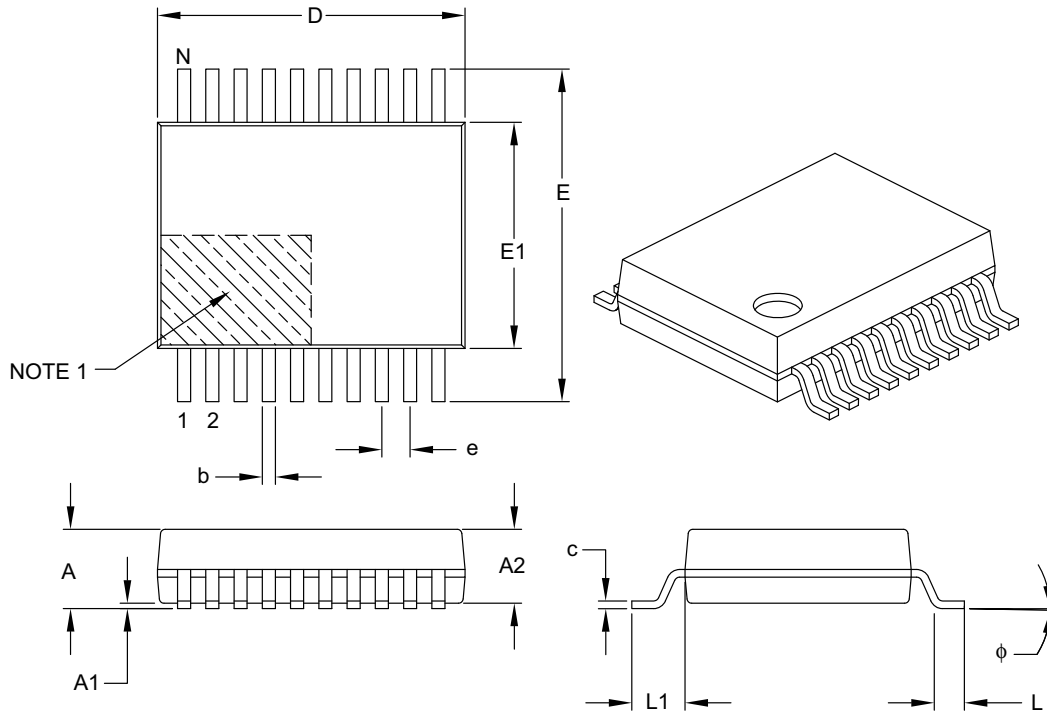
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2257A

## 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B