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### Applications of "**Embedded - Microcontrollers**"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 18MHz |
| Connectivity | I²C, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc9201fdh-112 |

## 3. Ordering information

**Table 1.     Ordering information**

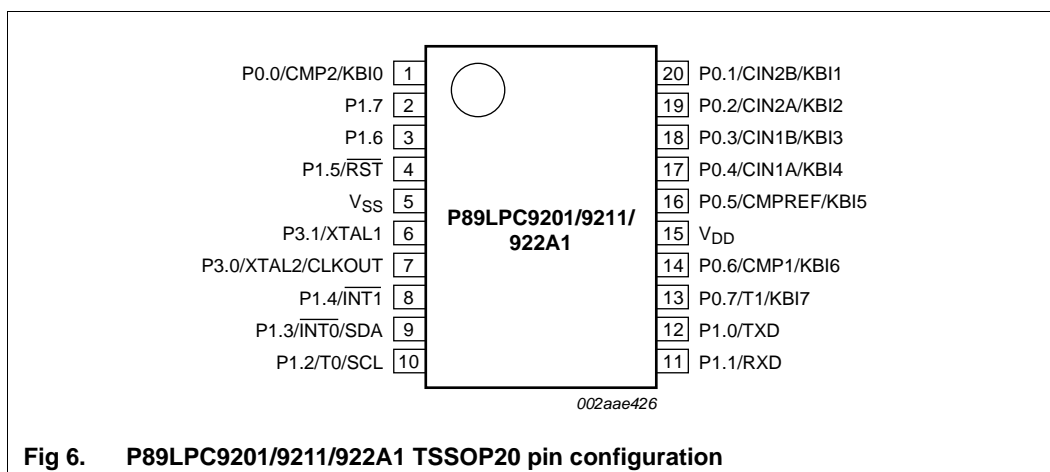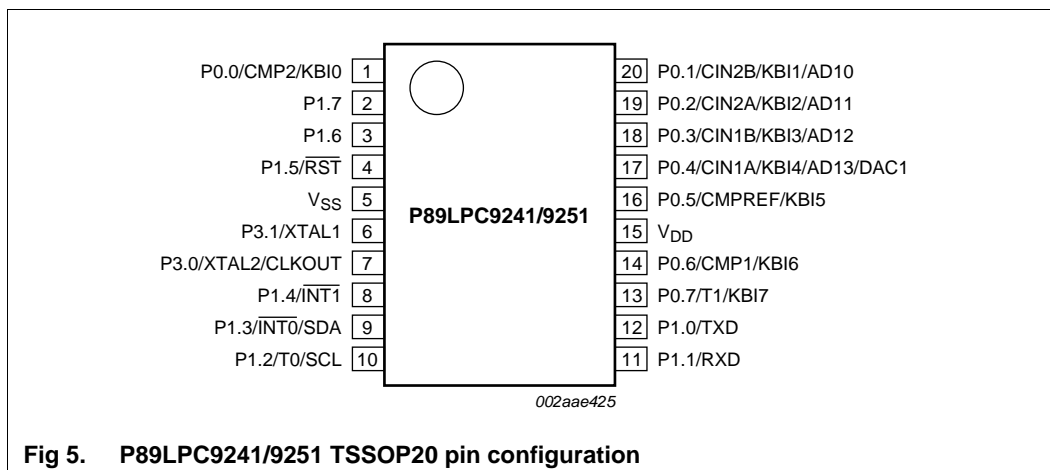| Type number | Package | | | |
|---|---|---|---|---|
| | **Name** | **Description** | | **Version** |
| P89LPC9201FDH | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | | SOT360-1 |
| P89LPC9211FDH | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | | SOT360-1 |
| P89LPC922A1FDH | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | | SOT360-1 |
| P89LPC922A1FN | DIP20 | plastic dual in-line package; 20 leads (300 mil) | | SOT146-1 |
| P89LPC9241FDH | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | | SOT360-1 |
| P89LPC9251FDH | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | | SOT360-1 |

### 3.1 Ordering options

**Table 2.     Ordering options**

| Type number | Flash memory | Temperature range | Frequency |
|---|---|---|---|
| P89LPC9201FDH | 2 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC9211FDH | 4 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC922A1FDH | 8 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC922A1FN | 8 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC9241FDH | 4 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC9251FDH | 8 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |

## 6. Pinning information

### 6.1 Pinning



**Fig 5.** **P89LPC9241/9251 TSSOP20 pin configuration**



**Fig 6.** **P89LPC9201/9211/922A1 TSSOP20 pin configuration**

### 6.2 Pin description

**Table 3.** **Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| | **TSSOP20, DIP20** | | |
| P0.0 to P0.7 | | I/O | **Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 12 "Static characteristics" for details. |
| | | | The Keypad Interrupt feature operates with Port 0 pins. |
| | | | All pins have Schmitt trigger inputs. |
| | | | Port 0 also provides various special functions as described below: |
| P0.0/CMP2/ KBI0 | 1 | I/O | **P0.0 —** Port 0 bit 0. |
| | | O | **CMP2 —** Comparator 2 output |
| | | I | **KBI0 —** Keyboard input 0. |
| P0.1/CIN2B/ KBI1/AD10 | 20 | I/O | **P0.1 —** Port 0 bit 1. |
| | | I | **CIN2B —** Comparator 2 positive input B. |
| | | I | **KBI1 —** Keyboard input 1. |
| | | I | **AD10 —** ADC1 channel 0 analog input. (P89LPC9241/9251) |
| P0.2/CIN2A/ KBI2/AD11 | 19 | I/O | **P0.2 —** Port 0 bit 2. |
| | | I | **CIN2A —** Comparator 2 positive input A. |
| | | I | **KBI2 —** Keyboard input 2. |
| | | I | **AD11 —** ADC1 channel 1 analog input. (P89LPC9241/9251) |
| P0.3/CIN1B/ KBI3/AD12 | 18 | I/O | **P0.3 —** Port 0 bit 3. High current source. |
| | | I | **CIN1B —** Comparator 1 positive input B. |
| | | I | **KBI3 —** Keyboard input 3. |
| | | I | **AD12 —** ADC1 channel 2 analog input. (P89LPC9241/9251) |
| P0.4/CIN1A/ KBI4/DAC1/AD13 | 17 | I/O | **P0.4 —** Port 0 bit 4. High current source. |
| | | I | **CIN1A —** Comparator 1 positive input A. |
| | | I | **KBI4 —** Keyboard input 4. |
| | | O | **DAC1 —** Digital-to-analog converter output 1. (P89LPC9241/9251) |
| | | I | **AD13 —** ADC1 channel 3 analog input. (P89LPC9241/9251) |
| P0.5/CMPREF/ KBI5 | 16 | I/O | **P0.5 —** Port 0 bit 5. High current source. |
| | | I | **CMPREF —** Comparator reference (negative) input. |
| | | I | **KBI5 —** Keyboard input 5. |

**Table 4.     Special function registers - P89LPC9201/9211/922A1**

*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| | | **Bit address** | **E7** | **E6** | **E5** | **E4** | **E3** | **E2** | **E1** | **E0** | | |
| ACC* | Accumulator | E0H | | | | | | | | | 00 | 0000 0000 |
| AUXR1 | Auxiliary function register | A2H | CLKLP | EBRR | ENT1 | ENT0 | SRST | 0 | - | DPS | 00 | 0000 00x0 |
| | | **Bit address** | **F7** | **F6** | **F5** | **F4** | **F3** | **F2** | **F1** | **F0** | | |
| B* | B register | F0H | | | | | | | | | 00 | 0000 0000 |
| BRGR0[2] | Baud rate generator 0 rate low | BEH | | | | | | | | | 00 | 0000 0000 |
| BRGR1[2] | Baud rate generator 0 rate high | BFH | | | | | | | | | 00 | 0000 0000 |
| BRGCON | Baud rate generator 0 control | BDH | - | - | - | - | - | - | SBRGS | BRGEN | 00[2] | xxxx xx00 |
| CMP1 | Comparator 1 control register | ACH | - | - | CE1 | CP1 | CN1 | OE1 | CO1 | CMF1 | 00[1] | xx00 0000 |
| CMP2 | Comparator 2 control register | ADH | - | - | CE2 | CP2 | CN2 | OE2 | CO2 | CMF2 | 00[1] | xx00 0000 |
| DIVM | CPU clock divide-by-M control | 95H | | | | | | | | | 00 | 0000 0000 |
| DPTR | Data pointer (2 bytes) | | | | | | | | | | | |
| DPH | Data pointer high | 83H | | | | | | | | | 00 | 0000 0000 |
| DPL | Data pointer low | 82H | | | | | | | | | 00 | 0000 0000 |
| FMADRH | Program flash address high | E7H | | | | | | | | | 00 | 0000 0000 |
| FMADRL | Program flash address low | E6H | | | | | | | | | 00 | 0000 0000 |

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**Table 4.    Special function registers - P89LPC9201/9211/922A1**
*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| **Bit address** | | | **8F** | **8E** | **8D** | **8C** | **8B** | **8A** | **89** | **88** | | |
| TCON* | Timer 0 and 1 control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00 | 0000 0000 |
| TH0 | Timer 0 high | 8CH | | | | | | | | | 00 | 0000 0000 |
| TH1 | Timer 1 high | 8DH | | | | | | | | | 00 | 0000 0000 |
| TL0 | Timer 0 low | 8AH | | | | | | | | | 00 | 0000 0000 |
| TL1 | Timer 1 low | 8BH | | | | | | | | | 00 | 0000 0000 |
| TMOD | Timer 0 and 1 mode | 89H | T1GATE | T1C/T | T1M1 | T1M0 | T0GATE | T0C/T | T0M1 | T0M0 | 00 | 0000 0000 |
| TRIM | Internal oscillator trim register | 96H | RCCLK | ENCLK | TRIM.5 | TRIM.4 | TRIM.3 | TRIM.2 | TRIM.1 | TRIM.0 | [5][6] | |
| WDCON | Watchdog control register | A7H | PRE2 | PRE1 | PRE0 | - | - | WDRUN | WDTOF | WDCLK | [4][6] | |
| WDL | Watchdog load | C1H | | | | | | | | | FF | 1111 1111 |
| WFEED1 | Watchdog feed 1 | C2H | | | | | | | | | | |
| WFEED2 | Watchdog feed 2 | C3H | | | | | | | | | | |

[1]   All ports are in input only (high-impedance) state after power-up.

[2]   BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3]   The RSTSRC register reflects the cause of the P89LPC9201/9211/922A1 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4]   After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5]   On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6]   The only reset sources that affect these SFRs are power-on reset and watchdog reset.

**Table 6.    Special function registers - P89LPC9241/9251**
*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| | | **Bit address** | **E7** | **E6** | **E5** | **E4** | **E3** | **E2** | **E1** | **E0** | | |
| ACC* | Accumulator | E0H | | | | | | | | | 00 | 0000 0000 |
| ADCON0 | A/D control register 0 | 8EH | ENBI0 | ENADCI0 | TMM0 | EDGE0 | ADCI0 | ENADC0 | ADCS01 | ADCS00 | 00 | 0000 0000 |
| ADCON1 | A/D control register 1 | 97H | ENBI1 | ENADCI1 | TMM1 | EDGE1 | ADCI1 | ENADC1 | ADCS11 | ADCS10 | 00 | 0000 0000 |
| ADINS | A/D input select | A3H | AIN13 | AIN12 | AIN11 | AIN10 | AIN03 | AIN02 | AIN01 | AIN00 | 00 | 0000 0000 |
| ADMODA | A/D mode register A | C0H | BNDI1 | BURST1 | SCC1 | SCAN1 | BNDI0 | BURST0 | SCC0 | SCAN0 | 00 | 0000 0000 |
| ADMODB | A/D mode register B | A1H | CLK2 | CLK1 | CLK0 | INBND0 | ENDAC1 | ENDAC0 | BSA1 | BSA0 | 00 | 000x 0000 |
| AD0BH | A/D_0 boundary high register | BBH | | | | | | | | | FF | 1111 1111 |
| AD0BL | A/D_0 boundary low register | A6H | | | | | | | | | 00 | 0000 0000 |
| AD0DAT0 | A/D_0 data register 0 | C5H | | | | | | | | | 00 | 0000 0000 |
| AD0DAT1 | A/D_0 data register 1 | C6H | | | | | | | | | 00 | 0000 0000 |
| AD0DAT2 | A/D_0 data register 2 | C7H | | | | | | | | | 00 | 0000 0000 |
| AD0DAT3 | A/D_0 data register 3 | F4H | | | | | | | | | 00 | 0000 0000 |
| AD1BH | A/D_0 boundary high register | C4H | | | | | | | | | FF | 1111 1111 |
| AD1BL | A/D_0 boundary low register | BCH | | | | | | | | | 00 | 0000 0000 |
| AD1DAT0 | A/D_0 data register 0 | D5H | | | | | | | | | 00 | 0000 0000 |

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**Table 6.     Special function registers - P89LPC9241/9251** *…continued*
*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| AD1DAT1 | A/D_0 data register 1 | D6H | | | | | | | | | 00 | 0000 0000 |
| AD1DAT2 | A/D_0 data register 2 | D7H | | | | | | | | | 00 | 0000 0000 |
| AD1DAT3 | A/D_0 data register 3 | F5H | | | | | | | | | 00 | 0000 0000 |
| AUXR1 | Auxiliary function register | A2H | CLKLP | EBRR | ENT1 | ENT0 | SRST | 0 | - | DPS | 00 | 0000 00x0 |
| | **Bit address** | | **F7** | **F6** | **F5** | **F4** | **F3** | **F2** | **F1** | **F0** | | |
| B* | B register | F0H | | | | | | | | | 00 | 0000 0000 |
| BRGR0[2] | Baud rate generator 0 rate low | BEH | | | | | | | | | 00 | 0000 0000 |
| BRGR1[2] | Baud rate generator 0 rate high | BFH | | | | | | | | | 00 | 0000 0000 |
| BRGCON | Baud rate generator 0 control | BDH | - | - | - | - | - | - | SBRGS | BRGEN | 00[2] | xxxx xx00 |
| CMP1 | Comparator 1 control register | ACH | - | - | CE1 | CP1 | CN1 | OE1 | CO1 | CMF1 | 00[1] | xx00 0000 |
| CMP2 | Comparator 2 control register | ADH | - | - | CE2 | CP2 | CN2 | OE2 | CO2 | CMF2 | 00[1] | xx00 0000 |
| DIVM | CPU clock divide-by-M control | 95H | | | | | | | | | 00 | 0000 0000 |
| DPTR | Data pointer (2 bytes) | | | | | | | | | | | |
| DPH | Data pointer high | 83H | | | | | | | | | 00 | 0000 0000 |
| DPL | Data pointer low | 82H | | | | | | | | | 00 | 0000 0000 |

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**Table 6.     Special function registers - P89LPC9241/9251** *…continued*
*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | | MSB | | | | | | | LSB | Hex | Binary |
| SP | Stack pointer | 81H | | | | | | | | | 07 | 0000 0111 |
| TAMOD | Timer 0 and 1 auxiliary mode | 8FH | - | - | - | T1M2 | - | - | - | T0M2 | 00 | xxx0 xxx0 |
| **Bit address** | | | **8F** | **8E** | **8D** | **8C** | **8B** | **8A** | **89** | **88** | | |
| TCON* | Timer 0 and 1 control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00 | 0000 0000 |
| TH0 | Timer 0 high | 8CH | | | | | | | | | 00 | 0000 0000 |
| TH1 | Timer 1 high | 8DH | | | | | | | | | 00 | 0000 0000 |
| TL0 | Timer 0 low | 8AH | | | | | | | | | 00 | 0000 0000 |
| TL1 | Timer 1 low | 8BH | | | | | | | | | 00 | 0000 0000 |
| TMOD | Timer 0 and 1 mode | 89H | T1GATE | T1C/T | T1M1 | T1M0 | T0GATE | T0C/T | T0M1 | T0M0 | 00 | 0000 0000 |
| TRIM | Internal oscillator trim register | 96H | RCCLK | ENCLK | TRIM.5 | TRIM.4 | TRIM.3 | TRIM.2 | TRIM.1 | TRIM.0 | [5][6] | |
| WDCON | Watchdog control register | A7H | PRE2 | PRE1 | PRE0 | - | - | WDRUN | WDTOF | WDCLK | [4][6] | |
| WDL | Watchdog load | C1H | | | | | | | | | FF | 1111 1111 |
| WFEED1 | Watchdog feed 1 | C2H | | | | | | | | | | |
| WFEED2 | Watchdog feed 2 | C3H | | | | | | | | | | |

[1]   All ports are in input only (high-impedance) state after power-up.

[2]   BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3]   The RSTSRC register reflects the cause of the P89LPC9241/9251 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4]   After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5]   On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6]   The only reset sources that affect these SFRs are power-on reset and watchdog reset.
      CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7

## 7.13 Memory organization

The various P89LPC9201/9211/922A1/9241/9251 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9201/9211/922A1/9241/9251 has 2 kB/4 kB/8 kB of on-chip Code memory.

## 7.14 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in Table 8.

**Table 8.**      **On-chip data memory usages**

| Type | Data RAM | Size (bytes) |
|------|----------|--------------|
| DATA | Memory that can be addressed directly and indirectly | 128 |
| IDATA | Memory that can be addressed indirectly | 256 |

## 7.15 Interrupts

The P89LPC9201/9211/922A1/9241/9251 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9201/9211/922A1/9241/9251 supports 12/13 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, $I^2C$-bus, keyboard, comparators 1 and 2, A/D Converter (P89LPC9241/9251).

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

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An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

### 7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

### 7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC9201/9211/922A1/9241/9251 device has high current source on eight pins in push-pull mode. See Table 11 "Limiting values".

## 7.16.2 Port 0 analog functions

The P89LPC9201/9211/922A1/9241/9251 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

## 7.16.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC9201/9211/922A1/9241/9251 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 12 "Static characteristics" for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

## 7.17 Power monitoring functions

The P89LPC9201/9211/922A1/9241/9251 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

### 7.20.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

## 7.21 RTC/system timer

The P89LPC9201/9211/922A1/9241/9251 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

## 7.22 UART

The P89LPC9201/9211/922A1/9241/9251 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9201/9211/922A1/9241/9251 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

### 7.22.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

### 7.22.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.22.5 "Baud rate generator and selection").

### 7.22.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

**Fig 14. Watchdog timer in Watchdog mode (WDTE = 1)**

## 7.27 Additional features

### 7.27.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

### 7.27.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

## 7.28 Flash program memory

### 7.28.1 General description

The P89LPC9201/9211/922A1/9241/9251 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9201/9211/922A1/9241/9251 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and

### 7.28.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC9201/9211/922A1/9241/9251 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application - using commercially available programmers - possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC9201/9211/922A1/9241/9251 User manual*.

### 7.28.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC9201/9211/922A1/9241/9251 User manual*.

### 7.28.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC9201/9211/922A1/9241/9251 through the serial port. This firmware is provided by NXP and embedded within each P89LPC9201/9211/922A1/9241/9251 device. The NXP ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins ($V_{DD}$, $V_{SS}$, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

### 7.28.9 Power-on reset code execution

The P89LPC9201/9211/922A1/9241/9251 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9201/9211/922A1/9241/9251 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

### 8.5.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

### 8.5.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

### 8.5.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

### 8.5.6 Single step mode

This special mode allows 'single-stepping' in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

## 8.6 Conversion start modes

### 8.6.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

### 8.6.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

### 8.6.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.
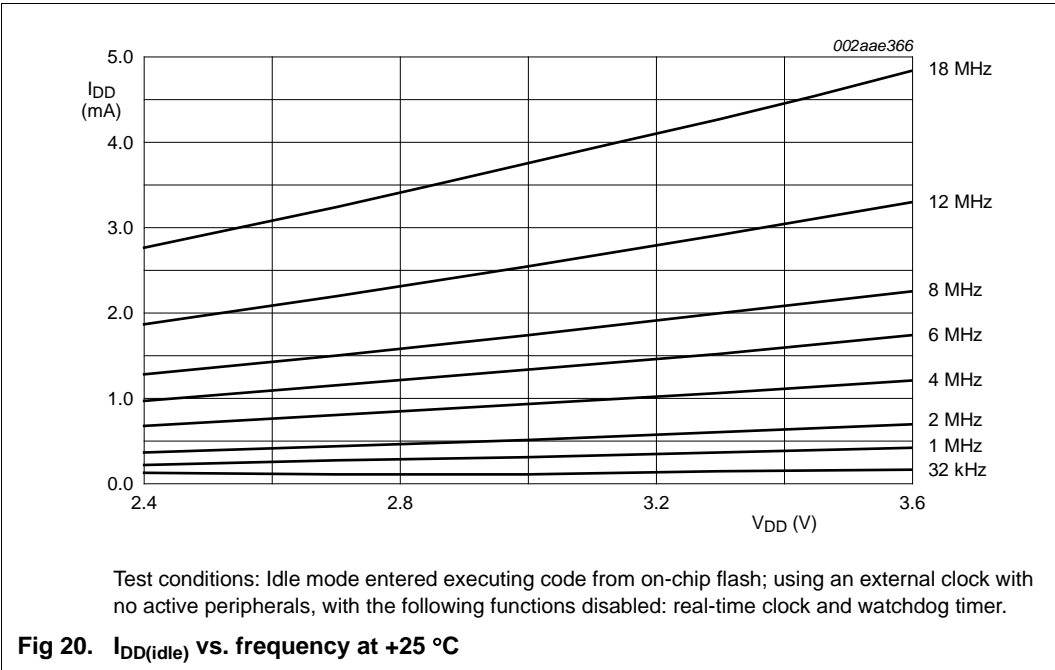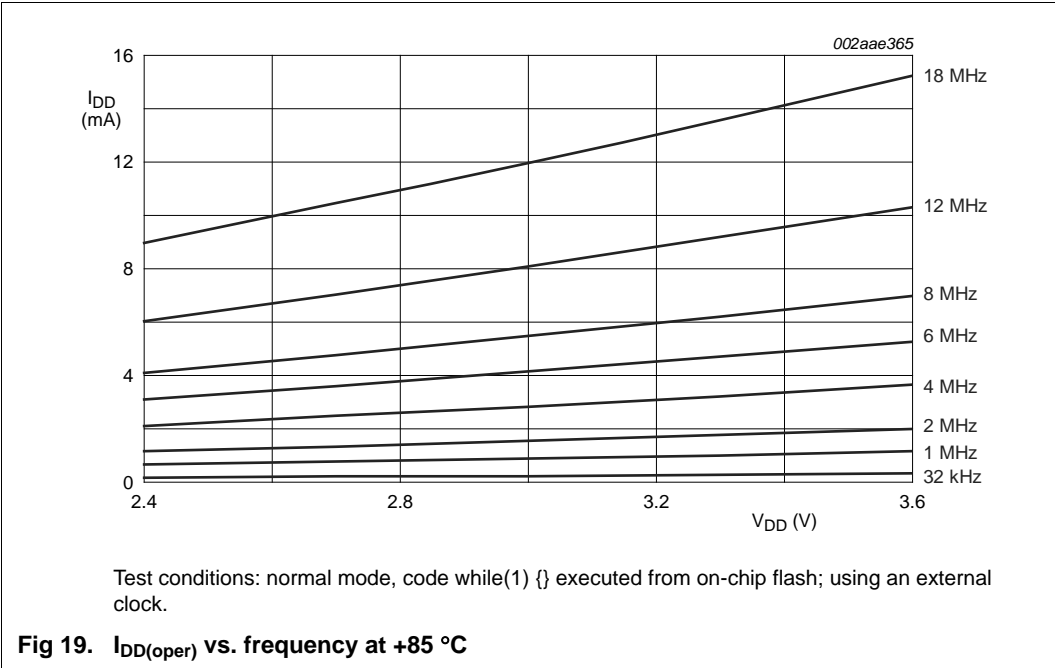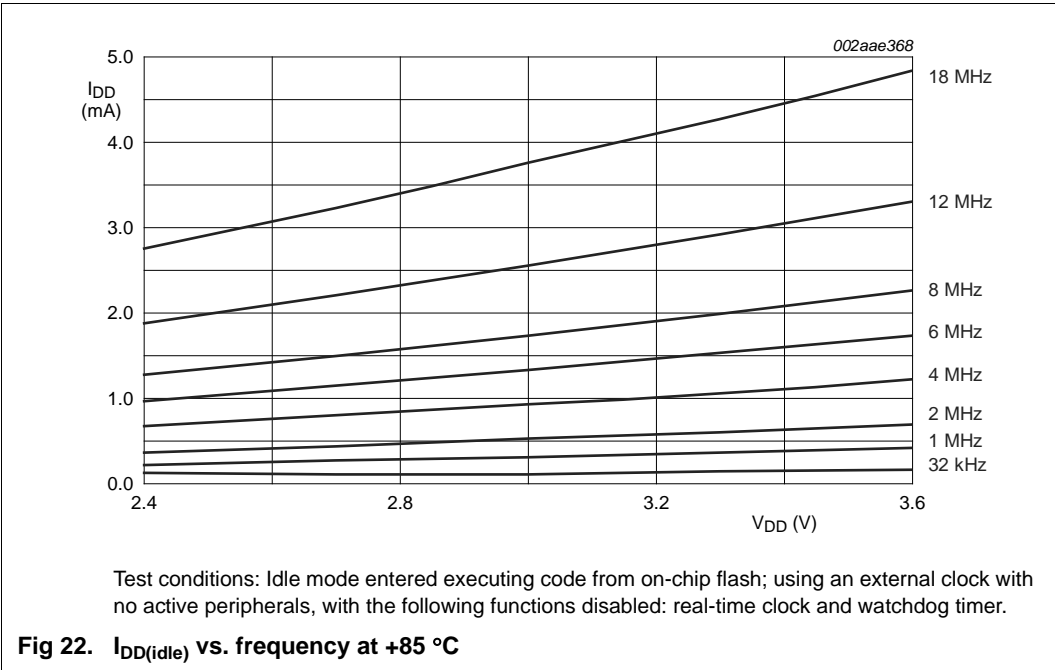
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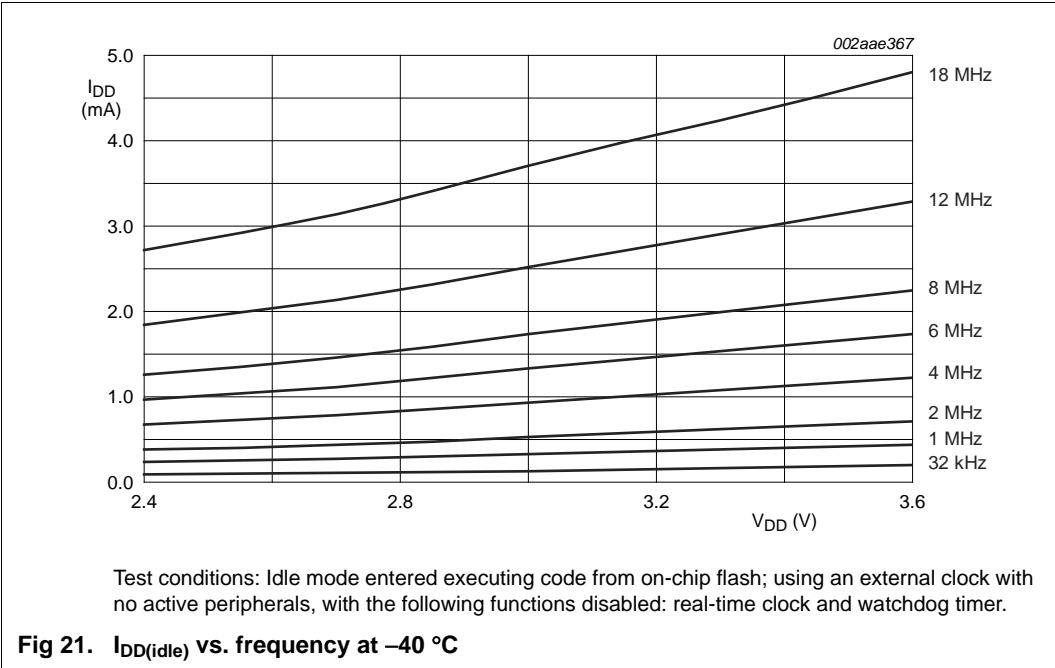**Product data sheet**  **Rev. 2.1 — 27 August 2012**  **49 of 75**

## 10. Static characteristics

**Table 12. Static characteristics**
*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(oper)}$ | operating supply current | $V_{DD}$ = 3.6 V; $f_{osc}$ = 12 MHz | [2] | - | 10 | 15 | mA |
| | | $V_{DD}$ = 3.6 V; $f_{osc}$ = 18 MHz | [2] | - | 14 | 23 | mA |
| $I_{DD(idle)}$ | Idle mode supply current | $V_{DD}$ = 3.6 V; $f_{osc}$ = 12 MHz | [3] | - | 3.25 | 5 | mA |
| | | $V_{DD}$ = 3.6 V; $f_{osc}$ = 18 MHz | [3] | - | 5 | 7 | mA |
| $I_{DD(pd)}$ | Power-down mode supply current | $V_{DD}$ = 3.6 V; voltage comparators powered down | [4] | - | 20 | 40 | μA |
| $I_{DD(tpd)}$ | total Power-down mode supply current | $V_{DD}$ = 3.6 V | [5] | - | 1 | 5 | μA |
| $(dV/dt)_r$ | rise rate | of $V_{DD}$; to ensure POR signal | | 5 | - | 5000 | V/S |
| $V_{POR}$ | power-on reset voltage | | | - | - | 0.5 | V |
| $V_{DDR}$ | data retention supply voltage | | | 1.5 | - | - | V |
| $V_{th(HL)}$ | HIGH-LOW threshold voltage | except SCL, SDA | | $0.22V_{DD}$ | $0.4V_{DD}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | SCL, SDA only | | −0.5 | - | $0.3V_{DD}$ | V |
| $V_{th(LH)}$ | LOW-HIGH threshold voltage | except SCL, SDA | | - | $0.6V_{DD}$ | $0.7V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | SCL, SDA only | | $0.7V_{DD}$ | - | 5.5 | V |
| $V_{hys}$ | hysteresis voltage | port 1 | | - | $0.2V_{DD}$ | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 20 mA; $V_{DD}$ = 2.4 V to 3.6 V all ports, all modes except high-Z | [6] | - | 0.6 | 1.0 | V |
| | | $I_{OL}$ = 3.2 mA; $V_{DD}$ = 2.4 V to 3.6 V all ports, all modes except high-Z | [6] | - | 0.2 | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −20 μA; $V_{DD}$ = 2.4 V to 3.6 V; all ports, quasi-bidirectional mode | | $V_{DD}$ − 0.3 | $V_{DD}$ − 0.2 | - | V |
| | | $I_{OH}$ = −3.2 mA; $V_{DD}$ = 2.4 V to 3.6 V; all ports, push-pull mode | | $V_{DD}$ − 0.7 | $V_{DD}$ − 0.4 | - | V |
| | | $I_{OH}$ = −10 mA; $V_{DD}$ = 2.4 V to 3.6 V; all ports, push-pull mode | | - | 3.2 | - | V |
| $V_{xtal}$ | crystal voltage | on XTAL1, XTAL2 pins; with respect to $V_{SS}$ | | −0.5 | - | +4.0 | V |
| $V_n$ | voltage on any other pin | except XTAL1, XTAL2, $V_{DD}$; with respect to $V_{SS}$ | [7] | −0.5 | - | +5.5 | V |
| $C_{iss}$ | input capacitance | | [8] | - | - | 15 | pF |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.4 V | [9] | - | - | −80 | μA |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{IL}$, $V_{IH}$, or $V_{th(HL)}$ | [10] | - | - | ±1 | μA |

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Test conditions: normal mode, code while(1) {} executed from on-chip flash; using an external clock.

**Fig 19.** $I_{DD(oper)}$ **vs. frequency at +85 °C**



Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

**Fig 20.** $I_{DD(idle)}$ **vs. frequency at +25 °C**

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Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

**Fig 21.** $I_{DD(idle)}$ **vs. frequency at –40 °C**



Test conditions: Idle mode entered executing code from on-chip flash; using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.

**Fig 22.** $I_{DD(idle)}$ **vs. frequency at +85 °C**

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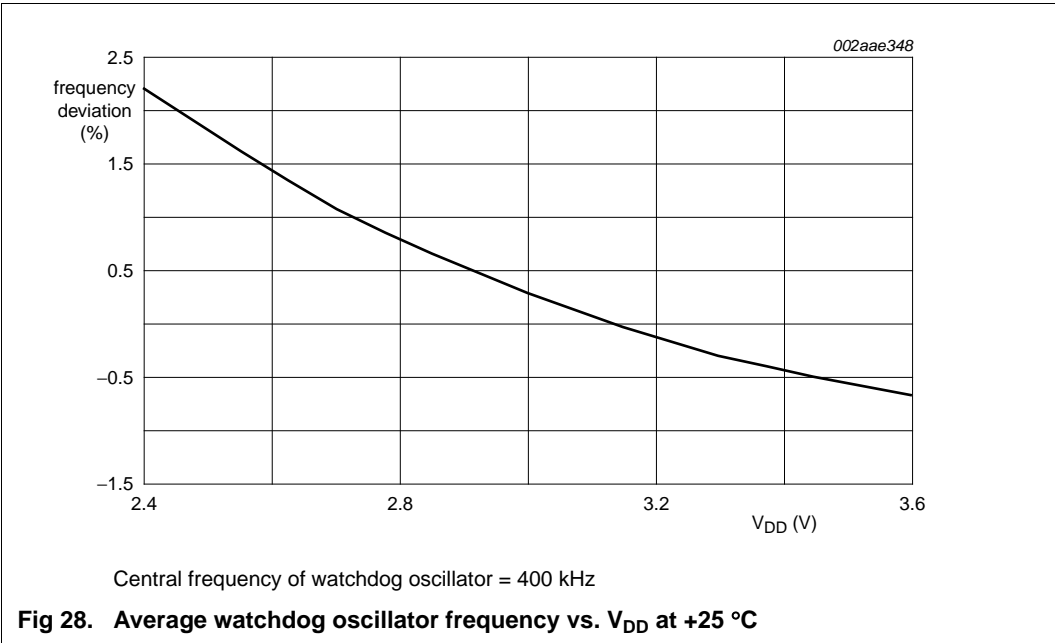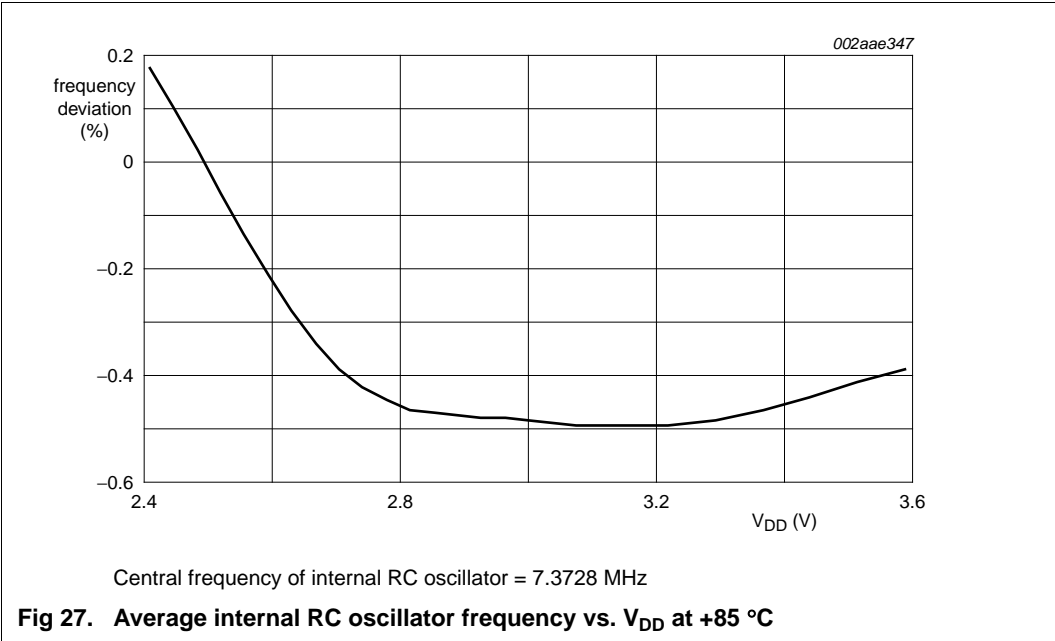**Rev. 2.1 — 27 August 2012**

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## 10.2 Internal RC/watchdog oscillator characteristics

Note: The graphs provided are a statistical summary based on a limited number of samples and only for information purposes. The performance characteristics listed are not tested or guaranteed.



Central frequency of internal RC oscillator = 7.3728 MHz

**Fig 25. Average internal RC oscillator frequency vs. $V_{DD}$ at +25 °C**



Note: Central frequency of internal RC oscillator = 7.3728 MHz

**Fig 26. Average internal RC oscillator frequency vs. $V_{DD}$ at −40 °C**

Central frequency of internal RC oscillator = 7.3728 MHz

**Fig 27. Average internal RC oscillator frequency vs. $V_{DD}$ at +85 °C**



Central frequency of watchdog oscillator = 400 kHz

**Fig 28. Average watchdog oscillator frequency vs. $V_{DD}$ at +25 °C**

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## 10.3 BOD characteristics

**Table 13.    BOD static characteristics**
*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*
*$T_{amb}$ = −40 ℃ to +85 ℃ for industrial applications, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **BOD interrupt** | | | | | | |
| $V_{trip}$ | trip voltage | falling stage | | | | |
| | | BOICFG1, BOICFG0 = 01 | 2.25 | - | 2.55 | V |
| | | BOICFG1, BOICFG0 = 10 | 2.60 | - | 2.80 | V |
| | | BOICFG1, BOICFG0 = 11 | 3.10 | - | 3.40 | V |
| | | rising stage | | | | |
| | | BOICFG1, BOICFG0 = 01 | 2.30 | - | 2.60 | V |
| | | BOICFG1, BOICFG0 = 10 | 2.70 | - | 2.90 | V |
| | | BOICFG1, BOICFG0 = 11 | 3.15 | - | 3.45 | V |
| **BOD reset** | | | | | | |
| $V_{trip}$ | trip voltage | falling stage | | | | |
| | | BOE1, BOE0 = 01 | 2.10 | - | 2.30 | V |
| | | BOE1, BOE0 = 10 | 2.25 | - | 2.55 | V |
| | | BOE1, BOE0 = 11 | 2.80 | - | 3.20 | V |
| | | rising stage | | | | |
| | | BOE1, BOE0 = 01 | 2.20 | - | 2.40 | V |
| | | BOE1, BOE0 = 10 | 2.30 | - | 2.60 | V |
| | | BOE1, BOE0 = 11 | 2.90 | - | 3.30 | V |
| **BOD EEPROM/FLASH** | | | | | | |
| $V_{trip}$ | trip voltage | falling stage | 2.25 | - | 2.55 | V |
| | | rising stage | 2.30 | - | 2.60 | V |

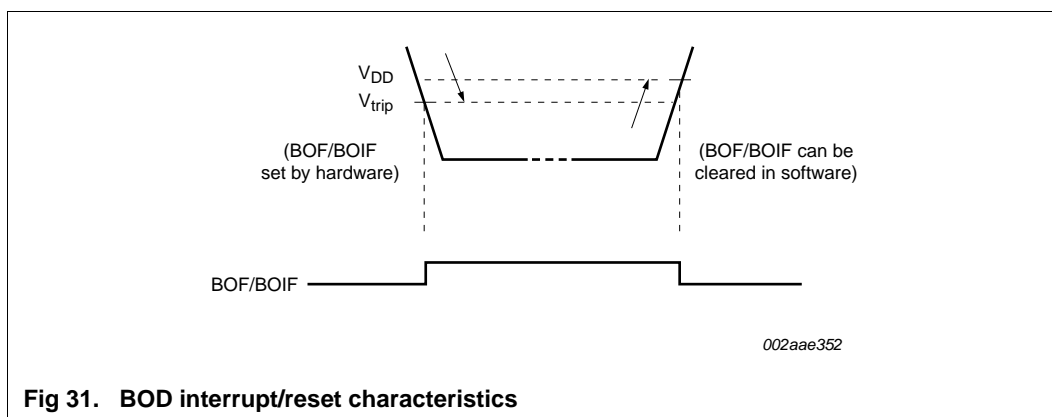[1]    Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.



**Fig 31.   BOD interrupt/reset characteristics**