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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc922a1fdh-112

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

8-bit microcontroller with 8-bit ADC



8-bit microcontroller with 8-bit ADC

6. Pinning information

6.1 Pinning



Table 4.Special function registers - P89LPC9201/9211/922A1* indicates SFRs that are bit addressable. P89LPC9

X1	Name	Description	SFR	Bit functions and addresses								Reset value	
			addr.	MSB							LSB	Hex	Binary
	IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00 <u>[1]</u>	x000 0000
-		Bit a	ddress	FF	FE	FD	FC	FB	FA	F9	F8		
	IP1*	Interrupt priority 1	F8H	-	PST	-	-	-	PC	PKBI	PI2C	00 <u>[1]</u>	00x0 0000
-	IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	-	PCH	PKBIH	PI2CH	00[1]	00x0 0000
	KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00 <u>[1]</u>	xxxx xx00
All information pr	KBMASK	Keypad interrupt mask register	86H									00	0000 0000
ovided in thi	KBPATN	Keypad pattern register	93H									FF	1111 1111
s docu		Bit a	ddress	87	86	85	84	83	82	81	80		
ment is sub	P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	<u>[1]</u>	
ect to		Bit a	ddress	97	96	95	94	93	92	91	90		
egal di	P1*	Port 1	90H	-	-	RST	INT1	INT0/SDA	T0/SCL	RXD	TXD	<u>[1]</u>	
sclaime		Bit a	ddress	B7	B6	B5	B4	B3	B2	B1	B0		
ers.	P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	<u>[1]</u>	
-	P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF <u>[1]</u>	1111 1111
-	P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00 <u>[1]</u>	0000 0000
-	P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3 <u>[1]</u>	11x1 xx11
© NXP B.V.	P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00 <u>[1]</u>	00x0 xx00
. 2012. All ri	P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03 <u>[1]</u>	xxxx xx11
ghts reserv	P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00 <u>[1]</u>	xxxx xx00

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Table 4.Special function registers - P89LPC9201/9211/922A1* indicates SFRs that are bit addressable. P89LPC9

Name	Description	SFR	Bit function	ns and addr	esses						Reset	value
		addr.	MSB							LSB	Hex	Binary
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	-	SPD	-	00 <u>[1]</u>	0000 0000
	Bit a	ddress	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	Р	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 <u>[1][6]</u>	011x xx00
RTCH	RTC register high	D2H									00 <u>[6]</u>	0000 0000
RTCL	RTC register low	D3H									00 <u>[6]</u>	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	XXXX XXXX
	Bit a	ddress	9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

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Extended special function registers - P89LPC9241/9251[1] Table 7.

N	lame	Description	SFR	Bit functions	and addre	sses						Rese	t value
•			addr.	MSB LSB						LSB	Hex	Binary	
В	ODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
С	LKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	<u>[3]</u>	
Т	PSCON	Temperature sensor control register	FFCAH	-	-	-	-	TSEL1	TSEL0	-	-	00	0000 0000
R	TCDATH	Real-time clock data register high	FFBFH									00	0000 0000
R	TCDATL	Real-time clock data register low	FFBEH									00	0000 0000

Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A, @DPTR and MOVX @DPTR, A instructions are [1] used to access these extended SFRs.

The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset. [2]

CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit [3] comes from UCFG2.7.

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7.5 Clock output

The P89LPC9201/9211/922A1/9241/9251 supports a user-selectable clock output function on the P3.0/XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC9201/9211/922A1/9241/9251. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC9201/9211/922A1/9241/9251 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz \pm 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz, calibrated to \pm 5 % at room temperature. This oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2/CLKOUT pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock sources switch on the fly

P89LPC9201/9211/922A1/9241/9251 can implement clock source switch in any sources of watchdog oscillator, 7 MHz/14 MHz internal RC oscillator, external clock source (external crystal or external clock input) during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is '0', writing to CLKCON register is not allowed.

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An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC9201/9211/922A1/9241/9251 device has high current source on eight pins in push-pull mode. See <u>Table 11 "Limiting values"</u>.

7.16.2 Port 0 analog functions

The P89LPC9201/9211/922A1/9241/9251 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.16.3 Additional port features

After power-up, all pins are in Input-Only mode. Please note that this is different from the LPC76x series of devices.

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC9201/9211/922A1/9241/9251 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to <u>Table 12 "Static characteristics"</u> for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.17 Power monitoring functions

The P89LPC9201/9211/922A1/9241/9251 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD FLASH.

BOD reset is always on except in total Power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD FLASH is always on, except in Power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD FLASH is used for flash programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to *P89LPC9201/9211/922A1/9251 User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage and is negated when V_{DD} rises above the brownout trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see <u>Table 12 "Static characteristics"</u> for specifications.

7.17.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.18 Power reduction modes

The P89LPC9201/9211/922A1/9241/9251 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.18.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.18.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9201/9211/922A1/9241/9251 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR} , therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

7.19.1 Reset vector

Following reset, the P89LPC9201/9211/922A1/9241/9251 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC9201/9211/922A1/9241/9251 User manual*). Otherwise, instructions will be fetched from address 0000H.

7.20 Timers/counters 0 and 1

The P89LPC9201/9211/922A1/9241/9251 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.20.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.20.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.20.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.20.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.20.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.22.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in Section 7.22.5 "Baud rate generator and selection").

7.22.5 Baud rate generator and selection

The P89LPC9201/9211/922A1/9241/9251 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see <u>Figure 10</u>). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generators use OSCCLK.



7.22.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

7.22.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.22.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.22.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.22.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.23 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 11. The

P89LPC9201/9211/922A1/9241/9251 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.



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7.24 Analog comparators

Two analog comparators are provided on the P89LPC9201/9211/922A1/9241/9251. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable inputs) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

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programming mechanisms. The P89LPC9201/9211/922A1/9241/9251 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms. When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

7.28.3 Flash organization

The program memory consists of two/four/eight 1 kB sectors on the P89LPC9201/9211/922A1/9241/9251 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 byte to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.28.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

10.2 Internal RC/watchdog oscillator characteristics

Note: The graphs provided are a statistical summary based on a limited number of samples and only for information purposes. The performance characteristics listed are not tested or guaranteed.





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12. Other characteristics

12.1 Comparator electrical characteristics

Table 17. Comparator electrical characteristics

 $V_{DD} = 2.4$ V to 3.6 V, unless otherwise specified.

 $T_{amb} = -40$ °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IO}	input offset voltage		-	-	±20	mV
V _{IC}	common-mode input voltage		0	-	$V_{DD}-0.3$	V
CMRR	common-mode rejection ratio	[;	<u>1]</u> _	-	-50	dB
t _{res(tot)}	total response time		-	250	500	ns
t _(CE-OV)	chip enable to output valid time		-	-	10	μS
ILI	input leakage current	$0 V < V_I < V_{DD}$	-	-	±1	μA

[1] This parameter is characterized, but not tested in production.

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15. Revision history

Table 20. Revision histo	ory			
Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC92X v.2.1	20120827	Product data sheet	-	P89LPC92X v.2
Modifications:	 Section 7.19: 	Added "When this pin function	ns as a reset input	"
	• <u>Table 12</u> : Add	ded V _{POR} .		
P89LPC92X v.2	20101201	Product data sheet	-	P89LPC92X v.1
Modifications:	Table 11: Upo	lated table.		
	 Table 17: Upo 	dated I _{LI} max value.		
	 Section 7.4: A 	Added low speed oscillator info	rmation.	
	 Section 7.26: 	Added low speed oscillator inf	formation.	
	 Changed data 	a sheet status to Product.		
P89LPC92X v.1	20090416	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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