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Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I ² C, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc922a1fn-112

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to $\pm 5\%$, requiring no external components. The watchdog prescaler is selectable from eight values.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Clock switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9201/9211/922A1/9241/9251 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

4. Block diagram

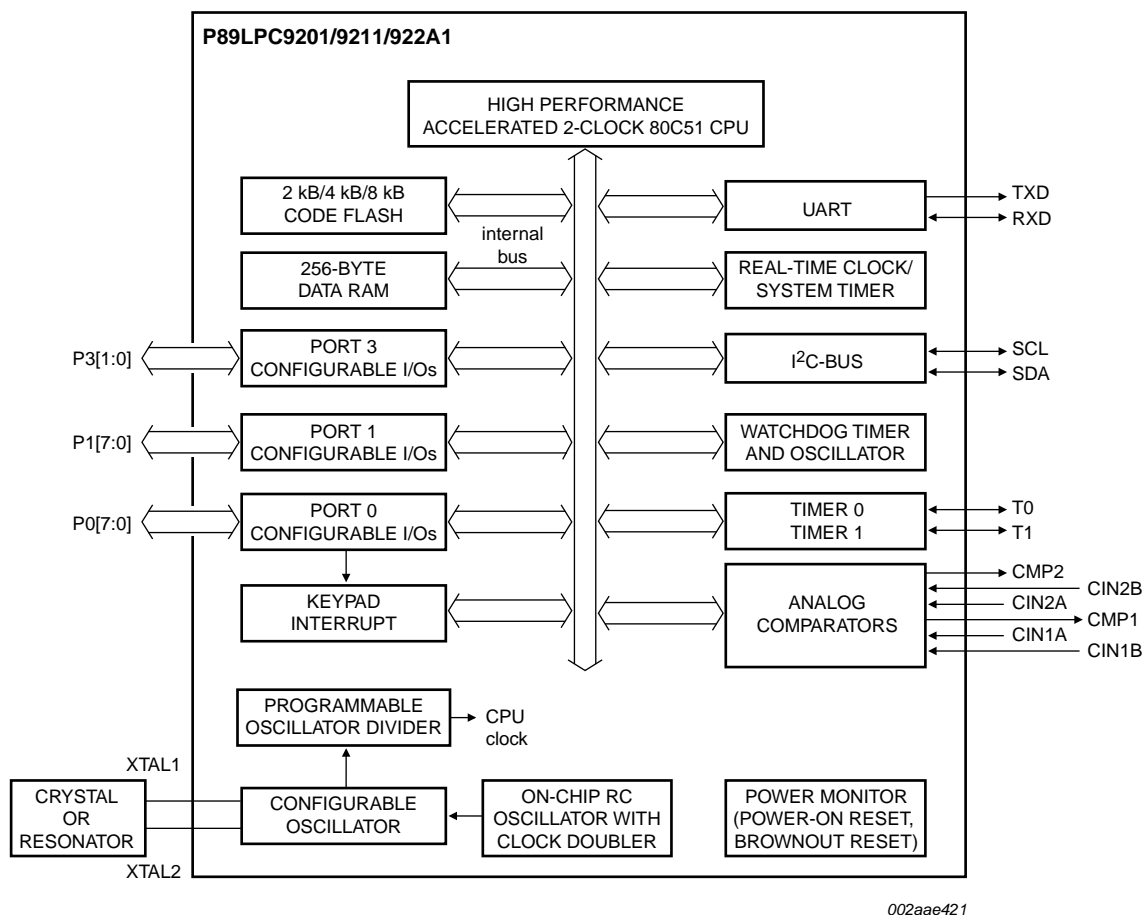


Fig 1. Block diagram (P89LPC9201/9211/922A1)

6.2 Pin description**Table 3. Pin description**

Symbol	Pin	Type	Description
	TSSOP20, DIP20		
P0.0 to P0.7		I/O	<p>Port 0: Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 12 "Static characteristics" for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 0 also provides various special functions as described below:</p>
P0.0/CMP2/ KBI0	1	I/O	P0.0 — Port 0 bit 0.
		O	CMP2 — Comparator 2 output
		I	KBI0 — Keyboard input 0.
P0.1/CIN2B/ KBI1/AD10	20	I/O	P0.1 — Port 0 bit 1.
		I	CIN2B — Comparator 2 positive input B.
		I	KBI1 — Keyboard input 1.
P0.2/CIN2A/ KBI2/AD11	19	I/O	P0.2 — Port 0 bit 2.
		I	CIN2A — Comparator 2 positive input A.
		I	KBI2 — Keyboard input 2.
P0.3/CIN1B/ KBI3/AD12	18	I/O	P0.3 — Port 0 bit 3. High current source.
		I	CIN1B — Comparator 1 positive input B.
		I	KBI3 — Keyboard input 3.
P0.4/CIN1A/ KBI4/DAC1/AD13	17	I/O	P0.4 — Port 0 bit 4. High current source.
		I	CIN1A — Comparator 1 positive input A.
		I	KBI4 — Keyboard input 4.
P0.5/CMPREF/ KBI5	16	O	DAC1 — Digital-to-analog converter output 1. (P89LPC9241/9251)
		I	AD13 — ADC1 channel 3 analog input. (P89LPC9241/9251)
		I	AD13 — ADC1 channel 3 analog input. (P89LPC9241/9251)
P0.5/CMPREF/ KBI5	16	I/O	P0.5 — Port 0 bit 5. High current source.
		I	CMPREF — Comparator reference (negative) input.
		I	KBI5 — Keyboard input 5.

Table 4. Special function registers - P89LPC9201/9211/922A1

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00 ^[1]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	-	PC	PKBI	PI2C	00 ^[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	-	PCH	PKBIH	PI2CH	00 ^[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00 ^[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		87	86	85	84	83	82	81	80		
P0*	Port 0	80H	T1/KB7	CMP1/KB6	CMPREF/KB5	CIN1A/KB4	CIN1B/KB3	CIN2A/KB2	CIN2B/KB1	CMP2/KB0	^[1]	
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	RST	INT1	INT0/SDA	T0/SCL	RXD	TXD	^[1]	
	Bit address		B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	^[1]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF ^[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00 ^[1]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3 ^[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00 ^[1]	00x0 xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03 ^[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00 ^[1]	xxxx xx00

Table 4. Special function registers - P89LPC9201/9211/922A1

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	-	SPD	-	00 ^[1]	0000 0000
Bit address			D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX	^[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60 ^[1] ^[6]	011x xx00
RTCH	RTC register high	D2H									00 ^[6]	0000 0000
RTCL	RTC register low	D3H									00 ^[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
Bit address			9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

Table 4. Special function registers - P89LPC9201/9211/922A1

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
Bit address			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

- [1] All ports are in input only (high-impedance) state after power-up.
- [2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.
- [3] The RSTSRC register reflects the cause of the P89LPC9201/9211/922A1 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.
- [4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.
- [5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
- [6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

Table 5. Extended special function registers - P89LPC9201/9211/922A1^[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	^[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	^[3]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A, @DPTR and MOVX @DPTR, A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

Table 6. Special function registers - P89LPC9241/9251 ...continued
** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB								Hex	Binary
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I ² C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I ² C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I ² C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I ² C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
	Bit address		AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	EI2C	00 ^[1]	00x0 0000

Table 6. Special function registers - P89LPC9241/9251 ...continued

* indicates SFRs that are bit addressable.

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB				LSB				Hex	Binary
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
Bit address			8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high-impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC9241/9251 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7

7.5 Clock output

The P89LPC9201/9211/922A1/9241/9251 supports a user-selectable clock output function on the P3.0/XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC9201/9211/922A1/9241/9251. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC9201/9211/922A1/9241/9251 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz \pm 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz, calibrated to \pm 5 % at room temperature. This oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2/CLKOUT pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock sources switch on the fly

P89LPC9201/9211/922A1/9241/9251 can implement clock source switch in any sources of watchdog oscillator, 7 MHz/14 MHz internal RC oscillator, external clock source (external crystal or external clock input) during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is '0', writing to CLKCON register is not allowed.

7.13 Memory organization

The various P89LPC9201/9211/922A1/9241/9251 memory spaces are as follows:

- **DATA**
128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.
- **IDATA**
Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- **SFR**
Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- **CODE**
64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9201/9211/922A1/9241/9251 has 2 kB/4 kB/8 kB of on-chip Code memory.

7.14 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in [Table 8](#).

Table 8. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256

7.15 Interrupts

The P89LPC9201/9211/922A1/9241/9251 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9201/9211/922A1/9241/9251 supports 12/13 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I²C-bus, keyboard, comparators 1 and 2, A/D Converter (P89LPC9241/9251).

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.15.1 External interrupt inputs

The P89LPC9201/9211/922A1/9241/9251 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9201/9211/922A1/9241/9251 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to [Section 7.18 “Power reduction modes”](#) for details.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD FLASH.

BOD reset is always on except in total Power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD FLASH is always on, except in Power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD FLASH is used for flash programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to *P89LPC9201/9211/922A1/9241/9251 User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage and is negated when V_{DD} rises above the brownout trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see [Table 12 "Static characteristics"](#) for specifications.

7.17.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.18 Power reduction modes

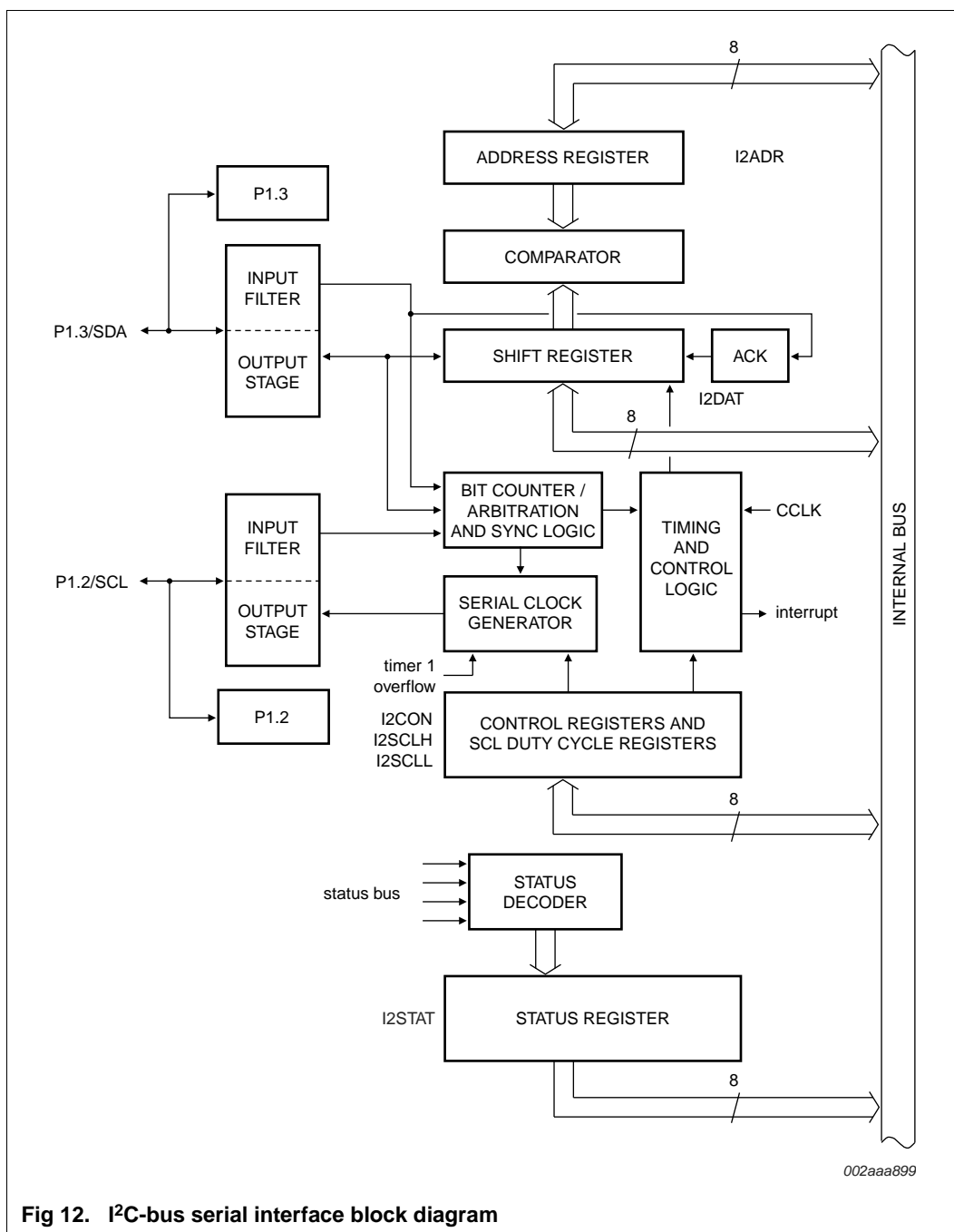
The P89LPC9201/9211/922A1/9241/9251 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.18.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.18.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9201/9211/922A1/9241/9251 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR} , therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.



7.24 Analog comparators

Two analog comparators are provided on the P89LPC9201/9211/922A1/9241/9251. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable inputs) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in [Figure 13](#). The comparators function to $V_{DD} = 2.4$ V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μ s. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, CO_n , goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMF_n . This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMF_n , after disabling the comparator.

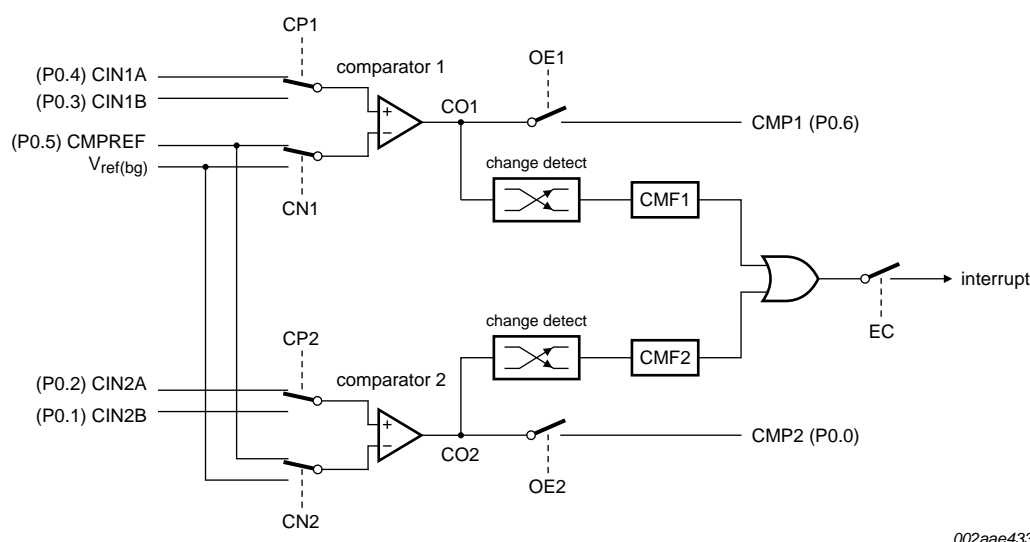


Fig 13. Comparator input and output connections

7.24.1 Internal reference voltage

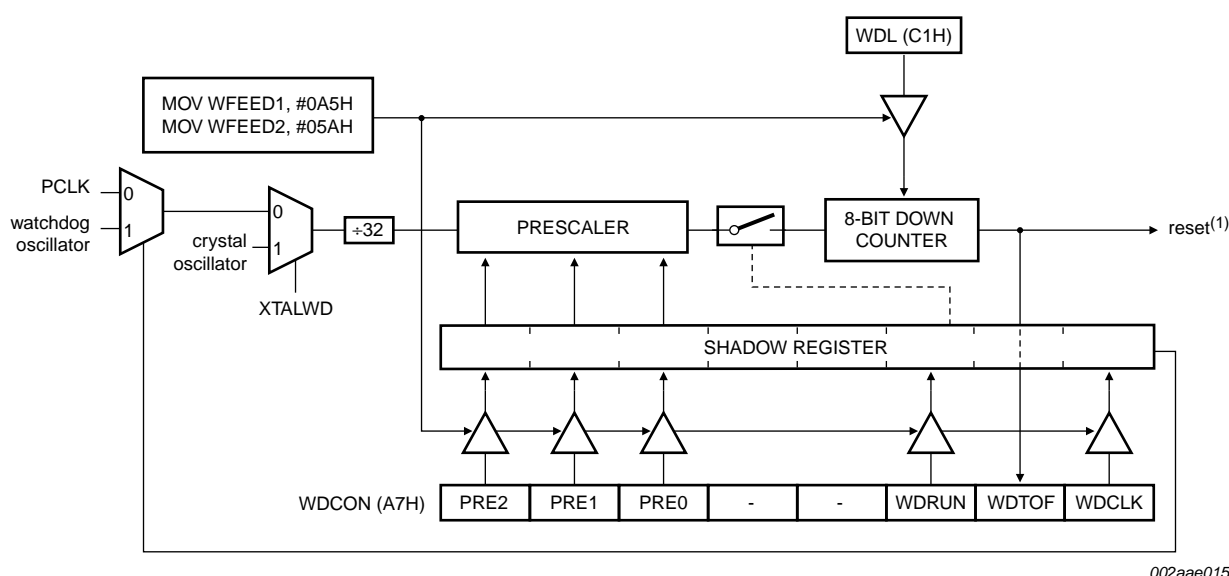
An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is $1.23\text{ V} \pm 10\%$.

7.24.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.24.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 14. Watchdog timer in Watchdog mode (WDTE = 1)

7.27 Additional features

7.27.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.27.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.28 Flash program memory

7.28.1 General description

The P89LPC9201/9211/922A1/9241/9251 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9201/9211/922A1/9241/9251 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and

8.7 Boundary limits interrupt

Each of the A/D converters has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt criteria, the boundary limits will again be compared after all 8 bits have been converted. The boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.8 DAC output to a port pin with high output impedance

The DAC block of ADC1 can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to AD1DAT3), the DAC output will appear on the channel 3 pin.

8.9 Clock divider

The ADC requires that its internal clock source be in the range of 320 kHz to 8 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.10 Power-down and Idle mode

In Idle mode the ADC, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the A/D and temperature sensor do not function. If temperature sensor or the A/D are enabled, they will consume power. Power can be reduced by disabling temperature sensor and A/D.

Table 12. Static characteristics ...continued $V_{DD} = 2.4\text{ V}$ to 3.6 V unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_{THL}	HIGH-LOW transition current	all ports; $V_I = 1.5\text{ V}$ at $V_{DD} = 3.6\text{ V}$	^[11] -30	-	-450	μA
$R_{RST_N(int)}$	internal pull-up resistance on pin \overline{RST}	pin \overline{RST}	10	-	30	$\text{k}\Omega$
$V_{ref(bg)}$	band gap reference voltage		1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient		-	10	20	$\text{ppm}/^{\circ}\text{C}$

- [1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.
- [2] The $I_{DD(oper)}$ specification is measured using an external clock with code while(1) {} executed from on-chip flash.
- [3] The $I_{DD(idle)}$ specification is measured using an external clock with no active peripherals, with the following functions disabled: real-time clock and watchdog timer.
- [4] The $I_{DD(pd)}$ specification is measured using internal RC oscillator with the following functions disabled: comparators, real-time clock, and watchdog timer.
- [5] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.
- [6] See Section 9 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH} . If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.
- [7] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS} .
- [8] Pin capacitance is characterized but not tested.
- [9] Measured with port in quasi-bidirectional mode.
- [10] Measured with port in high-impedance mode.
- [11] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

10.1 Current characteristics

Note: The graphs provided are a statistical summary based on a limited number of samples and only for information purposes. The performance characteristics listed are not tested or guaranteed.

