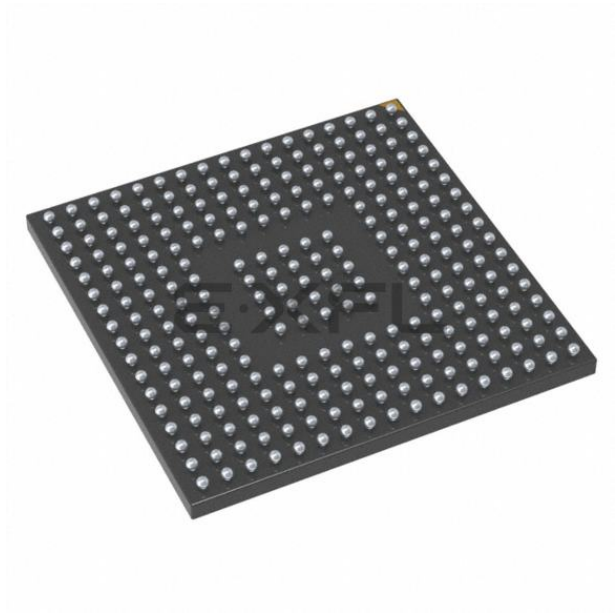


Welcome to E-XFL.COM

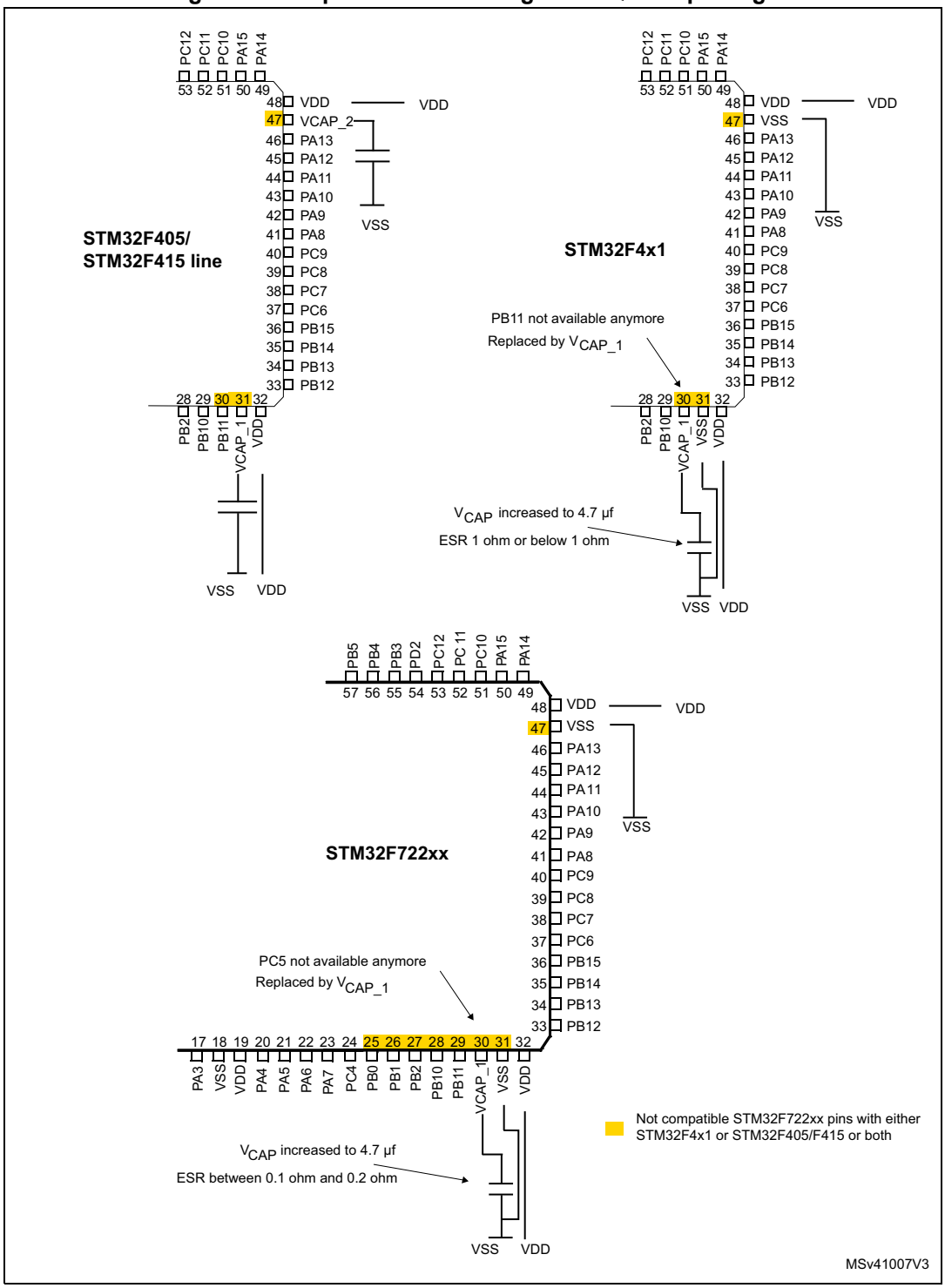
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f722ick6

Figure 2. Compatible board design for LQFP64 package



The STM32F722xx LQFP144, UFBGA176 and LQFP176 packages are fully pin to pin compatible with the STM32F4xx devices.

1.2 STM32F723xx versus STM32F722xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

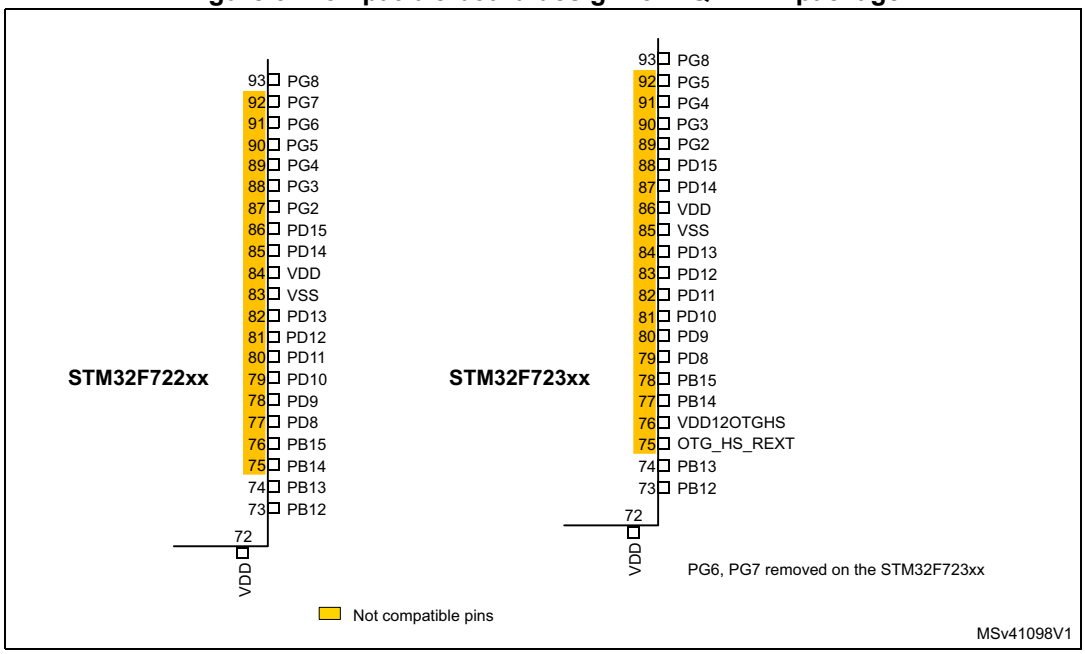
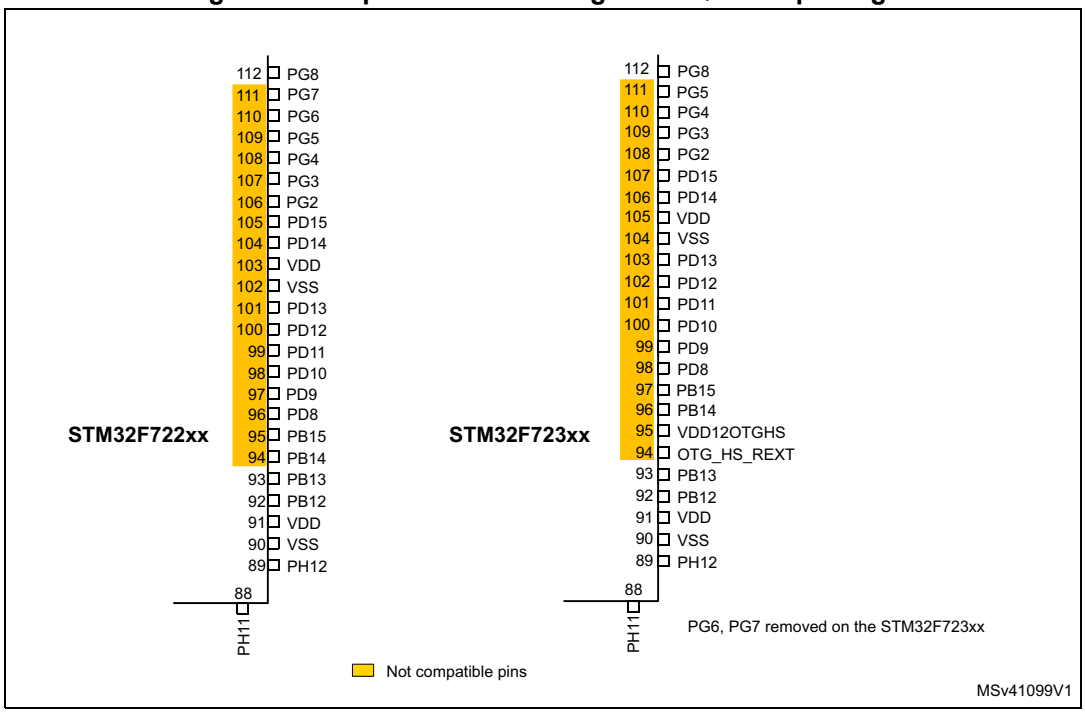


Figure 4. Compatible board design for LQFP176 package



2.19 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

The V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When the PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and the V_{BAT} pin should be connected to V_{DD}.

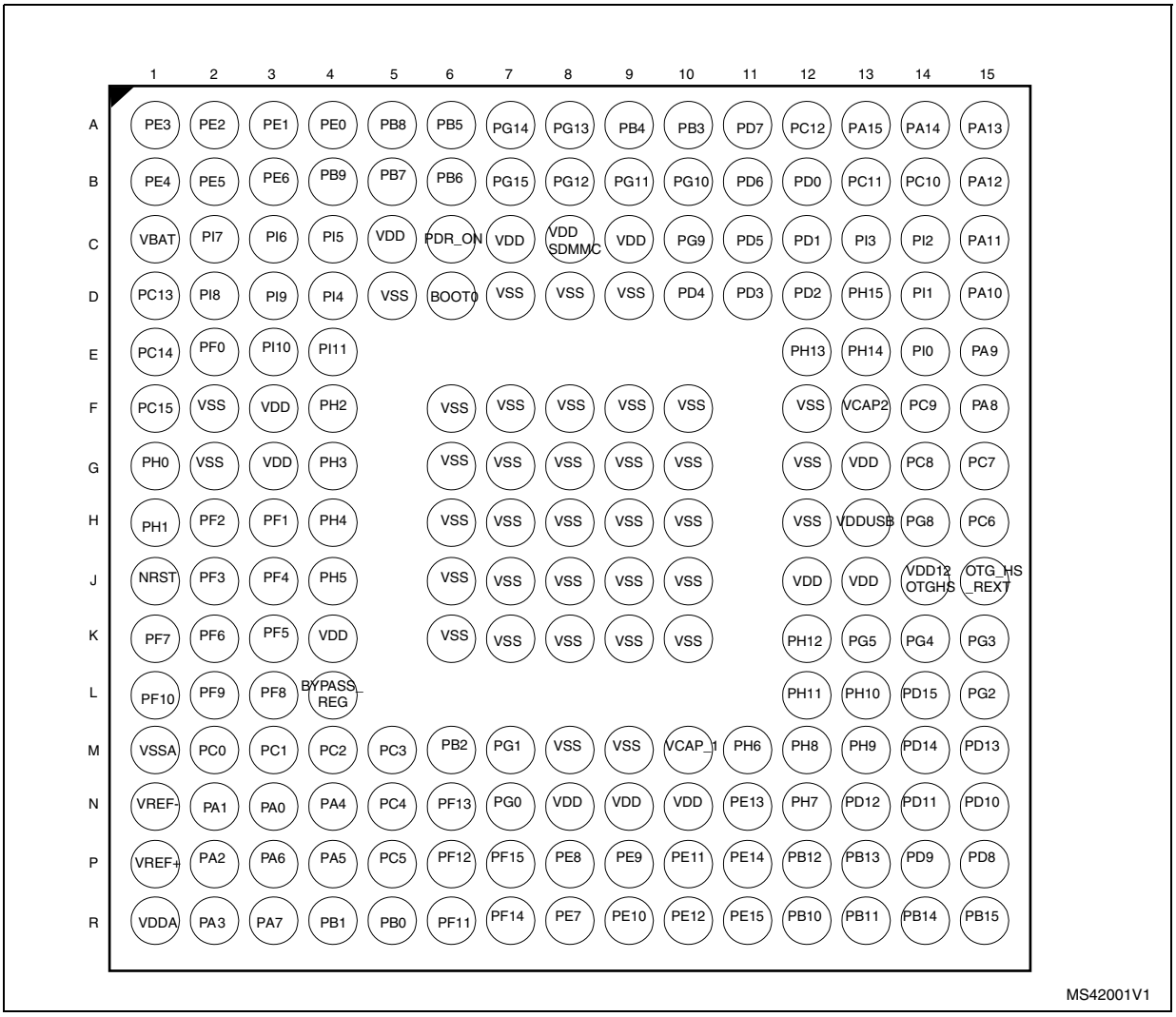
2.20 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 6 compares the features of the advanced-control, general-purpose and basic timers.

Figure 23. STM32F723xx UFBGA176 ballout (with OTG PHY HS)



1. The above figure shows the package top view.

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	20	L3	26	-	L3	G3	20	26	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	21	L2	27	-	L2	G2	21	27	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	-	22	L1	28	-	L1	G1	22	28	PF10	I/O	FT	-	EVENTOUT	ADC3_IN8
5	12	23	G1	29	G10	G1	D1	23	29	PH0-OSC_IN	I/O	FT	-	EVENTOUT	OSC_IN[5]
6	13	24	H1	30	H10	H1	E1	24	30	PH1-OSC_OUT	I/O	FT	-	EVENTOUT	OSC_OUT[5]
7	14	25	J1	31	G9	J1	F1	25	31	NRST	I/O	RST	-	-	-
8	15	26	M2	32	F8	M2	H1	26	32	PC0	I/O	FT	(4) (5)	SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
9	16	27	M3	33	H9	M3	H2	27	33	PC1	I/O	FT	(5)	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3, WKUP3

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
25	34	46	R5	56	F5	R5	L4	46	56	PB0	I/O	FT	(4) (5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, EVENTOUT	ADC1_IN8, ADC2_IN8
26	35	47	R4	57	G5	R4	M4	47	57	PB1	I/O	FT	(4) (5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, EVENTOUT	ADC1_IN9, ADC2_IN9
27	36	48	M6	58	K6	M6	J5	48	58	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, EVENTOUT	-
-	-	49	R6	59	-	R6	M5	49	59	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, EVENTOUT	-
-	-	50	P6	60	-	P6	L5	50	60	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	51	M8	61	-	M8	-	51	61	VSS	S	-	-	-	-
-	-	52	N8	62	-	N8	G5	52	62	VDD	S	-	-	-	-
-	-	53	N6	63	-	N6	K5	53	63	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	-	54	R7	64	-	R7	M6	54	64	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	-	55	P7	65	-	P7	L6	55	65	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	-	56	N7	66	-	N7	K6	56	66	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	57	M7	67	-	M7	J6	57	67	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	M13	86	-	M13	-	-	86	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, EVENTOUT	-
-	-	-	L13	87	-	L13	-	-	87	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, EVENTOUT	-
-	-	-	L12	88	-	L12	-	-	88	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, EVENTOUT	-
-	-	-	K12	89	-	K12	-	-	89	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, EVENTOUT	-
-	-	-	H12	90	-	H12	-	-	90	VSS	S	-	-	-	-
-	-	-	J12	91	K2	J12	-	-	91	VDD	S	-	-	-	-
33	51	73	P12	92	J2	P12	M11	73	92	PB12	I/O	FT	(4)	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT	-
34	52	74	P13	93	H2	P13	M12	74	93	PB13	I/O	FT	(4)	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, OTG_HS_ULPI_D6, EVENTOUT	OTG_HS_VBUS
-	-	-	-	-	G2	J15	H11	75	94	OTG_HS_REXT	-	-	-	USB HS OTG PHY calibration resistor	
-	-	-	-	-	G1	J14	H10	76	95	VDD12OTGHS	-	-	-	-	-

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/UART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port H	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	EVENTOUT
	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	FMC_D18	EVENTOUT
	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	FMC_D19	EVENTOUT
	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	FMC_D20	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	CAN1_TX	-	-	FMC_D21	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D22	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	EVENTOUT
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	EVENTOUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	EVENTOUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-	-	-	-	-	FMC_D26	EVENTOUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	EVENTOUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	-	FMC_NBL2	EVENTOUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	EVENTOUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	EVENTOUT

Table 28. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory on ITCM interface (ART disabled), regulator ON

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					TA= 25 °C	TA=85 °C	TA=105 °C	
I_{DD}	Supply current in RUN mode	All peripherals enabled(2)(3)	216	138	151	174.7	184	mA
			200	133	141	164.3	174	
			180	110	131	149.2	159	
			168	99	117	134	144	
			144	79	98	111.7	121	
			60	49	53	64	75	
			25	27	30	38.3	48	
		All peripherals disabled(3)	216	82	96	119.5	131	
			200	81	89	113.1	124	
			180	65	85	103.1	114	
			168	58	76	93.2	104	
			144	48	67	80.4	91	
			60	33	36	49.7	60	
			25	18	21	31.1	41	

1. Guaranteed by characterization results.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.73 mA per ADC for the analog part.

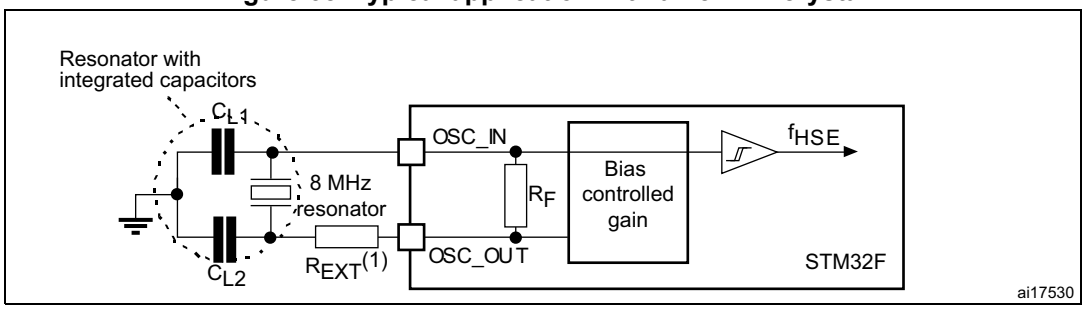
Table 36. Peripheral current consumption

Peripheral		I_{DD}(Typ)(1)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 216 MHz)	GPIOA	3.6	3.4	2.9	µA/MHz
	GPIOB	3.7	3.6	3.1	
AHB2 (up to 216 MHz)	GPIOC	3.7	3.4	3.0	µA/MHz
	GPIOD	3.7	3.6	3.0	
	GPIOE	3.6	3.4	2.9	
	GPIOF	3.5	3.4	2.9	
	GPIOG	3.5	3.3	2.8	
	GPIOH	3.5	3.4	2.9	
	GPIOI	3.5	3.3	2.9	
	CRC	1.2	1.1	0.9	
	BKPSRAM	0.8	0.7	0.6	
	DMA1	3.07 x N + 8.7	2.98 x N + 8.4	2.52 x N + 7.02	
	DMA2	3.01 x N + 7.98	2.95 x N + 7.95	2.48 x N + 6.69	
	OTG_HS+ULPI	54.4	53.2	44.6	
	RNG	1.9	1.8	1.6	
	USB_OTG_FS	28.7	27.9	23.5	
AHB3 (up to 216 MHz)	FMC	16.2	15.8	13.3	µA/MHz
	QSPI	16.9	16.3	13.8	
Bus matrix(2)		15.8	12.8	8.5	µA/MHz

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 38*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 38. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 60. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.19 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in *Table 61*.

Table 61. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0, PDR_ON, BYPASS_REG, OTG_HS_REXT	-0	0	mA
	Injected current on NRST	-0	NA	
	Injected current on PF9, PF10, PH0_OSCIN, PH1_OSCOUT, PC0, PC1, PC2, PC3, PB14(2), PB15(2)	-0	NA	
	Injected current on any other FT or FTf pins	-5	NA	
	Injected current on any other pins	-5	+5	

1. NA = not applicable.

Figure 53. SPI timing diagram - slave mode and CPHA = 1

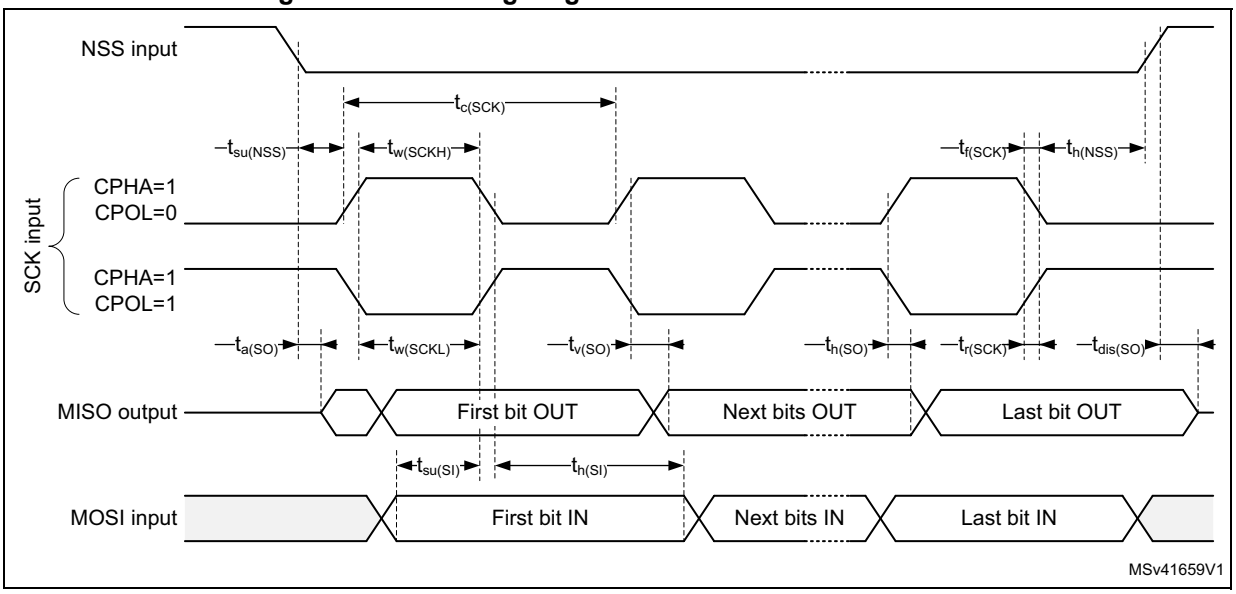
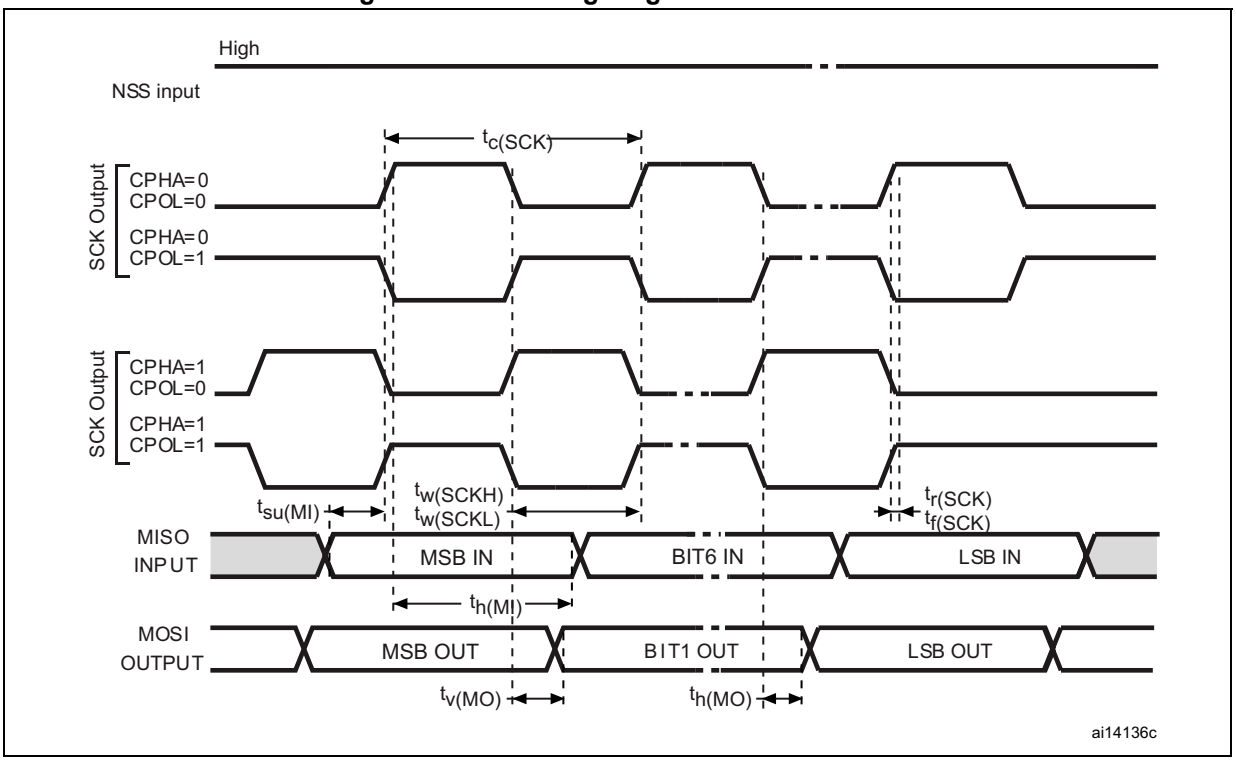


Figure 54. SPI timing diagram - master mode



SAI characteristics

Unless otherwise specified, the parameters given in *Table 84* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 84. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256x8K	256xFs	MHz
F_{CK}	SAI clock frequency(2)	Master data: 32 bits	-	128xFs(3)	
		Slave data: 32 bits	-	128xFs(3)	
$t_{v(FS)}$	FS valid time	Master mode 2.7≤VDD≤3.6V	-	18	ns
		Master mode 1.71≤VDD≤3.6V	-	20	
$t_{su(FS)}$	FS setup time	Slave mode	1	-	
$t_{h(FS)}$	FS hold time	Master mode	7	-	
		Slave mode	0.5	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	3.5	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	0.5		
$t_{v(SD\_B\_MT)}$	Data output valid time	Slave transmitter (after enable edge) 2.7≤VDD≤3.6V	-	11	
		Slave transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	5	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7≤VDD≤3.6V	-	16	
		Master transmitter (after enable edge) 1.71≤VDD≤3.6V	-	18.5	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	7.5	-	

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With Fs = 192 KHz.

1. Guaranteed by characterization results.

Table 101. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk -0.5	7Thclk + 0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 65 through *Figure 68* represent synchronous waveforms and *Table 102* through *Table 105* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

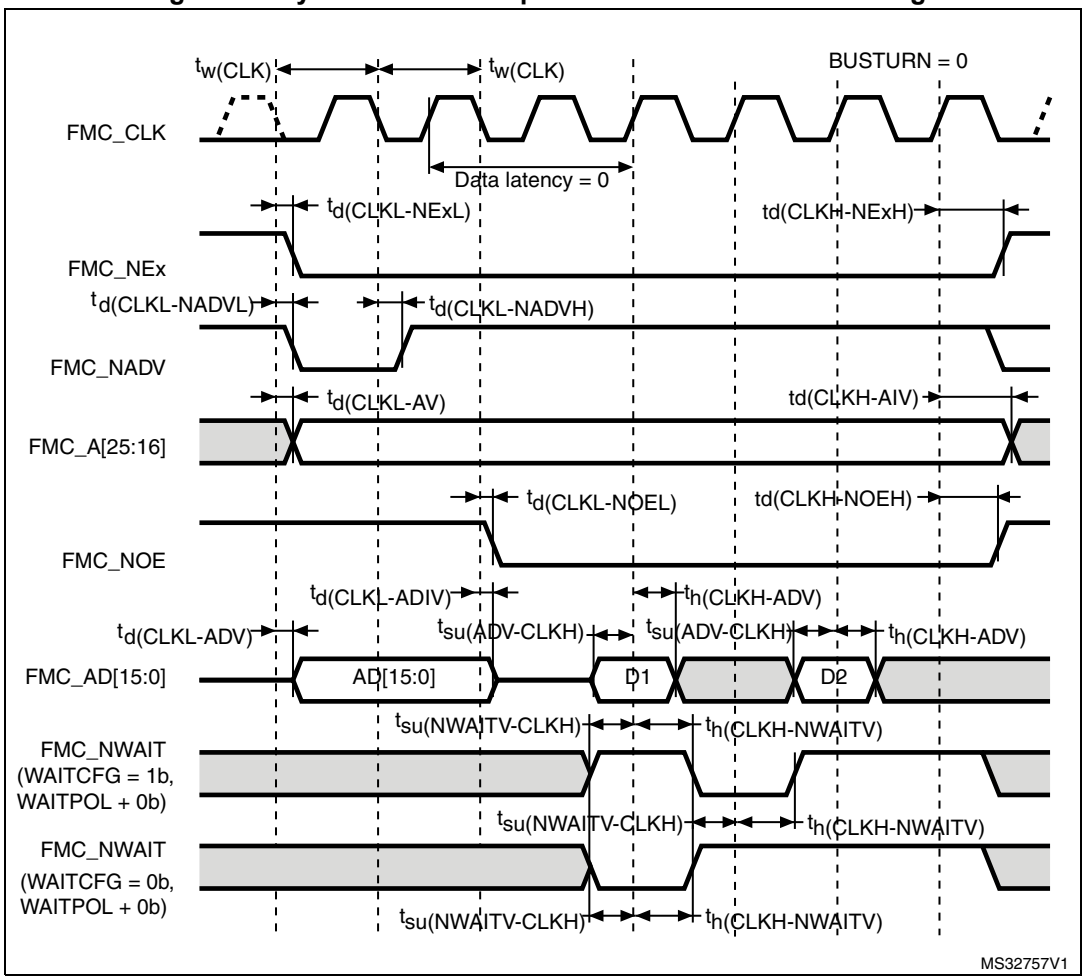
- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

– For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Figure 65. Synchronous multiplexed NOR/PSRAM read timings

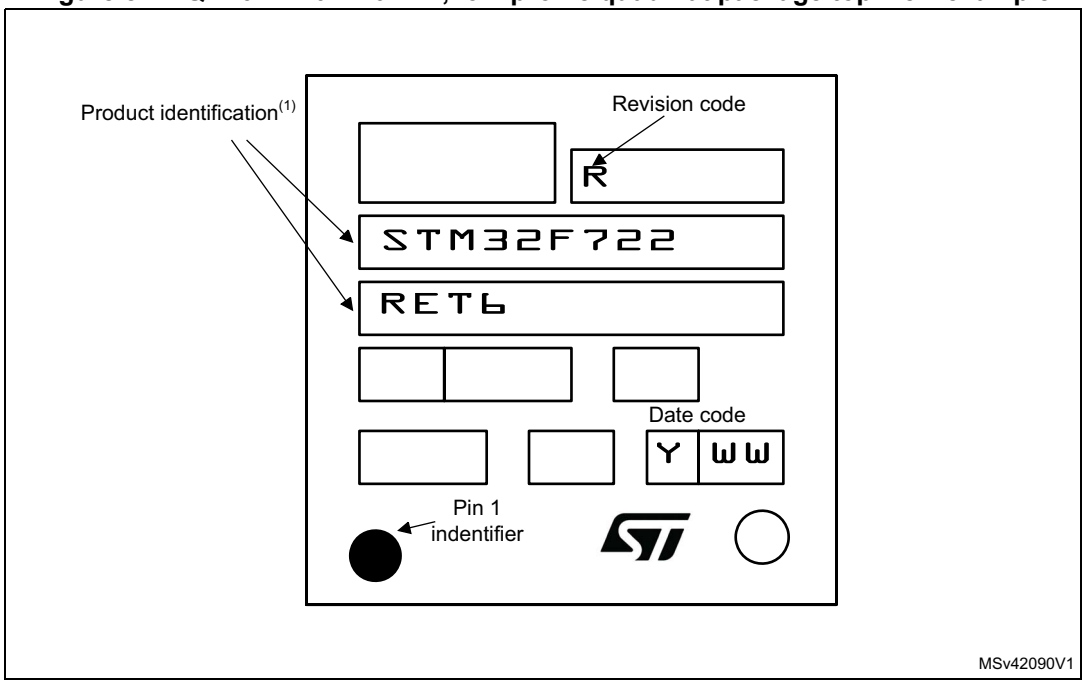


LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 81. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example



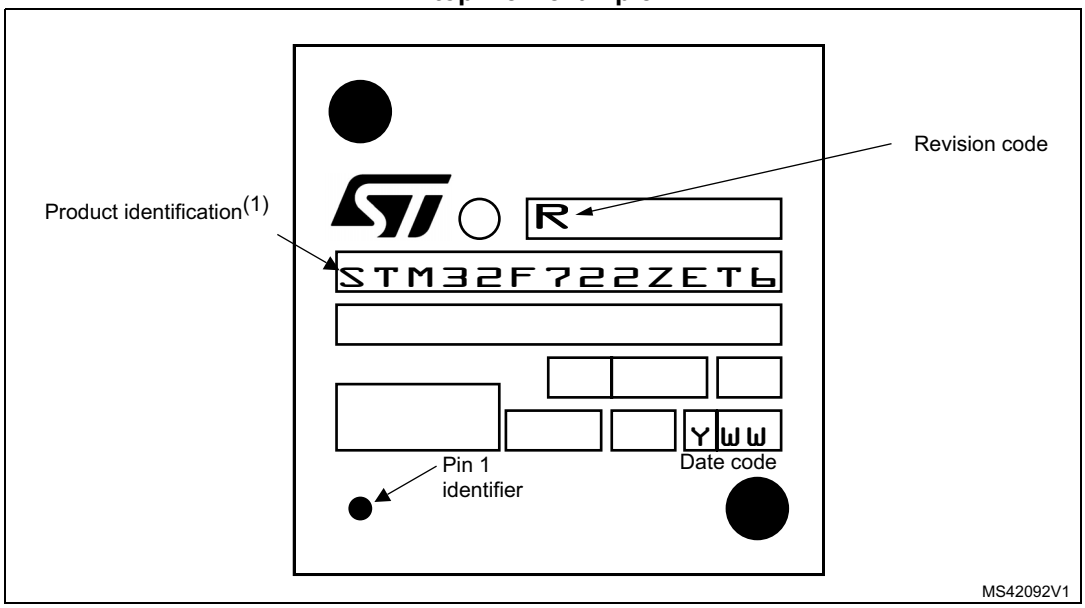
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

LQP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

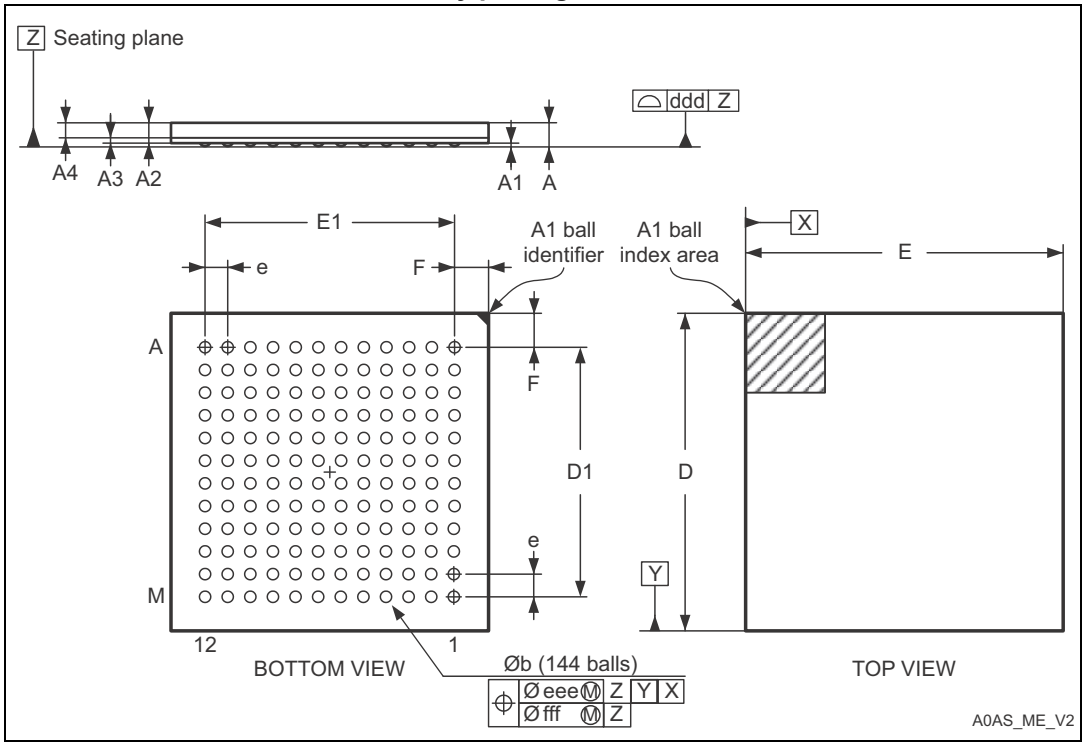
Figure 87. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.5 UFBGA144 package information

Figure 91. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 120. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.230	0.280	0.320	0.0091	0.0110	0.0126
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

Table 120. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 92. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

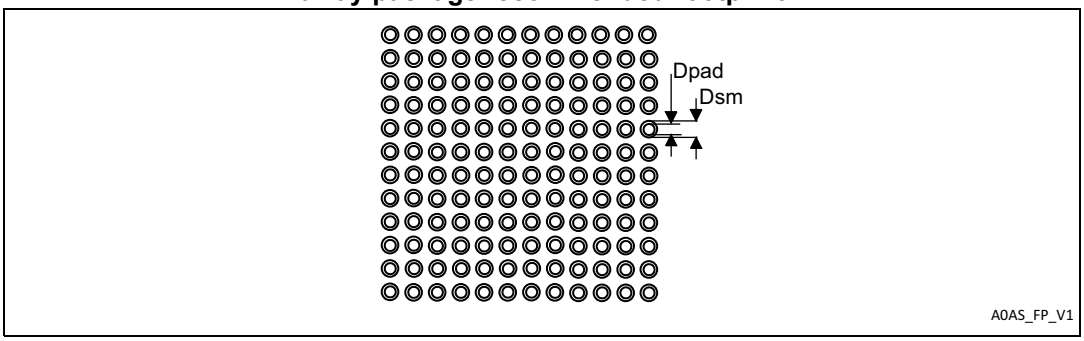


Table 121. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm