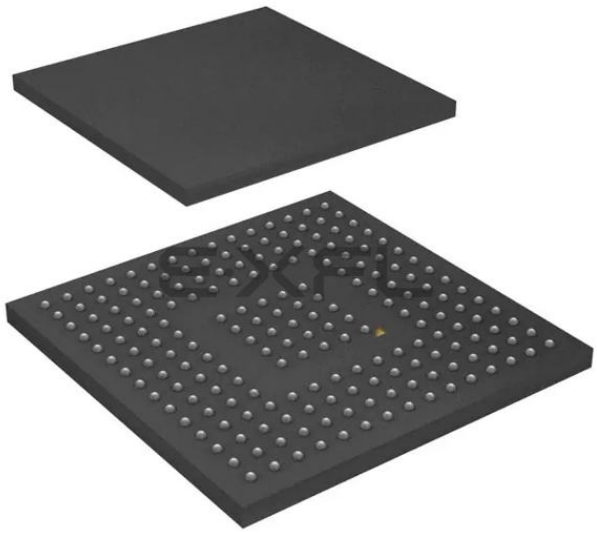

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	140
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-UFBGA
Supplier Device Package	176-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f722iek6

1 Description

The STM32F722xx and STM32F723xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F722xx and STM32F723xx devices incorporate high-speed embedded memories with a Flash memory up to 512 Kbytes, 256 Kbytes of SRAM (including 64 Kbytes of data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Five SPIs, three I^2Ss in half duplex mode. To achieve the audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI in the STM32F722xx devices and with the integrated HS PHY in the STM32F723xx devices)
- One CAN
- Two SAI serial audio interfaces
- Two SDMMC host interfaces

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface. Refer to *Table 2: STM32F722xx and STM32F723xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F722xx and STM32F723xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for the USB (OTG_FS and OTG_HS) and the SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 and LQFP64 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.15.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F722xx and STM32F723xx devices offer devices in 7 packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

1.2 STM32F723xx versus STM32F722xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

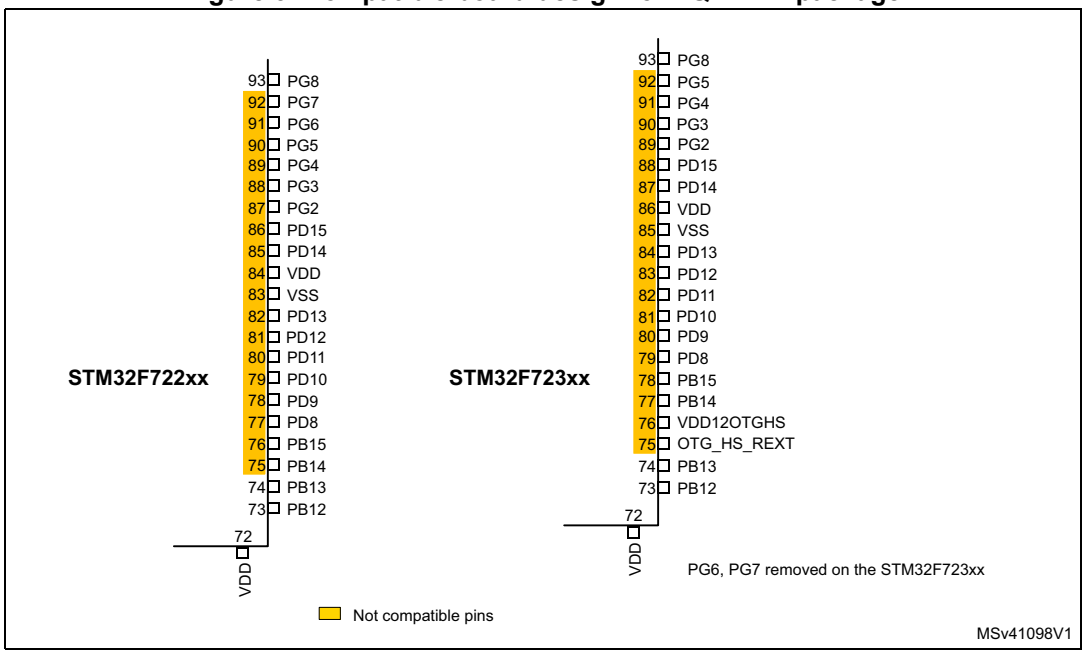
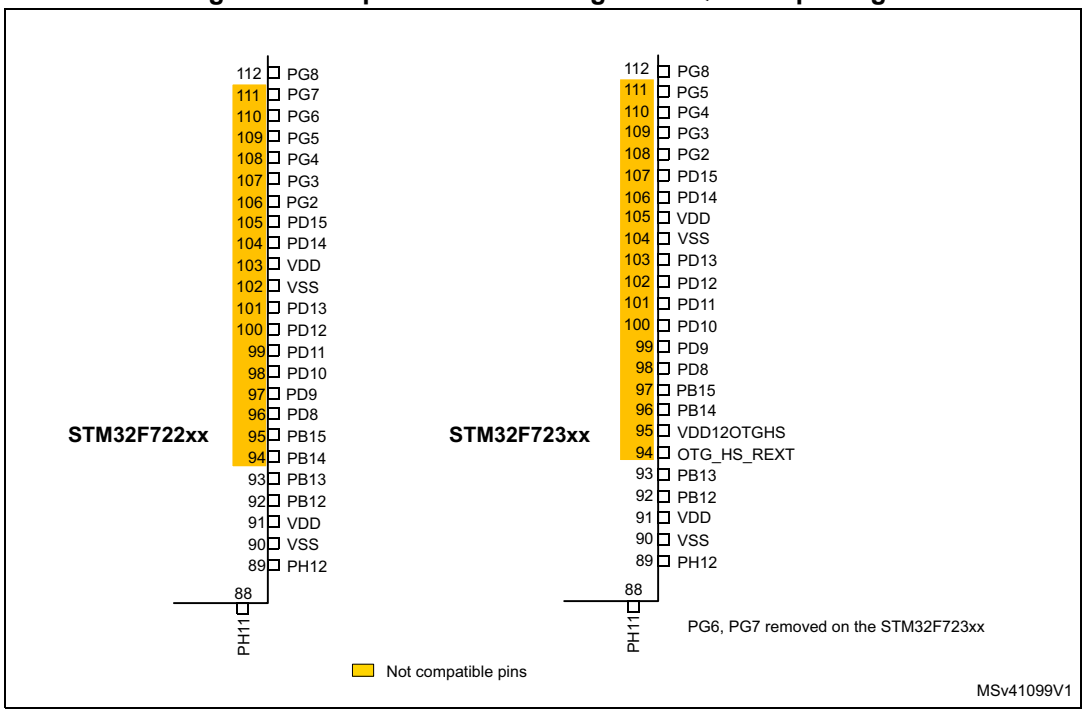


Figure 4. Compatible board design for LQFP176 package



2.3 Embedded Flash memory

The STM32F722xx and STM32F723xx devices embed a Flash memory of up to 512 Kbytes available for storing programs and data.

The flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: No access (read, erase, program) to the Flash memory or backup SRAM can be performed while the debug feature is connected or while booting from RAM or system memory bootloader
  - Level 2: debug/chip read protection disabled.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): Flash memory user sectors (0 to 7) can be protected against D-bus read accesses by using the proprietary readout protection (PCROP). The protected area is execute-only.

2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 256 Kbytes:
  - SRAM1 on AHB bus Matrix: 176 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 64 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripheral DMAs through the specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

– The V_{DDUSB} rising and falling time rate specifications must be respected
– In the operating mode phase, V_{DDUSB} could be lower or higher than V_{DD}:
  - If the USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX}.
  - The V_{DDUSB} supplies both USB transceiver (USB OTG_HS and USB OTG_FS). If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB}.
  - If the USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX}.

Figure 7. V_{DDUSB} connected to V_{DD} power supply

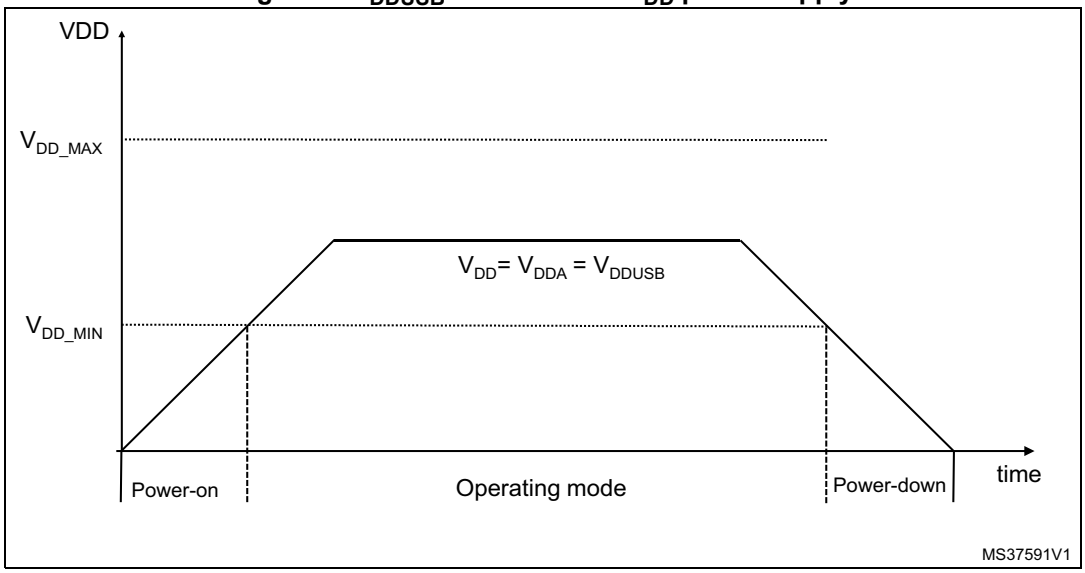
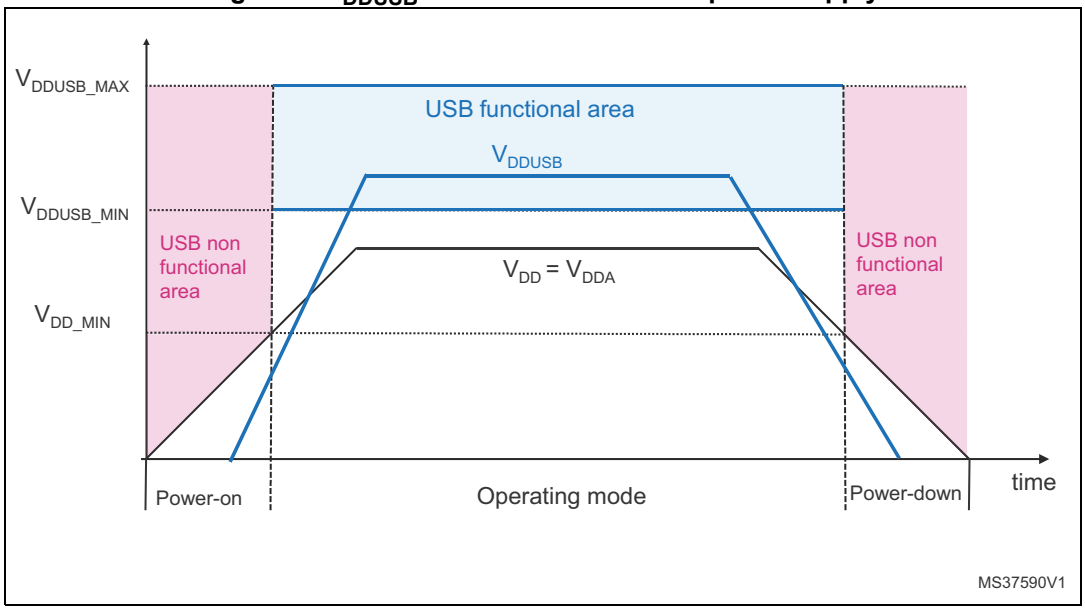


Figure 8. V_{DDUSB} connected to external power supply



- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

Universal Serial Bus controller on-the-go High-Speed PHY controller (USBPHYC) only on STM32F723xx devices.

The USB HS PHY controller:

– Sets the PHYPLL1/2 values for the PHY HS
– Sets the other controls on the PHY HS
– Controls and monitors the USB PHY's LDO

2.31 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.32 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

A Fast I/O handling allows a maximum I/O toggling up to 108 MHz.

2.33 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In the scan mode, an automatic conversion is performed on a selected group of analog inputs.

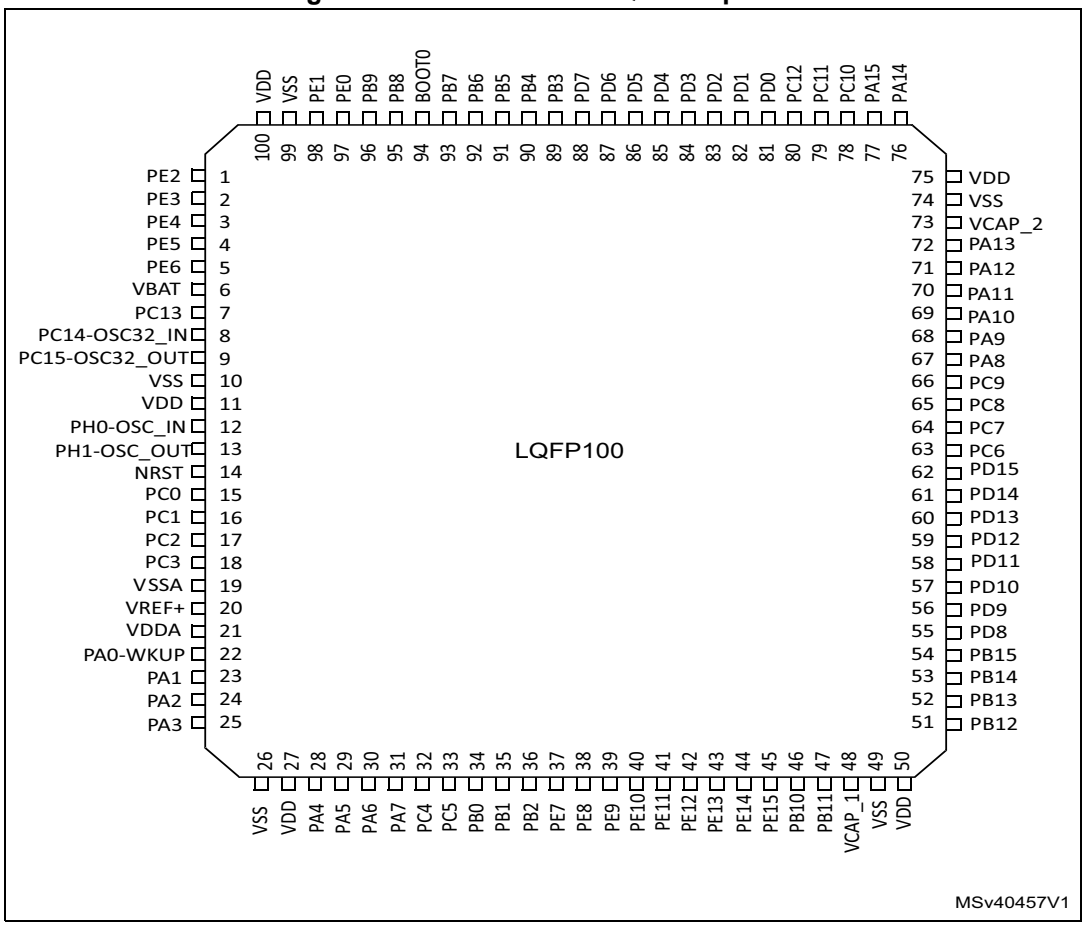
Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

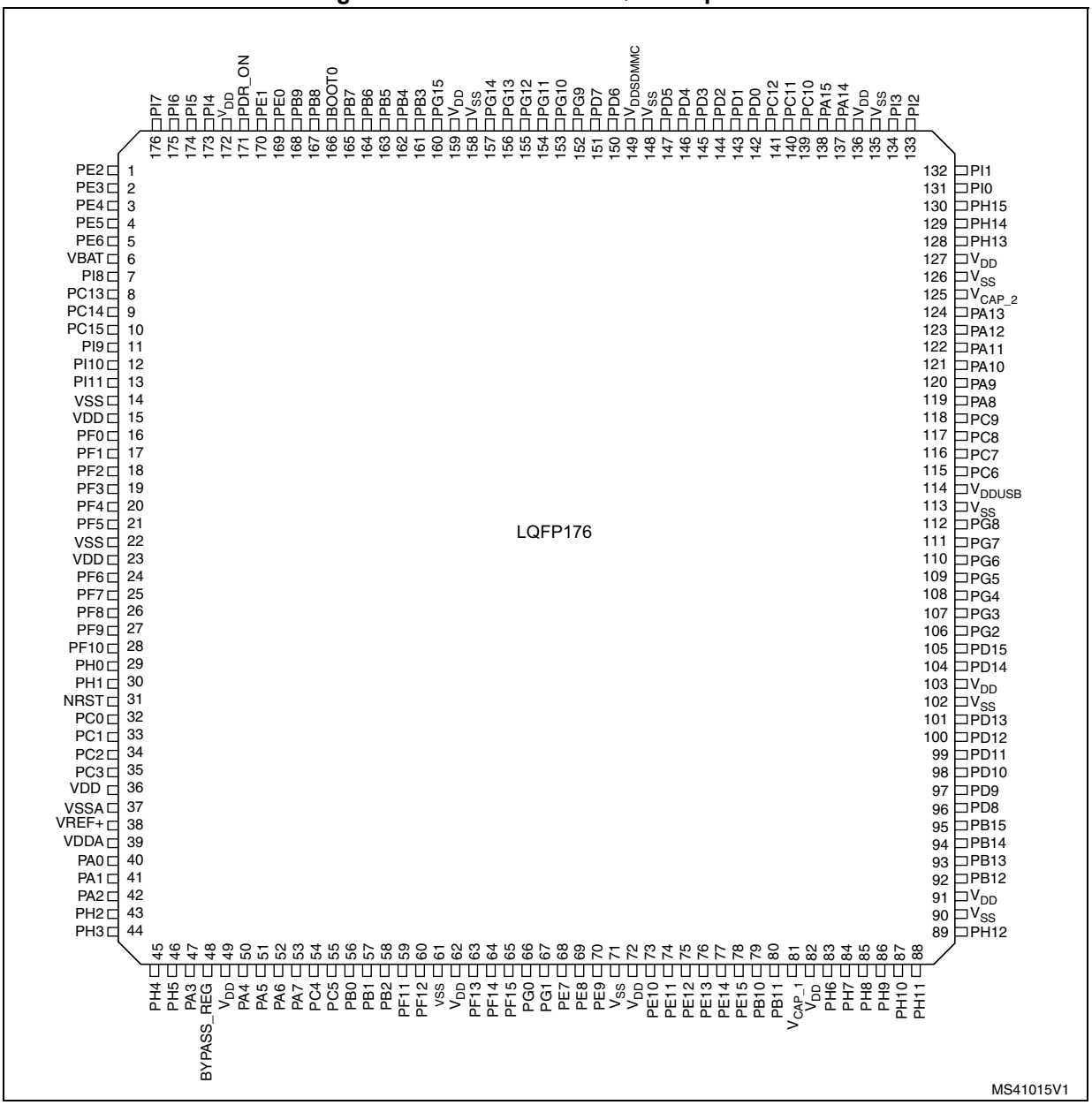
To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

Figure 15. STM32F722xx LQFP100 pinout



1. The above figure shows the package top view.

Figure 20. STM32F722xx LQFP176 pinout



1. The above figure shows the package top view.

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
-	-	-	D2	7	-	D2	-	-	7	PI8	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP2/ RTC_TS, WKUP5
2	7	7	D1	8	D10	D1	A1	7	8	PC13	I/O	FT	(2) (3)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT, WKUP4
3	8	8	E1	9	E9	E1	B1	8	9	PC14-OSC32_IN(PC14)	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
4	9	9	F1	10	E10	F1	C1	9	10	PC15-OSC32_OUT(PC15)	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT
-	-	-	D3	11	-	D3	-	-	11	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, EVENTOUT	-
-	-	-	E3	12	-	E3	-	-	12	PI10	I/O	FT	-	FMC_D31, EVENTOUT	-
-	-	-	E4	13	-	E4	-	-	13	PI11	I/O	FT	(4)	OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	-	F2	14	-	F2	-	-	14	VSS	S	-	-	-	-
-	-	-	F3	15	-	F3	-	-	15	VDD	S	-	-	-	-

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	B1	A15	A12	105	124	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port A	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	-	UART4_RTS	-	-	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	UART4_CTS		OTG_HS_ULPI_D1	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-		OTG_HS_ULPI_D2	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SD		QUADSPI_CLK	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	-	-	SDMMC2_D2	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	-	-	SDMMC2_D3	-	-	EVENTOUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	-	OTG_HS_ULPI_D7	-	FMC_SDCKE1	EVENTOUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	QUADSPI_BK1_NCS	-	FMC_SDNE1	EVENTOUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	SDMMC2_D4	-	SDMMC1_D4	EVENTOUT

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	EVENTOUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	EVENTOUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	UART7_RTS	TIM13_CH1	QUADSPI_BK1_IO0	-	-	EVENTOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	UART7_CTS	TIM14_CH1	QUADSPI_BK1_IO1	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	EVENTOUT
Port F	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	EVENTOUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	EVENTOUT
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	EVENTOUT

Figure 59. USB OTG full speed timings: definition of data signal rise and fall time

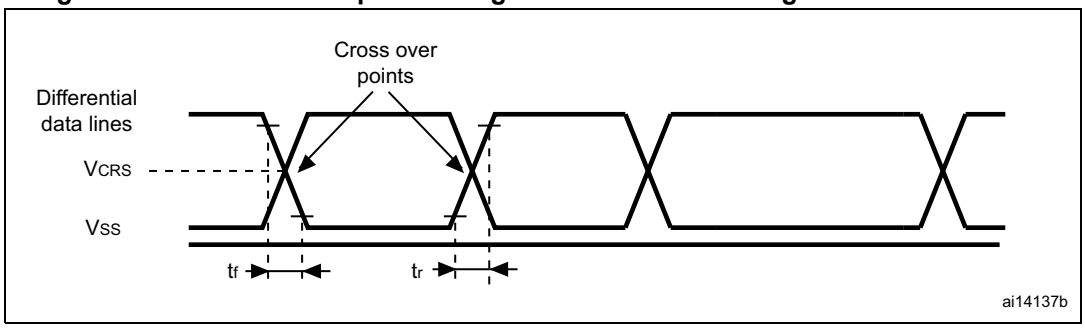


Table 87. USB OTG full speed electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics (through ULPI in STM32F722xx devices)

Unless otherwise specified, the parameters given in *Table 90* for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in *Table 89* and V_{DD} supply voltage conditions summarized in *Table 88*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

Table 88. USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	USB OTG HS operating voltage	1.7	3.6	V

1. All the voltages are measured from the local ground potential.

Table 93. USB FS PHY BCD electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDUSB}	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	
R_{DAT_LKG}	Data line leakage resistance	-	300	-	-	kΩ
V_{DAT_LKG}	Data line leakage voltage	-	0.0	-	3.6	V
R_{DCP_DAT}	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
V_{LGC_HI}	Logic high	-	2.0	-	3.6	V
V_{LGC_LOW}	Logic low	-	-	-	0.8	
VL_{GC}	Logic threshold	-	0.8	-	2.0	
V_{DAT_REF}	Data detect voltage	-	0.25	-	3.6	
V_{DP_SRC}	D+ source voltage	-	0.5	-	3.6	
V_{DM_SRC}	D- source voltage	-	0.5	-	3.6	
I_{DM_SINK}	D- sink current	-	25	-	175	µA
I_{DP_SINK}	D+ sink current	-	25	-	175	
I_{DP_SRC}	Data contact detect current source	-	7	-	30	

CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 94* to *Table 107* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 61 through *Figure 64* represent asynchronous waveforms and *Table 94* through *Table 101* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the T_{HCLK} is the HCLK clock period

Table 94. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	2Thclk -1	2Thclk +1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	0.5	
$t_{w(NOE)}$	FMC_NOE low time	2Thclk -1	2Thclk +1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	Thclk -1.5	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	Thclk -1.5	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	0	
$t_{w(NADV)}$	FMC_NADV low time	-	Thclk -0.5	

1. C_L = 30 pF.

Table 95. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	7Thclk +1	7Thclk +1	ns
$t_{w(NOE)}$	FMC_NWE low time	5Thclk -1	5Thclk +1	
$t_{w(NWAIT)}$	FMC_NWAIT low time	Thclk -0.5	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5Thclk +1.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk +1	-	

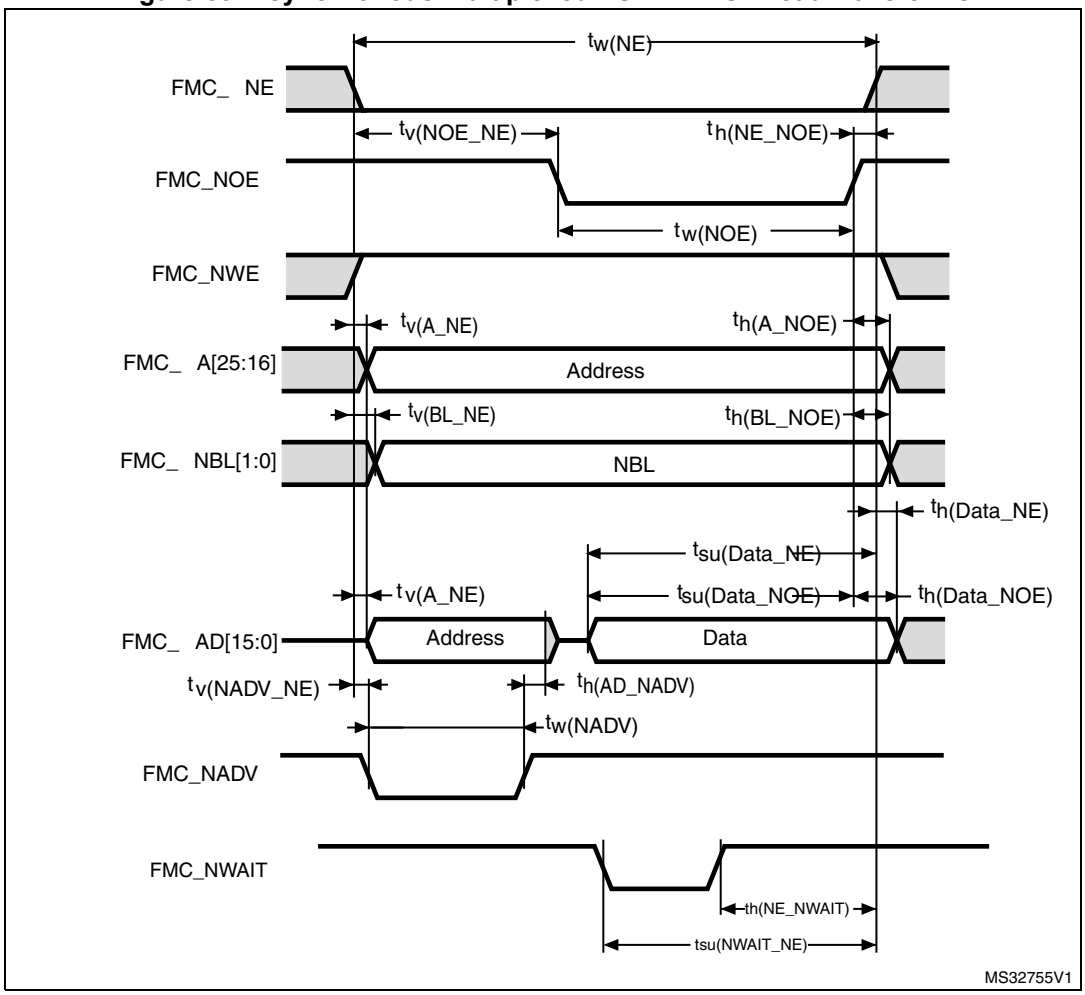
1. Guaranteed by characterization results.

Table 97. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8Thclk -1	8Thclk +1	ns
$t_{w(NWE)}$	FMC_NWE low time	6Thclk -1.5	6Thclk +0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk -1	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk + 2	-	

1. Guaranteed by characterization results.

Figure 63. Asynchronous multiplexed PSRAM/NOR read waveforms



1. Guaranteed by characterization results.

Table 101. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk -0.5	7Thclk + 0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 65 through *Figure 68* represent synchronous waveforms and *Table 102* through *Table 105* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

– For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).

– For 1.71 V≤V_{DD}<2.7 V, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

Table 112. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN)	Data input setup time	-	3	-	-	
th(IN)	Data input hold time		1	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3	
		1.71 V<V_{DD}<3.6 V	-	1.5	2.5	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 113. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	1	-	-	
		1.71 V<V_{DD}<2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	2.25	-	-	
		1.71 V<V_{DD}<2 V	2.75	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	9.5	11.5	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	9.5	12.25	
		DHHC=1 Pres=1, 2...	-	Thclk/2 +2	Thclk/2 +2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	5.5	-	-	
		DHHC=1 Pres=1, 2...	Thclk/2 +0.75	-	-	

1. Guaranteed by characterization results.

Figure 77. SDIO high-speed mode

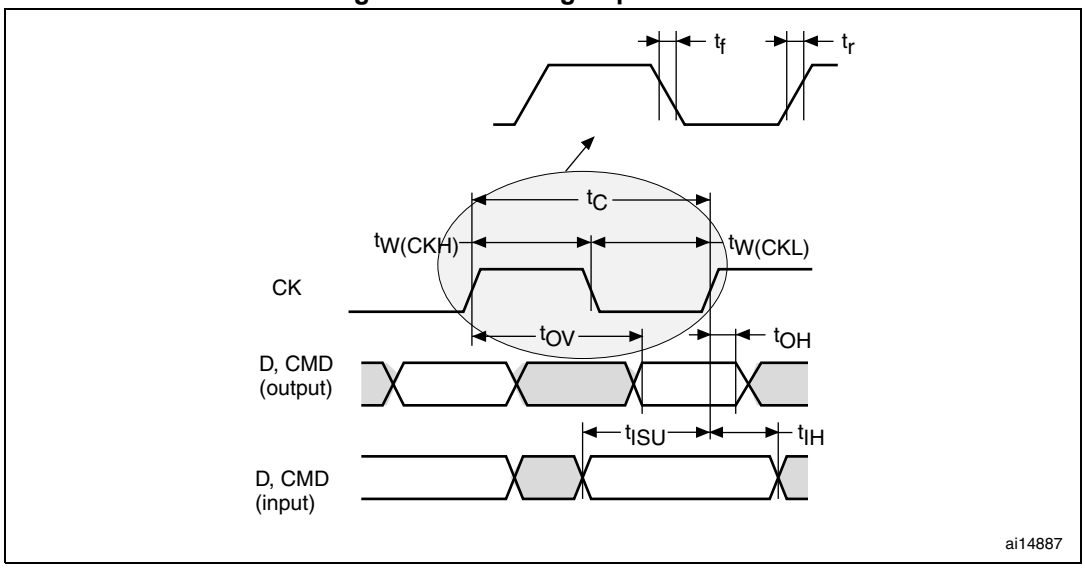


Figure 78. SD default mode

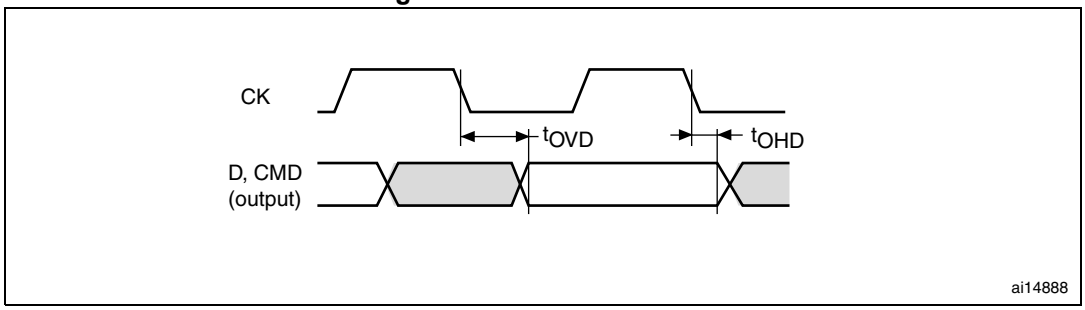


Table 114. Dynamic characteristics: SD / MMC characteristics, V_{DD}=2.7V to 3.6V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDMMC_CK/fPCLK2 frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	fpp =50 MHz	9	10	-	ns
$t_{W(CKH)}$	Clock high time	fpp =50 MHz	9	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	fpp =50 MHz	1	-	-	ns
t_{IH}	Input hold time HS	fpp =50 MHz	3	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	fpp =50 MHz	-	11	12	ns
t_{OH}	Output hold time HS	fpp =50 MHz	9	-	-	

Table 120. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 92. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

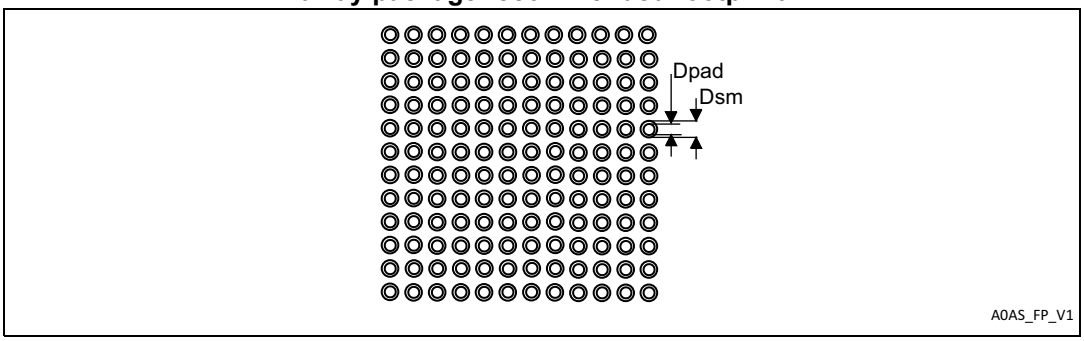


Table 121. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm