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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f722ret6

1 Description

The STM32F722xx and STM32F723xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a single floating point unit (SFPU) precision which supports ARM® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances the application security.

The STM32F722xx and STM32F723xx devices incorporate high-speed embedded memories with a Flash memory up to 512 Kbytes, 256 Kbytes of SRAM (including 64 Kbytes of data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, thirteen general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Five SPIs, three I^2Ss in half duplex mode. To achieve the audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI in the STM32F722xx devices and with the integrated HS PHY in the STM32F723xx devices)
- One CAN
- Two SAI serial audio interfaces
- Two SDMMC host interfaces

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface. Refer to *Table 2: STM32F722xx and STM32F723xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F722xx and STM32F723xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for the USB (OTG_FS and OTG_HS) and the SDMMC2 (clock, command and 4-bit data) are available on all the packages except LQFP100 and LQFP64 for a greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.15.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F722xx and STM32F723xx devices offer devices in 7 packages ranging from 64 pins to 176 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F722xx and STM32F723xx microcontrollers suitable for a wide range of applications:

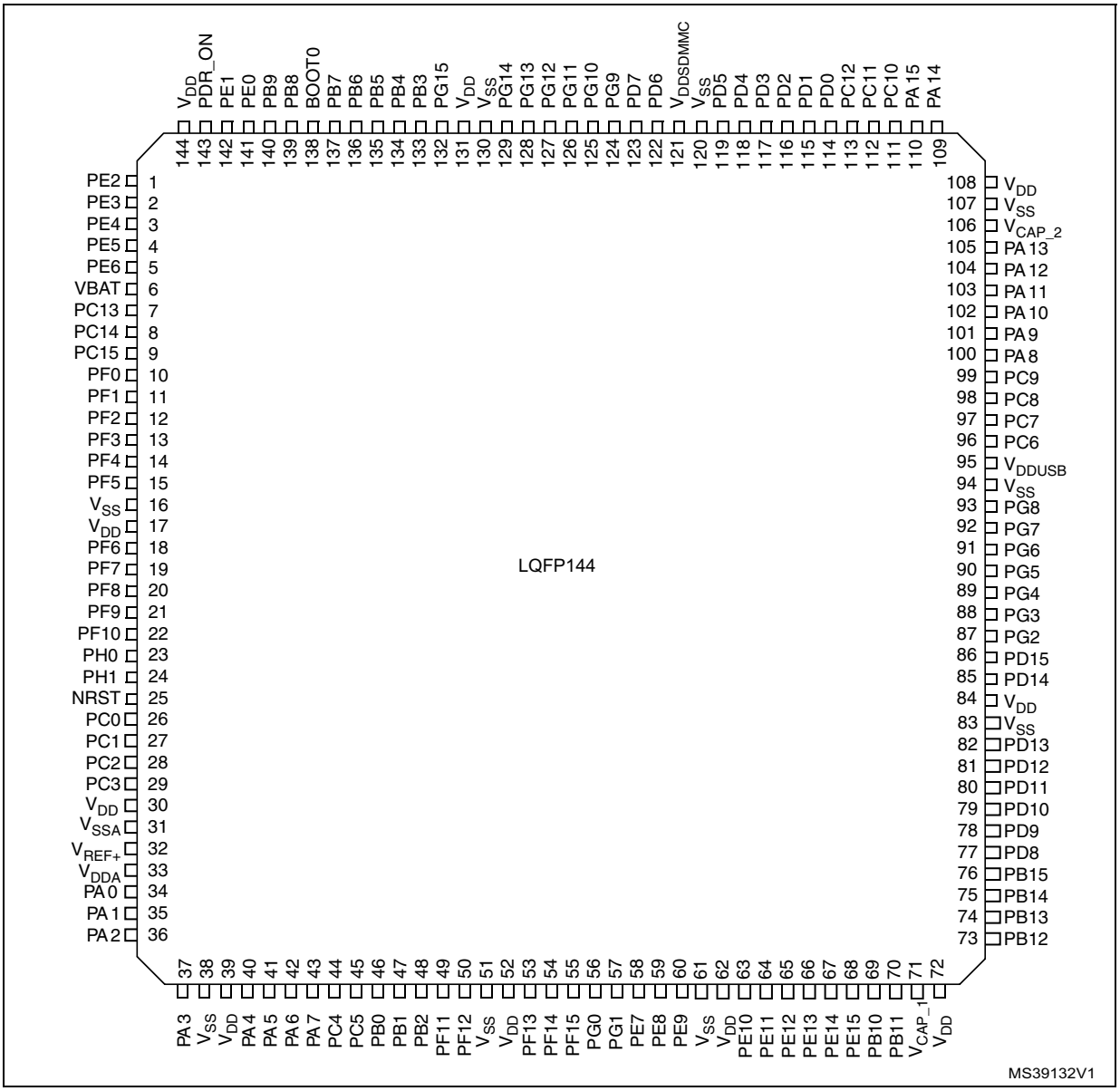
- Motor drive and application control,
- Medical equipment,
- Industrial applications: PLC, inverters, circuit breakers,
- Printers, and scanners,
- Alarm systems, video intercom, and HVAC,
- Home audio appliances,
- Mobile applications, Internet of Things,
- Wearable devices: smartwatches.

Figure 5 shows the general block diagram of the device family

Table 2. STM32F722xx and STM32F723xx features and peripheral counts

Peripherals		STM32F72xRx		STM32F72xVx		STM32F72xZx		STM32F72xIx	
Flash memory in Kbytes		256	512	256	512	256	512	256	512
SRAM in Kbytes	System	256(176+16+64)							
	Instruction	16							
	Backup	4							
FMC memory controller		No		Yes(1)					
Quad-SPI		Yes							
Timers	General-purpose	10(2)							
	Advanced-control	2							
	Basic	2							
	Low-power	No		1					
Random number generator		Yes							
Communication interfaces	SPI / I^2S	3/3 (simplex)(3)		4/3 (simplex)(3)		5/3 (simplex)(3)			
	I^2C	3							
	USART/UART	4/2		4/4					
	USB OTG FS	Yes							
	USB OTG HS(4)	Yes							
	USB OTG PHY HS controller (USBPHYC)	No		Yes(10)					
	CAN	1							
	SAI	2							
	SDMMC1	Yes							
	SDMMC2	No		Yes(5)(6)					
GPIOs		50		82 in STM32F722xx 79 in STM32F723xx		114 in STM32F722xx 112 in STM32F723xx		140 in STM32F722xx 138 in STM32F723xx	
12-bit ADC		3							
Number of channels		16				24			
12-bit DAC Number of channels		Yes 2							
Maximum CPU frequency		216 MHz(7)							

Figure 17. STM32F722xx LQFP144 pinout



1. The above figure shows the package top view.

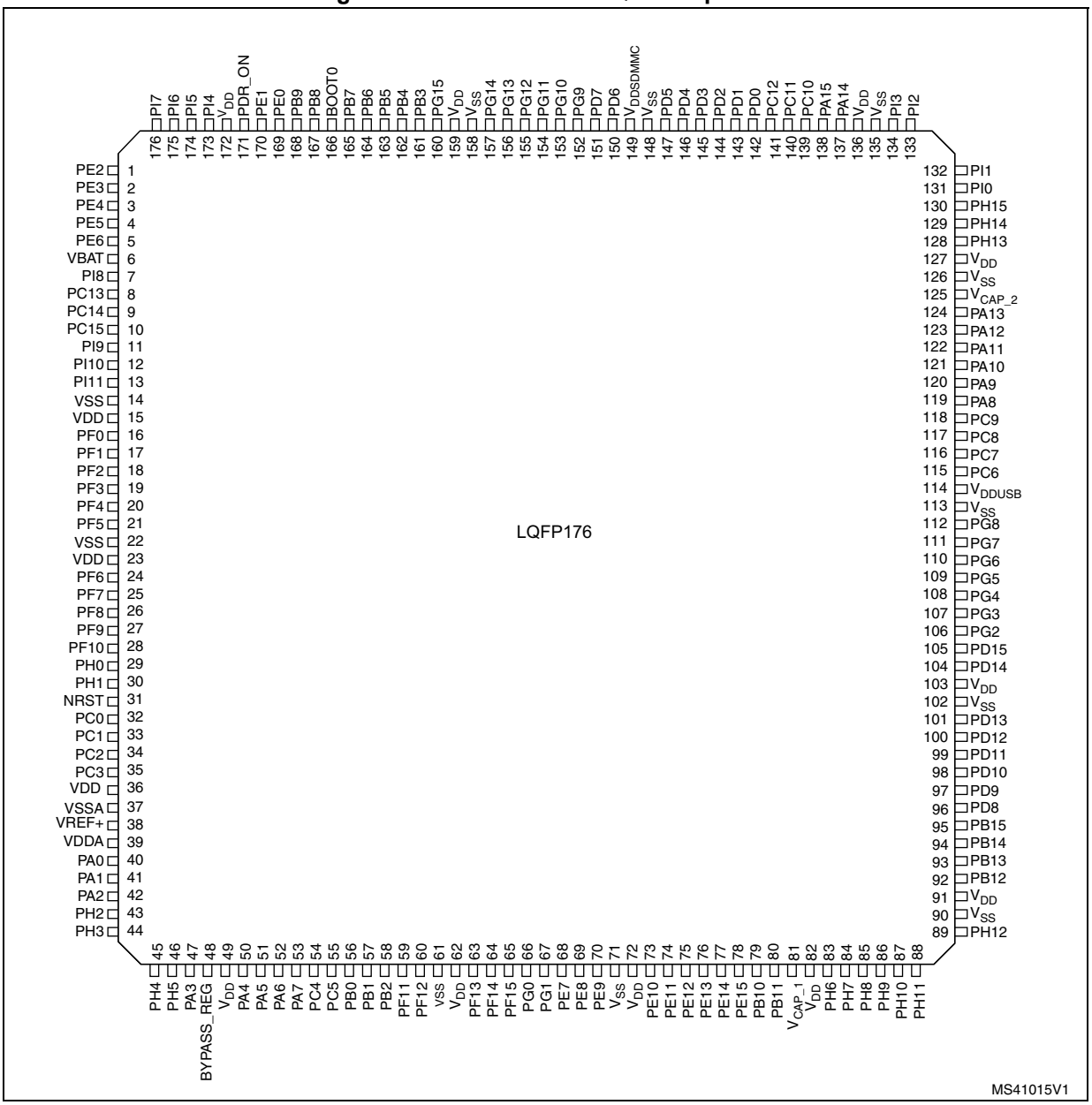
Figure 19. STM32F723xx UFBGA144 ballout (with OTG PHY HS)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PC13	PE3	PE2	PE1	PE0	PB4	PB3	PD6	PD7	PA15	PA14	PA13
B	PC14-OSC32_IN	PE4	PE5	PE6	PB9	PB5	PG15	PG12	PD5	PC11	PC10	PA12
C	PC15-OSC32_OUT	VBAT	PF0	PF1	PB8	PB6	PG14	PG11	PD4	PC12	VDDUSB	PA11
D	PH0 - OSC_IN	VSS	VDD	PF2	BOOT0	PB7	PG13	PG10	PD3	PD1	PA10	PA9
E	PH1 - OSC_OUT	PF3	PF4	PF5	PDR_ON	VSS	VSS	PG9	PD2	PD0	PC9	PA8
F	NRST	PF7	PF6	VDD	VDD	VDD	VDD	VDD	VDD	VDD	PC8	PC7
G	PF10	PF9	PF8	VSS	VDD	VDD	VDD	VSS	VCAP_2	VSS	PG8	PC6
H	PC0	PC1	PC2	PC3	BYPASS_REG	VSS	VCAP_1	PE11	PD11	VDD12OTGHS	OTG_HS_REXT	PG5
J	VSSA	PA0	PA4	PC4	PB2	PG1	PE10	PE12	PD10	PG4	PG3	PG2
K	VREF-	PA1	PA5	PC5	PF13	PG0	PE9	PE13	PD9	PD13	PD14	PD15
L	VREF+	PA2	PA6	PB0	PF12	PF15	PE8	PE14	PD8	PD12	PB14	PB15
M	VDDA	PA3	PA7	PB1	PF11	PF14	PE7	PE15	PB10	PB11	PB12	PB13

MSv42000V1

1. The above figure shows the package top view.

Figure 20. STM32F722xx LQFP176 pinout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5V tolerant I/O, I2C Fm+ option.
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

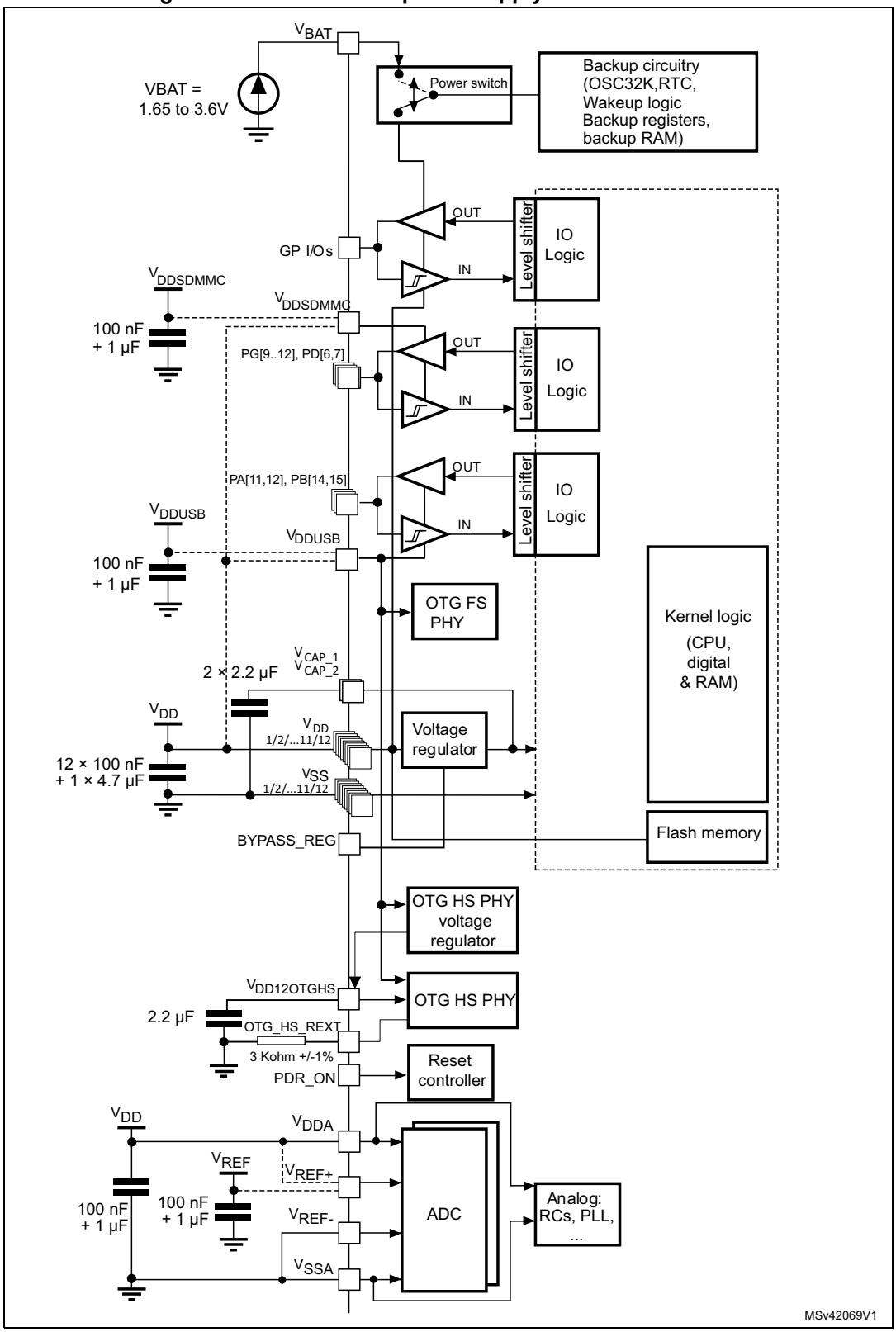
Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
39	65	98	G14	117	D2	G14	F11	98	117	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT	-
40	66	99	F14	118	D1	F14	E11	99	118	PC9	I/O	FTf	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT	-
41	67	100	F15	119	D3	F15	E12	100	119	PA8	I/O	FTf	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT	-
42	68	101	E15	120	C3	E15	D12	101	120	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT	OTG_FS_VBUS
43	69	102	D15	121	C2	D15	D11	102	121	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT	-
44	70	103	C15	122	C1	C15	C12	103	122	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT	-
45	71	104	B15	123	B2	B15	B12	104	123	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	72	105	A15	124	B1	A15	A12	105	124	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

Table 12. STM32F722xx and STM32F723xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_ TX	-	SAI2_SD_B	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	-	-	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	-	OTG_HS_ULPI_D0	-	-	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	-	-	OTG_HS_ULPI_CK	-	-	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	-	TIM14_CH1	-	-	FMC_SDNWE	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	EVENTOUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	EVENTOUT

Figure 28. STM32F723xx power supply scheme

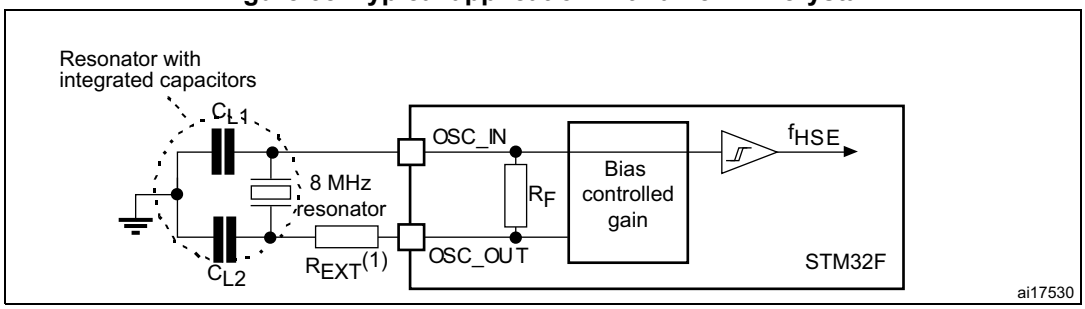


1. The V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and the PHY HS on PB14/PB15.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 38*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 38. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 Low drive capability	-	250	-	nA
		LSEDRV[1:0]=10 Medium low drive capability	-	300	-	
		LSEDRV[1:0]=01 Medium high drive capability	-	370	-	
		LSEDRV[1:0]=11 High drive capability	-	480	-	

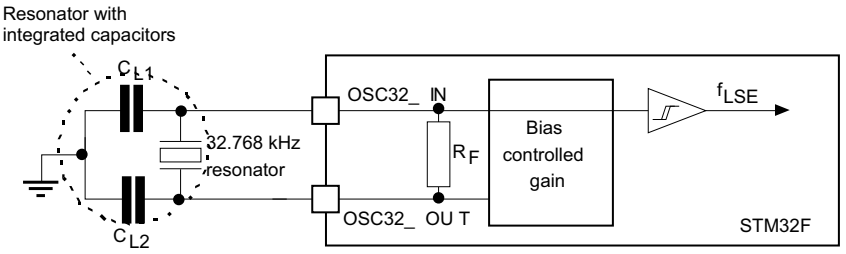
Table 42. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_m_crit_max	Maximum critical crystal g_m	LSEDRV[1:0]=00 Low drive capability	-	-	0.48	µA/V
		LSEDRV[1:0]=10 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0]=01 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0]=11 High drive capability	-	-	2.7	
t_{SU}(2)	start-up time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Guaranteed by characterization results. t_{SU} is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST Microelectronics website www.st.com.

Figure 39. Typical application with a 32.768 kHz crystal



5.3.13 USB OTG HS PHY PLLs characteristics (on STM32F723xx devices)

The parameters given in *Table 49* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 49. USB OTG HS PLL1 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL1_IN}	PLL1 input clock	-	12, 12.5, 16, 24, 25			MHz
f_{PLL1_OUT}	PLL1 output clock(2)	-	-	60	-	
f_{VCO_OUT}	PLL1 VCO output	-	600	-	720	
t_{LOCK}	PLL1 lock time(2)	-	-	-	22	µs
$I_{DD(PLL1)}$	PLL1 digital power consumption	-	-	-	1.8	mA
$I_{DDA(PLL1)}$	PLL1 analog power consumption	-	-	-	2.75	

1. Guaranteed by design.
2. Based on test during characterization.

Table 50. USB OTG HS PLL2 characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL2_IN}	PLL2 input clock	-	-	60	-	MHz
f_{PLL2_OUT}	PLL2 output clock(2)	-	-	480	-	
f_{VCO_OUT}	PLL2 VCO output	-	-	480	-	
t_{LOCK}	PLL2 lock time(2)	-	-	-	91	µs
$I_{DD(PLL2)}$	PLL2 digital power consumption	-	-	-	2.1	mA
$I_{DDA(PLL2)}$	PLL2 analog power consumption	-	-	-	1.5	

1. Guaranteed by design.
2. Based on test during characterization.

5.3.14 USB OTG HS PHY regulator characteristics (on STM32F723xx devices)

The parameters given in *Table 51* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 51. USB OTG HS PHY regulator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD12OTGHS}$	1.2 V internal voltage on $V_{DD12OTGHS}$	-	1.18	1.2	1.24	V
CEXT	External capacitor on $V_{DD12OTGHS}$	-	1.1	2.2	3.3	µF
$I_{DDPHYHSREG}$	Regulator power consumption	-	100	120	125	µA

1. Based on test during characterization.

2. PB14 and PB15 in the STM32F723xx devices.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.20 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 62: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 62. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04$(1) $0.3V_{DD}$(2)	V
	BOOT I/O input low level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	-	$0.1V_{DD}+0.1$(1)	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3$(1) $0.7V_{DD}$(2)	-	-	V
	BOOT I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7$(1)	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	$10\%V_{DD}$(3)	-	-	V
	BOOT I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	0.1	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)	V_{IN} = 5 V	-	-	3	

5.3.25 Temperature sensor characteristics

Table 74. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 75. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FF0 7A2C - 0x1FF0 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FF0 7A2E - 0x1FF0 7A2F

5.3.26 V_{BAT} monitoring characteristics

Table 76. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(2)(2)	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

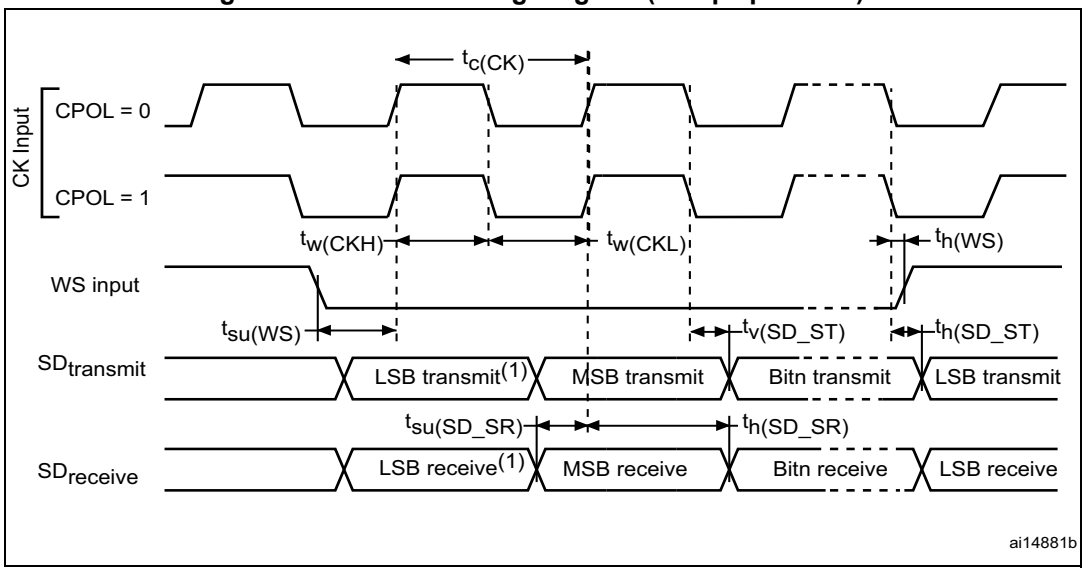
5.3.27 Reference voltage

The parameters given in *Table 77* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 77. internal reference voltage

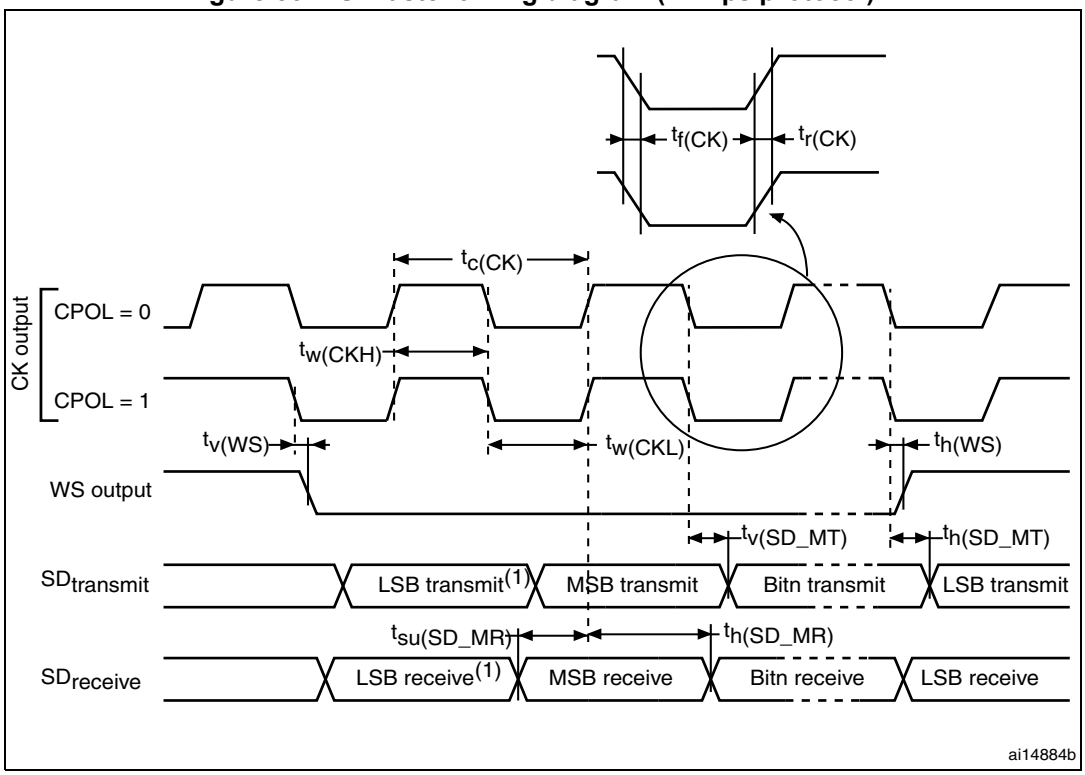
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.18	1.21	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	10	-	-	µs
V_{RERINT_s}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3V ± 10mV	-	3	5	mV

Figure 55. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 56. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SDRAM waveforms and timings

- CL = 30 pF on data and address lines. CL = 10 pF on FMC_SDCLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 3.0 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK= 100 MHz at CL=20 pF (on FMC_SDCLK).
- For 2.7 V≤V_{DD}≤3.6 V, maximum FMC_SDCLK = 90 MHz at CL=30 pF (on FMC_SDCLK).
- For 1.71 V≤V_{DD}<1.9 V, maximum FMC_SDCLK = 70 MHz at CL=10 pF (on FMC_SDCLK).

Figure 73. SDRAM read access waveforms (CL = 1)

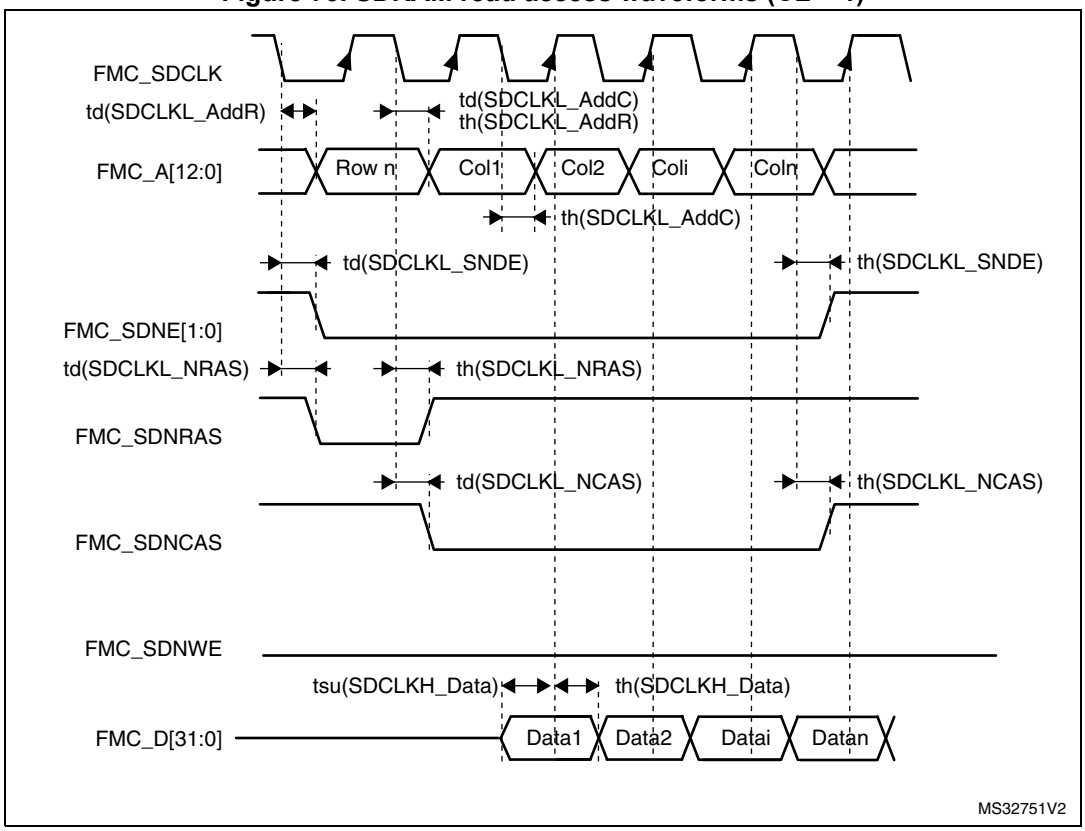


Table 112. Quad-SPI characteristics (continued)in SDR mode(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN)	Data input setup time	-	3	-	-	
th(IN)	Data input hold time		1	-	-	
tv(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	1.5	3	
		1.71 V<V_{DD}<3.6 V	-	1.5	2.5	
th(OUT)	Data output hold time	-	0.5	-	-	

1. Guaranteed by characterization results.

Table 113. Quad-SPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fck1/t(CK)	Quad-SPI clock frequency	2.7 V<V_{DD}<3.6 V CL=20 pF	-	-	80	MHz
		1.8 V<V_{DD}<3.6 V CL=15 pF	-	-	80	
		1.71 V<V_{DD}<3.6 V CL=10 pF	-	-	80	
tw(CKH)	Quad-SPI clock high and low time	-	t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	ns
tw(CKL)			t(CK)/2 - 0.5	-	t(CK)/2 + 0.5	
ts(IN), tsf(IN)	Data input setup time	2.7 V<V_{DD}<3.6 V	1	-	-	
		1.71 V<V_{DD}<2 V	0.5	-	-	
thr(IN), thf(IN)	Data input hold time	2.7 V<V_{DD}<3.6 V	2.25	-	-	
		1.71 V<V_{DD}<2 V	2.75	-	-	
tvr(OUT), tvf(OUT)	Data output valid time	2.7 V<V_{DD}<3.6 V	-	9.5	11.5	
		1.71 V<V_{DD}<3.6 V DHHC=0	-	9.5	12.25	
		DHHC=1 Pres=1, 2...	-	Thclk/2 +2	Thclk/2 +2.5	
thr(OUT), thf(OUT)	Data output hold time	DHHC=0	5.5	-	-	
		DHHC=1 Pres=1, 2...	Thclk/2 +0.75	-	-	

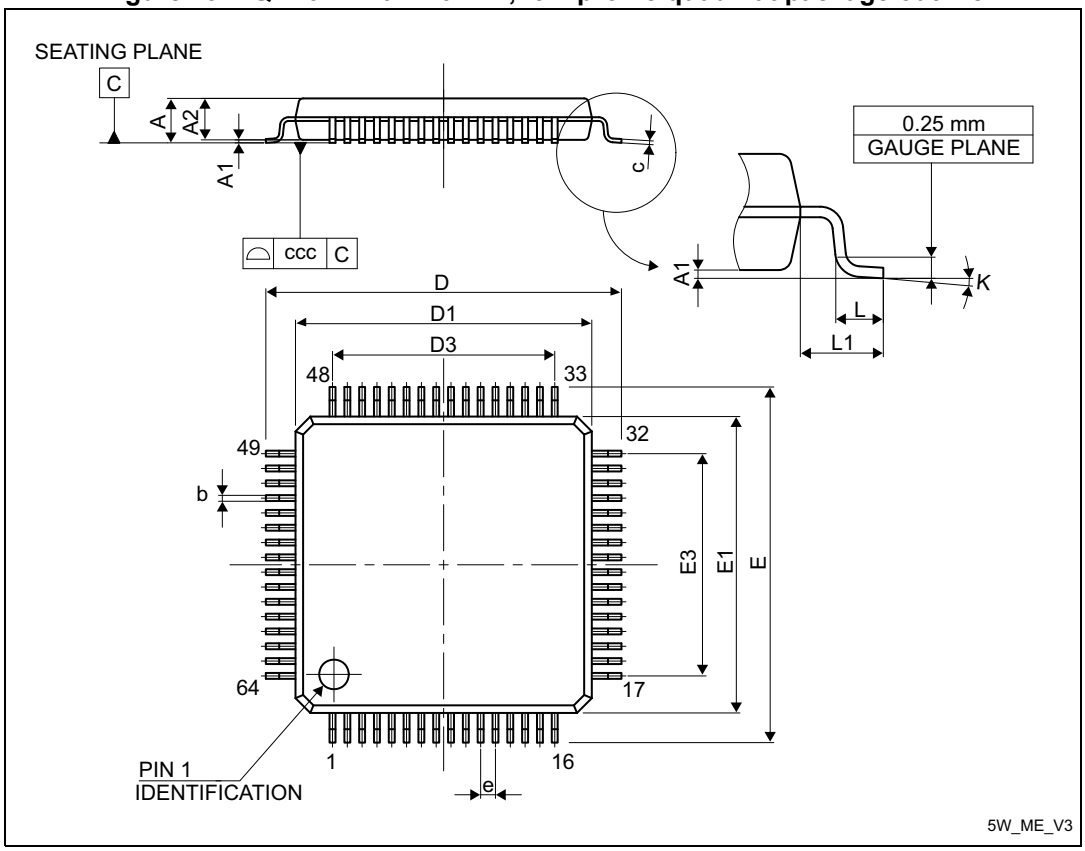
1. Guaranteed by characterization results.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP64 – 10 x 10 mm, low-profile quad flat package information

Figure 79. LQFP64 – 10 x 10 mm, low-profile quad flat package outline



1. Drawing is not to scale.

Table 116. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106

Figure 98. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package recommended footprint

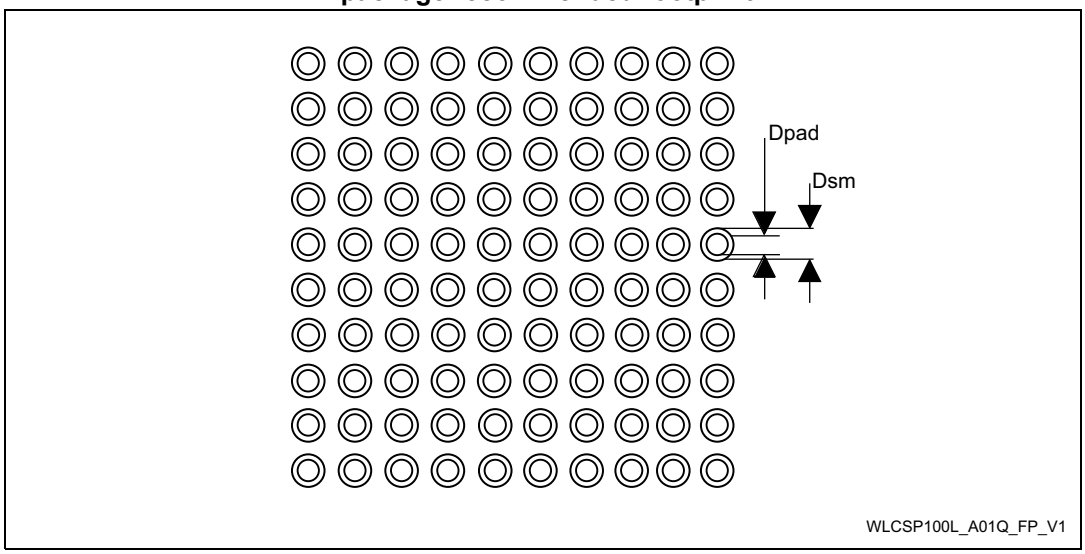


Table 125. WLCSP100 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm