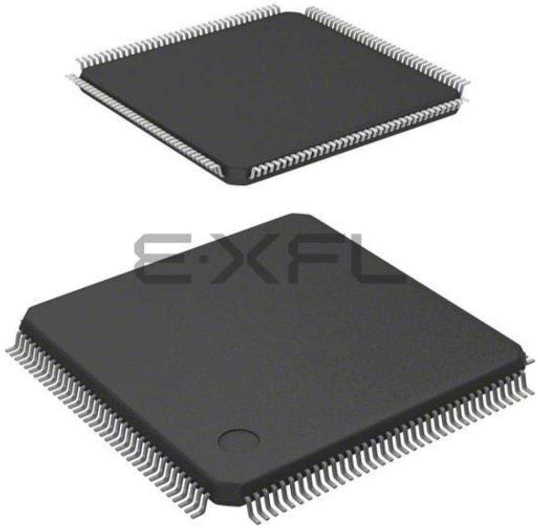

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f722zet6

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1.2 STM32F723xx versus STM32F722xx LQFP144/LQFP176 packages:

Figure 3. Compatible board design for LQFP144 package

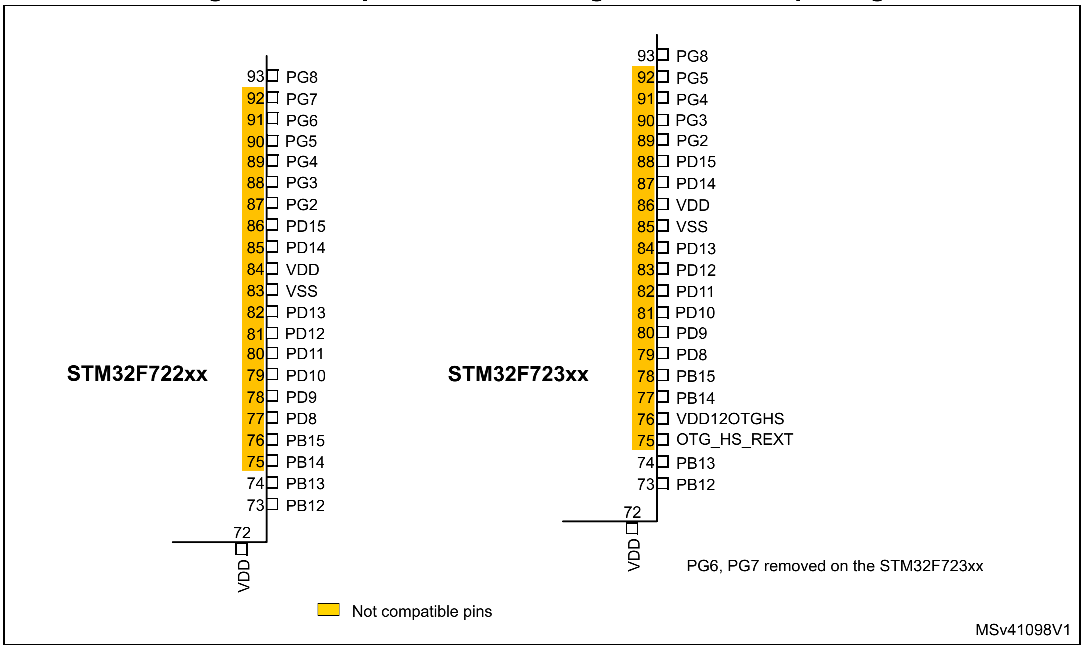
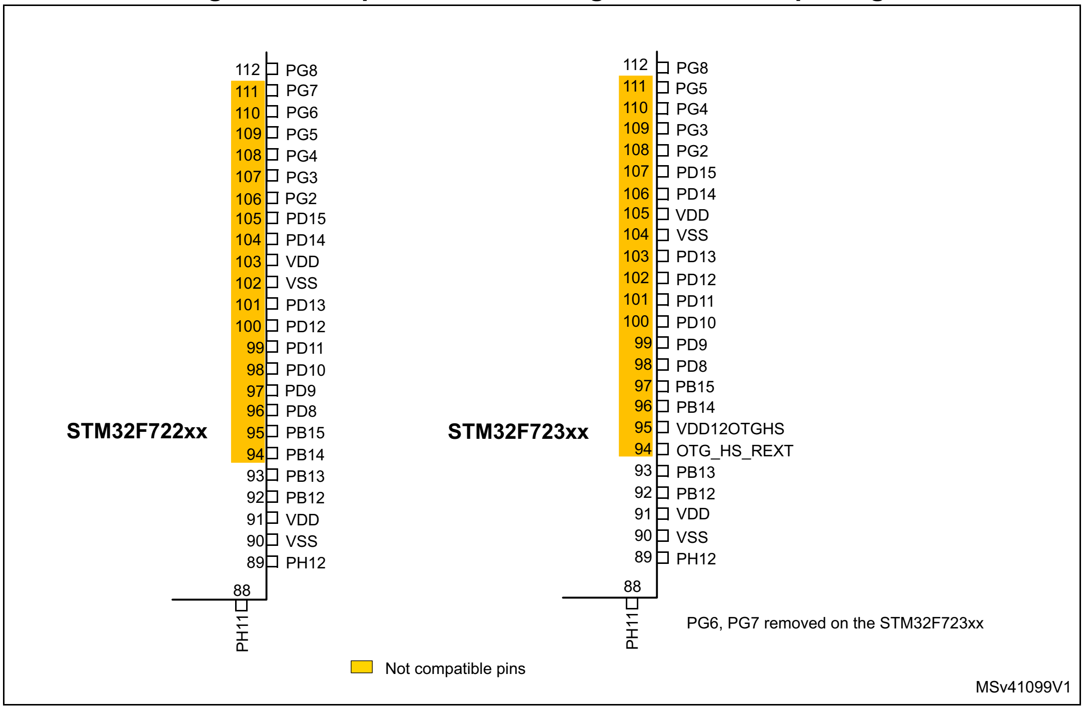


Figure 4. Compatible board design for LQFP176 package



2.20.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

The TIM1 and TIM8 support independent DMA request generation.

2.20.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F722xx and STM32F723xx devices (see *Table 6* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F722xx and STM32F723xx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.20.3 Basic timers TIM6 and TIM7

These timers are mainly used for the DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

The TIM6 and TIM7 support independent DMA request generation.

2.29 Universal serial bus on-the-go full-speed (OTG_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)
- BCD support

For the OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.30 Universal serial bus on-the-go high-speed (OTG_HS)

The device embeds an USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s).

The STM32F722xx devices feature a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The STM32F723xx devices feature an integrated PHY HS.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has a software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- **For the STM32F722xx devices:** External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- **For the STM32F723xx devices:** Internal HS OTG PHY support.

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port B	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	CAN1_TX	SDMMC2_D5	-	SDMMC1_D5	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX	-	-	OTG_HS_ULPI_D3	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	-	USART3_CK	-	-	OTG_HS_ULPI_D5	-	OTG_HS_ID	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	-	USART3_CTS	-	-	OTG_HS_ULPI_D6	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	-	USART3_RTS	-	TIM12_CH1	SDMMC2_D0	-	OTG_HS_DM	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI/I2S2_SD	-	-	-	TIM12_CH2	SDMMC2_D1	-	OTG_HS_DP	EVENTOUT
Port C	PC0	-	-	-	-	-	-	-	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	EVENTOUT
	PC1	TRACED0	-	-	-	-	SPI2_MOSI/I2S2_SD	SAI1_SD_A	-	-	-	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	SPI2_MISO	-	-	-	-	OTG_HS_ULPI_DIR	-	FMC_SDNE0	EVENTOUT
	PC3	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	-	FMC_SDCKE0	EVENTOUT

Table 13. STM32F722xx and STM32F723xx register boundary addresses[(1)] (continued)

Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6800 - 0x4000 6FFF	Reserved
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	Reserved
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	Reserved
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

1. The gray color is used for reserved Flash memory addresses.
2. Only for the STM32F723xx devices.

Table 33. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ[1]			Max[2]			Unit
			T_A = 25 °C			T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
			V_{DD} = 1.7 V	V_{DD}= 2.4 V	V_{DD} = 3.3 V	V_{DD} = 3.3 V			
I_{DD_STBY}	Supply current in Standby mode	Backup SRAM OFF, RTC and LSE OFF	1.09	1.13	1.4	4	27	55	µA
		Backup SRAM ON, RTC and LSE OFF	1.85	1.88	2.17	5	30	60	
		Backup SRAM OFF, RTC ON and LSE in low drive mode	1.65	1.86	2.43	7	47	95.5	
		Backup SRAM OFF, RTC ON and LSE in medium low drive mode	1.67	1.88	2.46	7	47.5	97	
		Backup SRAM OFF, RTC ON and LSE in medium high drive mode	1.8	2.01	2.61	7.5	50.5	102.5	
		Backup SRAM OFF, RTC ON and LSE in high drive mode	1.92	2.13	2.73	8	53	107	
		Backup SRAM ON, RTC ON and LSE in low drive mode	2.39	2.6	3.23	9	62	127	
		Backup SRAM ON, RTC ON and LSE in Medium low drive mode	2.41	2.64	3.25	9	63	128	
		Backup SRAM ON, RTC ON and LSE in Medium high drive mode	2.67	2.89	2.53	10	68	139	
		Backup SRAM ON, RTC ON and LSE in High drive mode	2.68	2.9	3.51	10	68	138	

1. PDR is OFF for V_{DD}=1.7V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA.
2. Guaranteed by characterization results.

Figure 31. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in low drive mode)

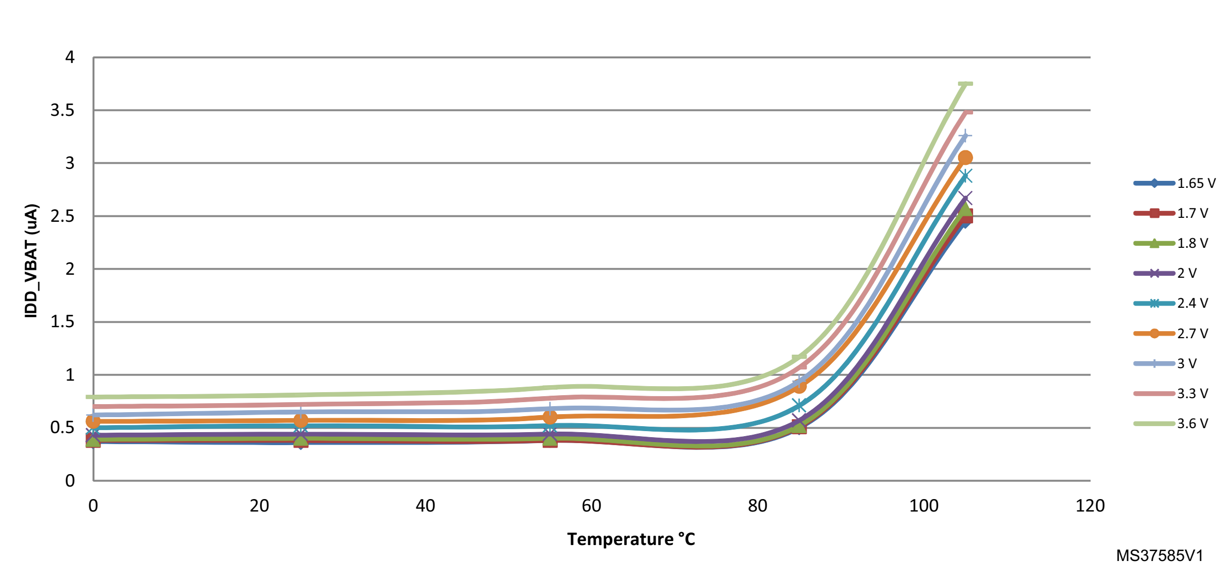


Figure 32. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium low drive mode)

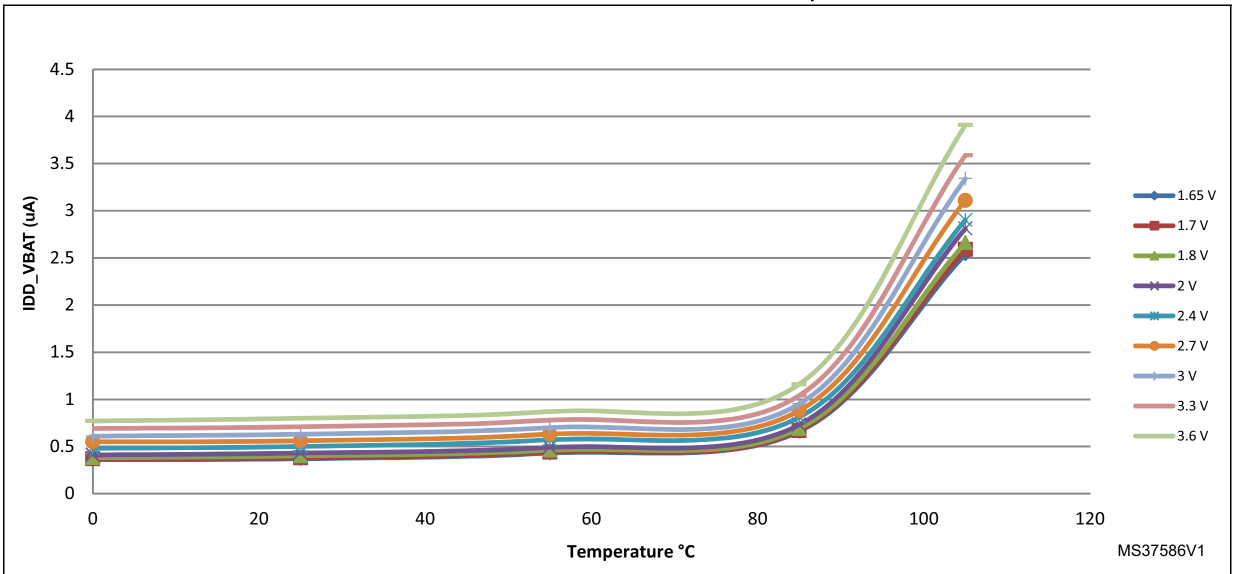


Figure 33. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in medium high drive mode)

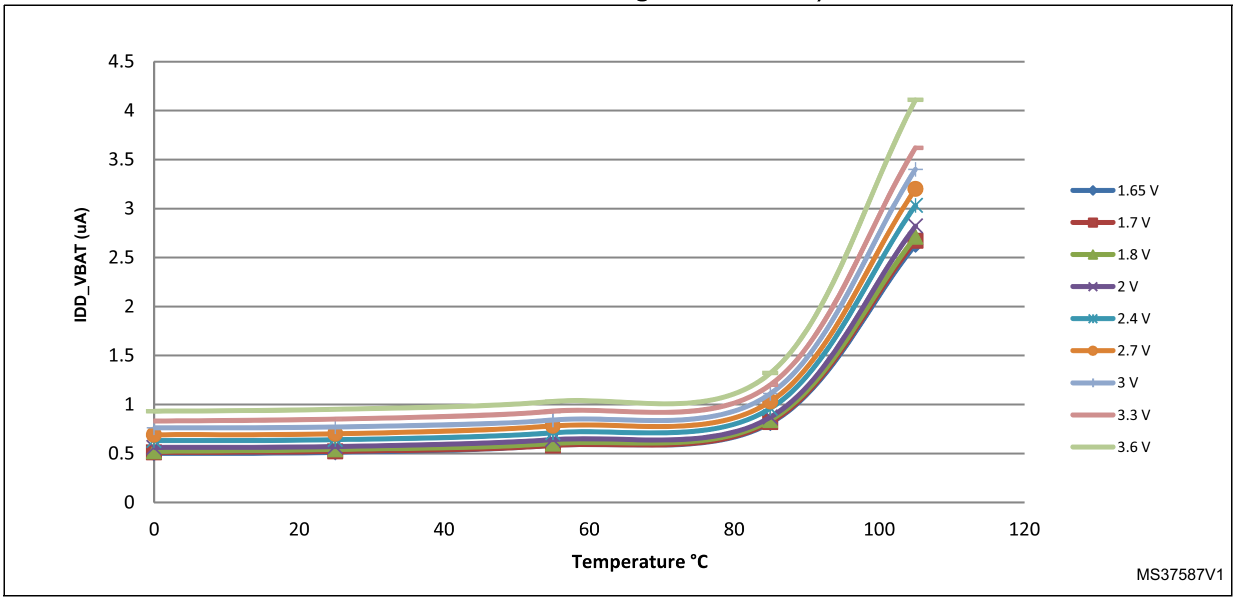
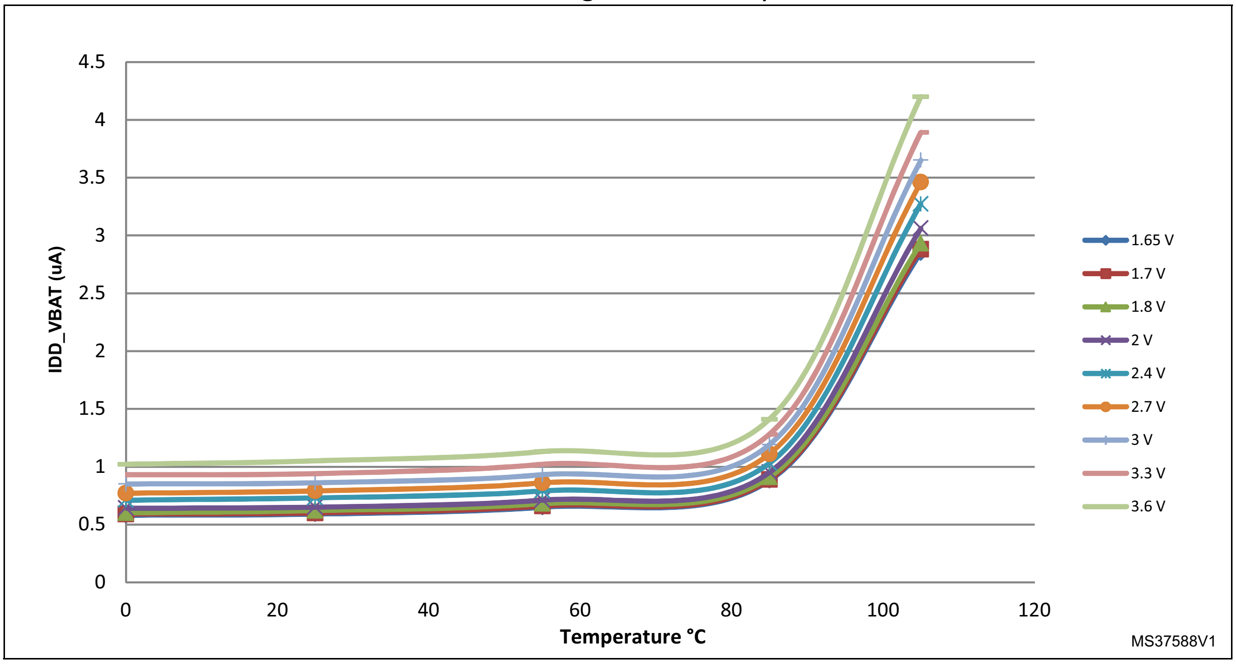


Figure 34. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high drive mode)



USB OTG HS and USB OTG HS PHY current consumption (on STM32F723xx devices)

The MCU is placed under the following conditions:

- STM32 MCU is enumerated as a HID device.
- f_{HCLK} = 216 MHz (Scale 1 + over-drive ON), f_{HCLK} = 168 MHz (Scale 2), f_{HCLK} = 144 MHz (Scale 3)
  The given value is calculated by measuring the difference of current consumption in case:
  - USB is configured but no transfer is done.
  - USB is configured and there is a transmission on going.
- Ambient operating temperature is 25 °C, V_{DD} = V_{DDUSB} = 3.3 V.

Table 37. USB OTG HS and USB OTG PHY HS current consumption

	I_{DD} (Typ)			Unit
	Scale 1	Scale 2	Scale 3	
USB OTG HS and USB OTG HS PHY current consumption	50.16	44.92	38.98	mA

5.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 38* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 38. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep	-	13	13	CPU clock cycles
t_{WUSTOP}(2)	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	14	14.9	µs
		Main regulator is ON and Flash memory in Deep power down mode	104.1	107.6	
		Low power regulator is ON	21.4	24.2	
		Low power regulator is ON and Flash memory in Deep power down mode	111.5	116.5	

5.3.10 Internal clock source characteristics

The parameters given in *Table 43* and *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

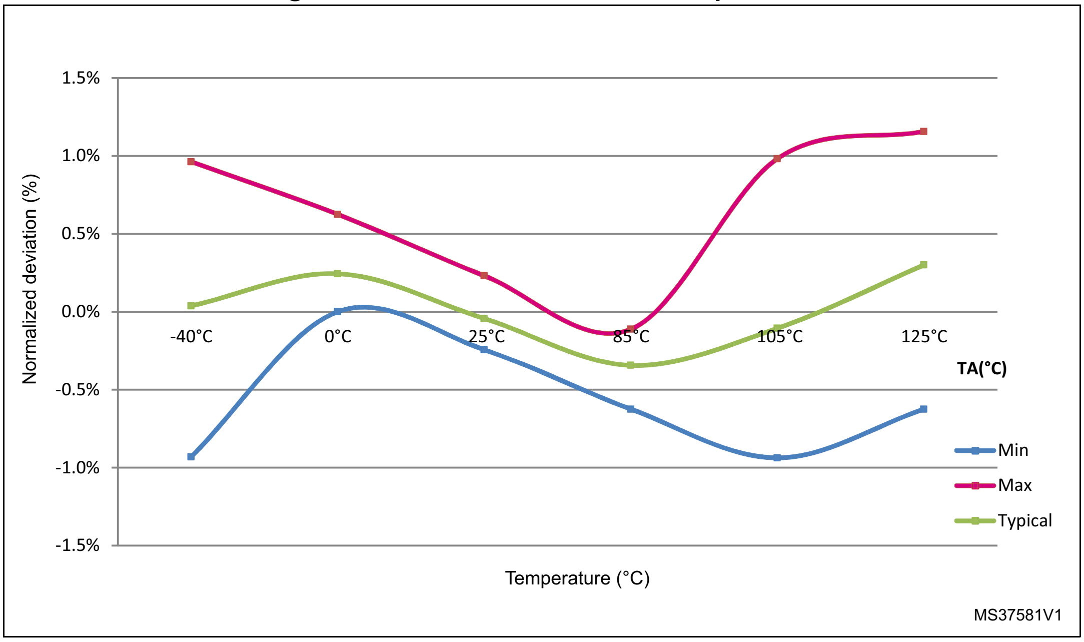
High-speed internal (HSI) RC oscillator

Table 43. HSI oscillator characteristics [(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step[(2)]	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C[(3)]	− 8	-	4.5	%
		T_A = –10 to 85 °C[(3)]	− 4	-	4	%
		T_A = 25 °C[(4)]	− 1	-	1	%
$t_{su(HSI)}$[(2)]	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$[(2)]	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 40. HSI deviation versus temperature



1. Guaranteed by characterization results.

Table 47. PLLISAI characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(PLLSAI)}$(4)	PLLSAI power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLSAI)}$(4)	PLLSAI power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	mA

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.
2. Guaranteed by design.
3. Value given with main PLL running.
4. Guaranteed by characterization results.

5.3.12 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see *Table 58: EMI characteristics*). It is available only on the main PLL.

Table 48. SSCG parameters constraint

Symbol	Parameter	Min	Typ	Max(1)	Unit
f_{Mod}	Modulation frequency	-	-	10	KHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	-	-	-	$2^{15} - 1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = round[f_{PLL\_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If f_{PLL_IN} = 1 MHz, and f_{MOD} = 1 kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = round[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = round[((2^{15} - 1) \times md \times PLLN) / (100 \times 5 \times MODEPER)]$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = ±2 % (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = round[((2^{15} - 1) \times 2 \times 240) / (100 \times 5 \times 250)] = 126md(quantitazed)\%$$

2. PB14 and PB15 in the STM32F723xx devices.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

5.3.20 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 62: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 17*. All I/Os are CMOS and TTL compliant.

Table 62. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}-0.04^{(1)}$	V
					$0.3V_{DD}^{(2)}$	
	BOOT I/O input low level voltage	1.75 V≤V_{DD}≤3.6 V, –40 °C≤T_A≤105 °C	-	-	$0.1V_{DD}+0.1^{(1)}$	
		1.7 V≤V_{DD}≤3.6 V, 0 °C≤T_A≤105 °C	-	-		
V_{IH}	FT, TTa and NRST I/O input high level voltage(5)	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$	-	-	V
			$0.7V_{DD}^{(2)}$			
	BOOT I/O input high level voltage	1.75 V≤V_{DD}≤3.6 V, –40 °C≤T_A≤105 °C	$0.17V_{DD}+0.7^{(1)}$	-	-	
		1.7 V≤V_{DD}≤3.6 V, 0 °C≤T_A≤105 °C				
V_{HYS}	FT, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	$10\%V_{DD}^{(3)}$	-	-	V
	BOOT I/O input hysteresis	1.75 V≤V_{DD}≤3.6 V, –40 °C≤T_A≤105 °C	0.1	-	-	
		1.7 V≤V_{DD}≤3.6 V, 0 °C≤T_A≤105 °C				
I_{lkg}	I/O input leakage current (4)	V_{SS}≤V_{IN}≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)	V_{IN} = 5 V	-	-	3	

Table 63. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	CMOS port(2) I_{IO} = -8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OH} (3)	Output high level voltage for PC14	CMOS port(2) I_{IO} = -2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	TTL port(2) I_{IO} =-8mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3(4)	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 1.3(4)	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	-	0.4(4)	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -6 mA 1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD} − 0.4(4)	-	
V_{OL} (1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	-	0.4(5)	V
V_{OH} (3)	Output high level voltage for an I/O pin except PC14	I_{IO} = -4 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD} − 0.4(5)	-	
V_{OH} (3)	Output high level voltage for PC14	I_{IO} = -1 mA 1.7 V ≤ V_{DD} ≤ 3.6V	V_{DD} − 0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data.
5. Guaranteed by design.

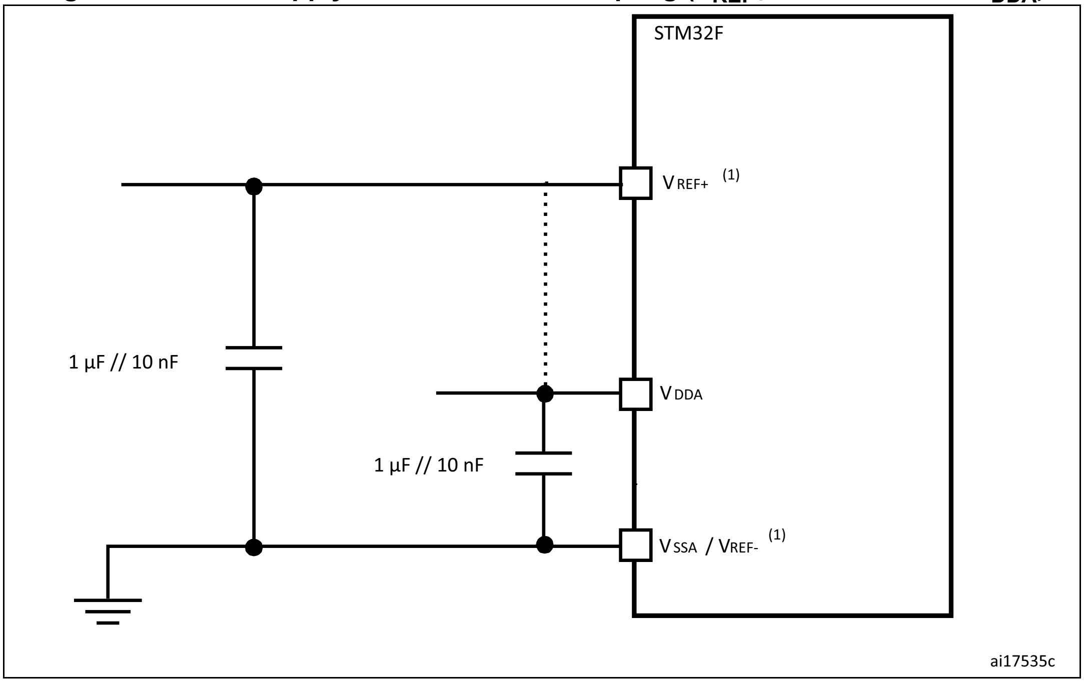
Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 45* and *Table 64*, respectively.

General PCB design guidelines

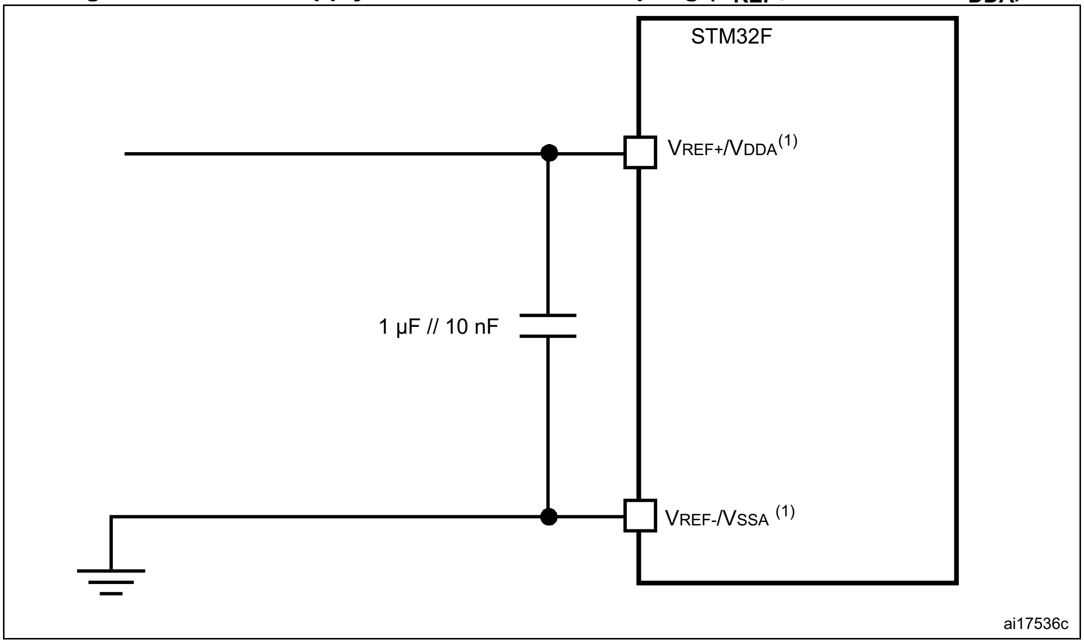
Power supply decoupling should be performed as shown in *Figure 49* or *Figure 50*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 49. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all the packages except LQFP64, whereas the V_{REF-} is available only on UFBGA176 and UFBGA144. When V_{REF-} is not available, it is internally connected to V_{SSA}.

Figure 50. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all the packages except LQFP64, whereas the V_{REF-} is available only on UFBGA176 and UFBGA144. When V_{REF-} is not available, it is internally connected to V_{SSA}.

Figure 57. SAI master timing waveforms

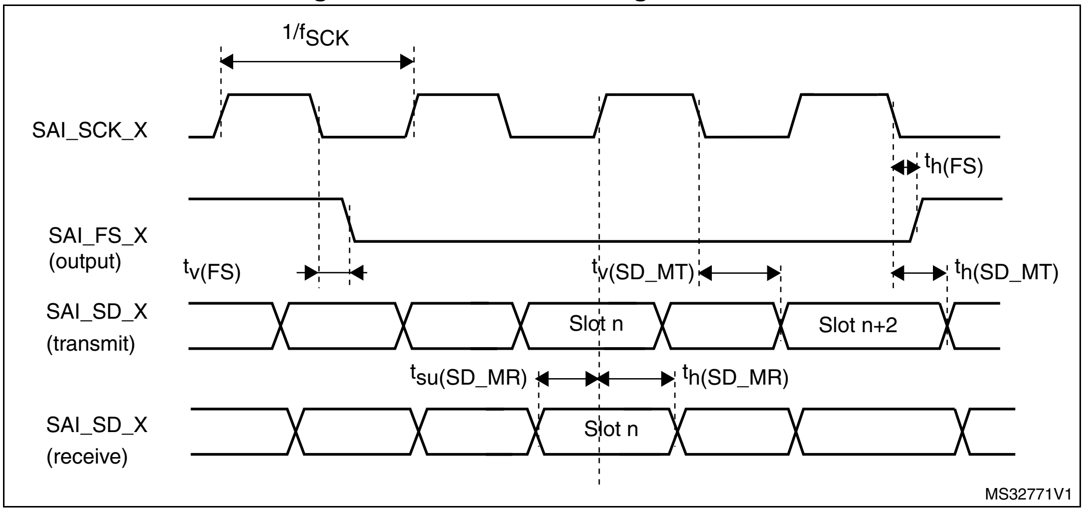


Figure 58. SAI slave timing waveforms

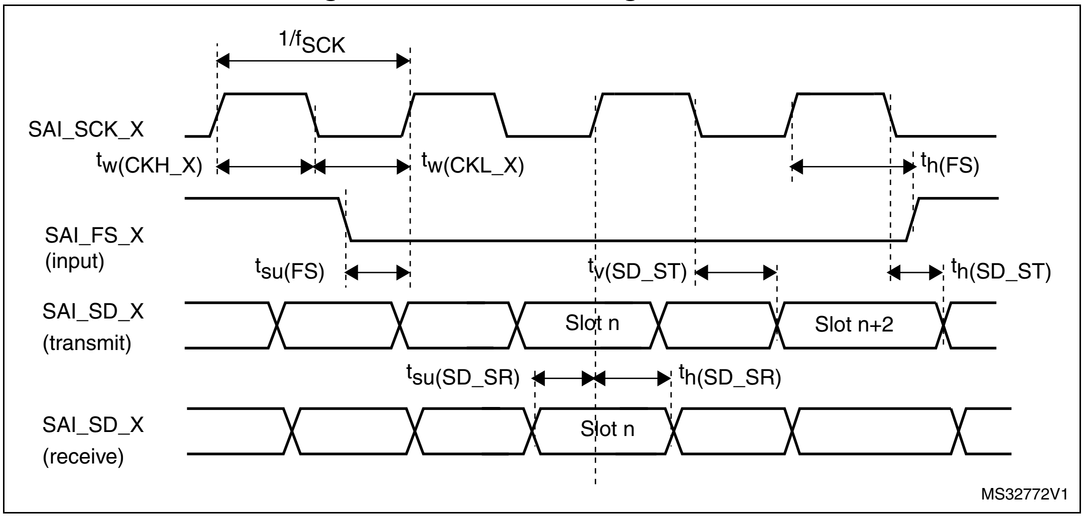


Figure 72. NAND controller waveforms for common memory write access

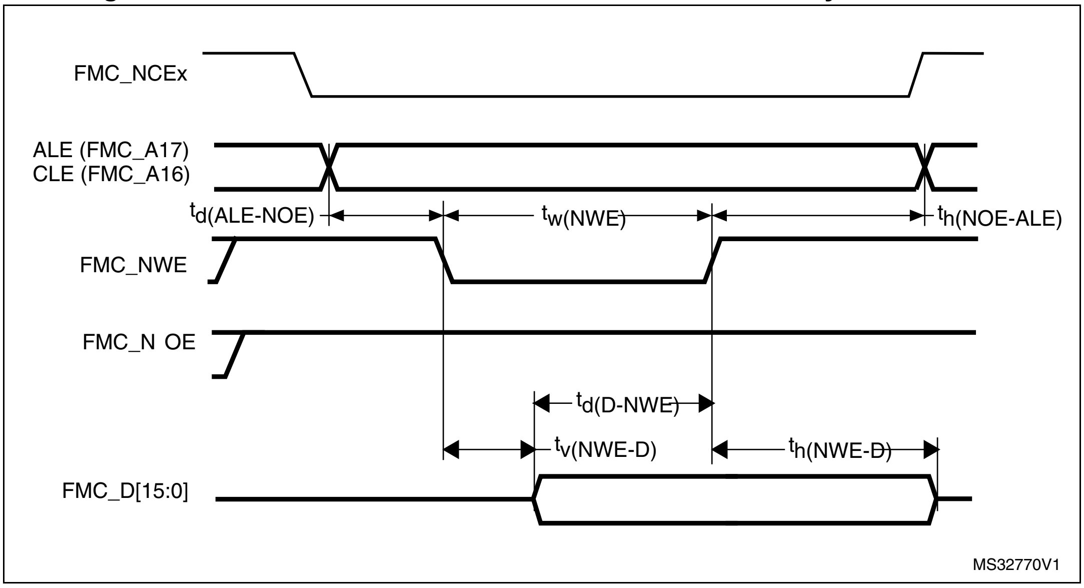


Table 106. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	4Thclk -0.5	4Thclk +0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	11	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	3Thclk +1.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	4Thclk - 2	-	

1. Guaranteed by characterization results.

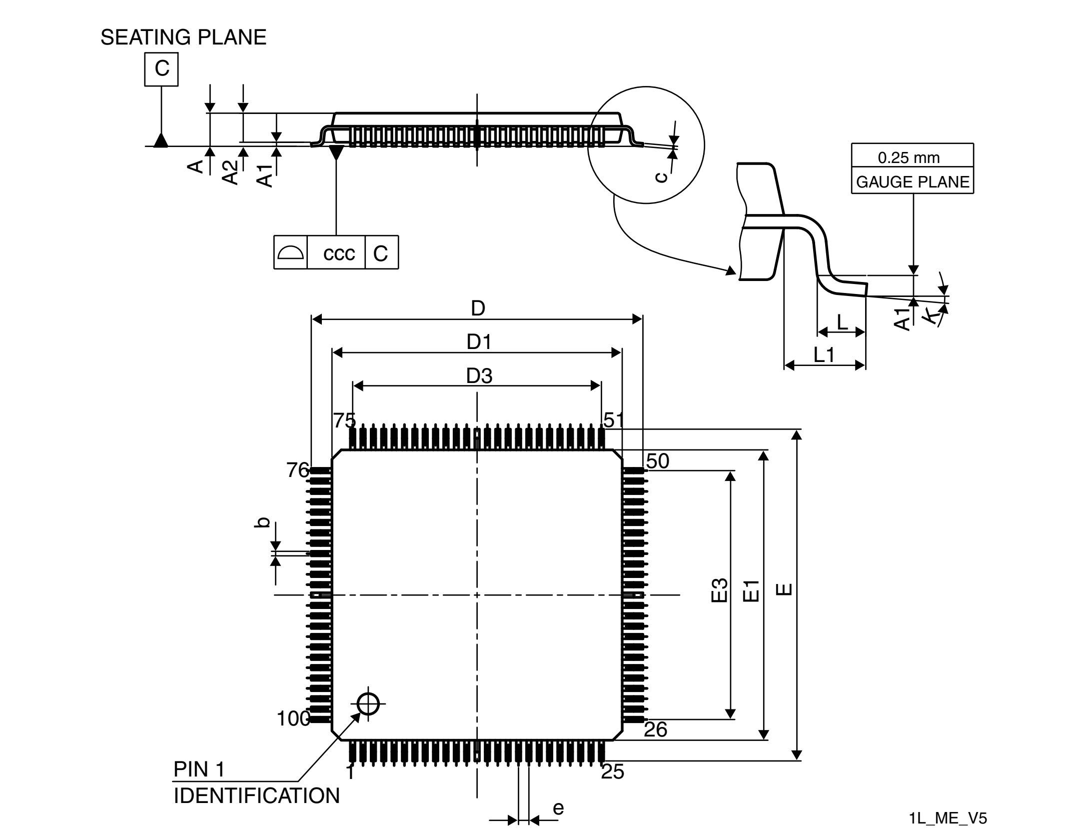
Table 107. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	4Thclk -0.5	4Thclk +0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	2Thclk - 1	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	5Thclk - 1	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	3Thclk +1.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	2Thclk - 2	-	

1. Guaranteed by characterization results.

6.2 LQFP100, 14 x 14 mm low-profile quad flat package information

Figure 82. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



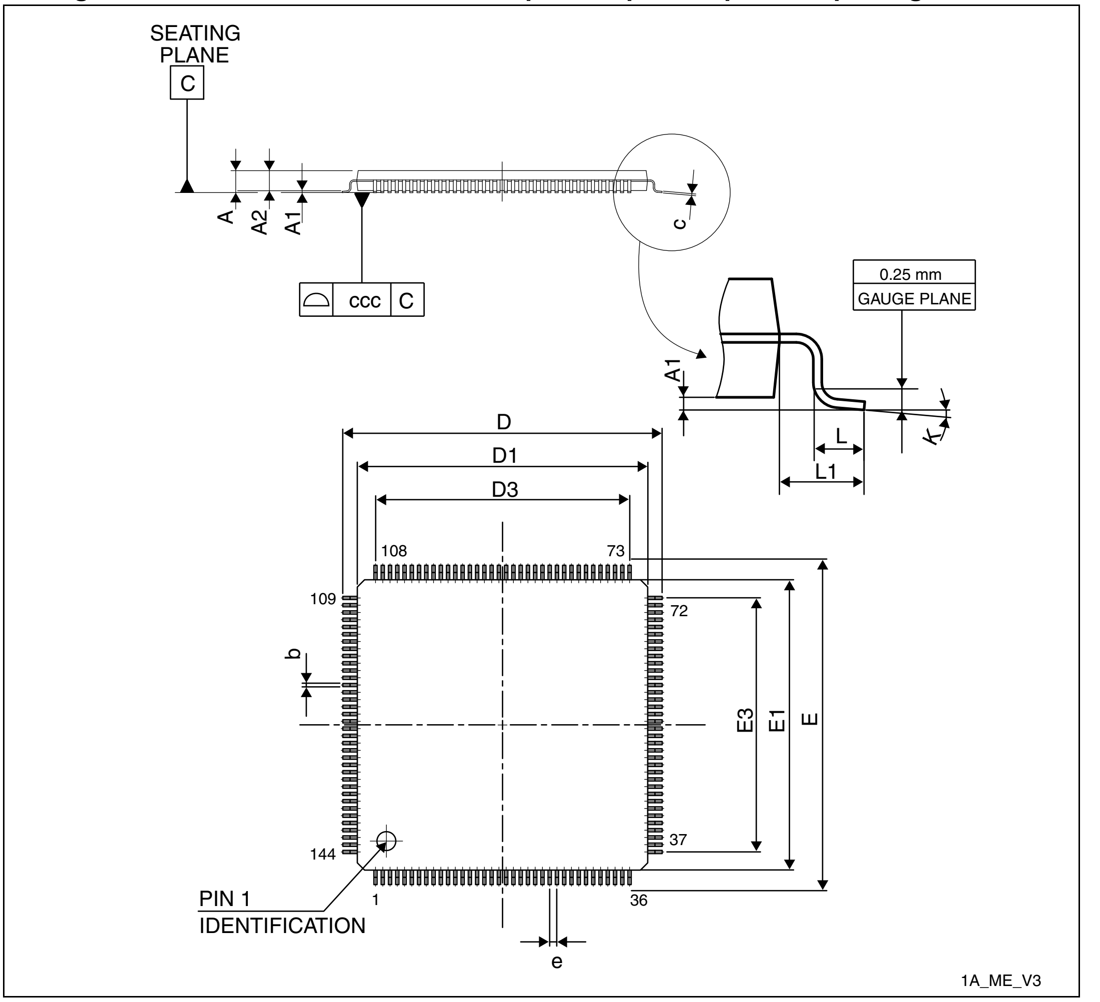
1. Drawing is not to scale.

Table 117. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

6.3 LQFP144, 20 x 20 mm low-profile quad flat package information

Figure 85. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 118. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874

Table 120. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 92. UFBGA144 - 144-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

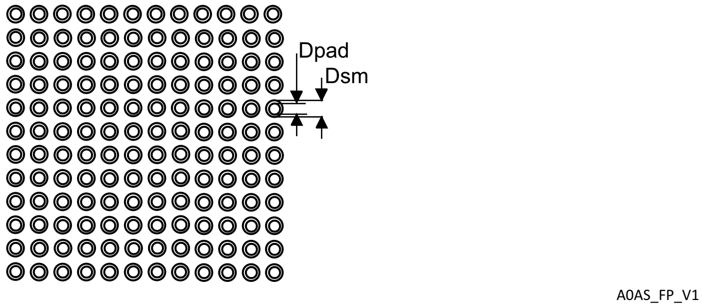


Table 121. UFBGA144 recommended PCB design rules (0.50 mm pitch BGA)

Dimension	Recommended values
Pitch	0.50 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm