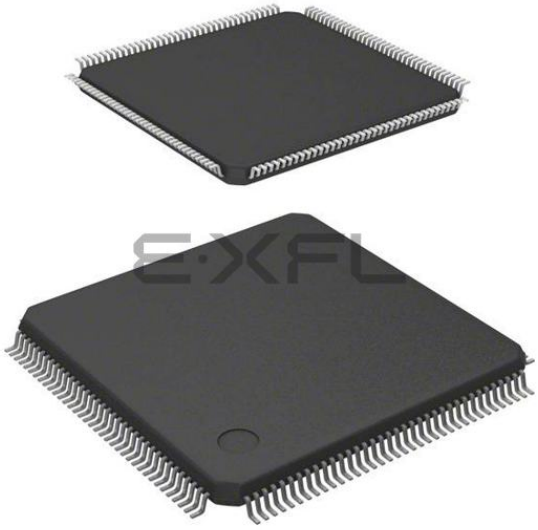
# STMicroelectronics - STM32F722ZET6U Datasheet



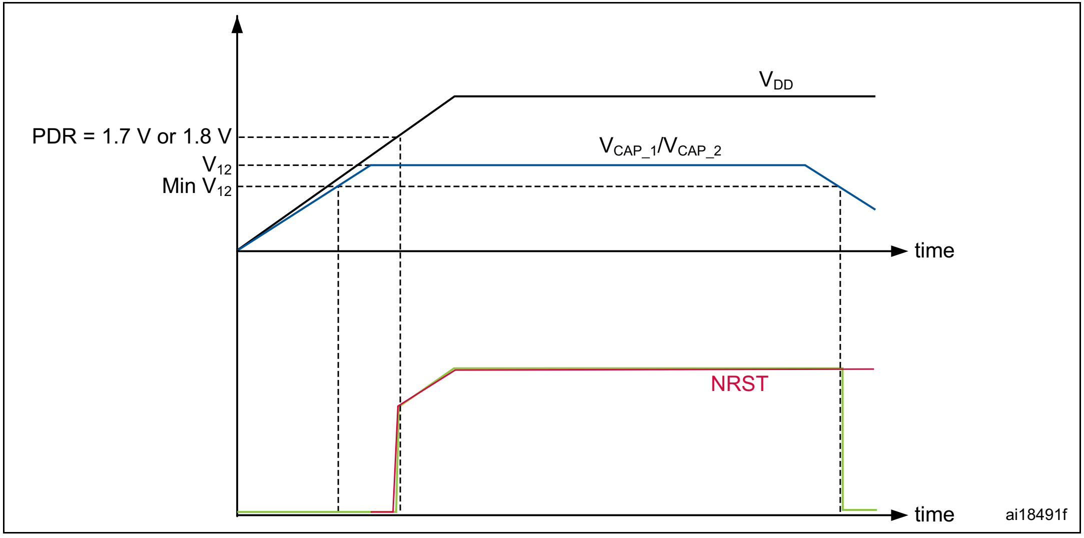
| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f722zet6u |

### Table 2. STM32F722xx and STM32F723xx features and peripheral counts (continued)

| Peripherals | STM32F72xRx | STM32F72xVx | STM32F72xZx | STM32F72xIx |
|---|---|---|---|---|
| Operating voltage | 1.7 to 3.6 V(8) | | | |
| Operating temperatures | Ambient temperatures: –40 to +85 °C /–40 to +105 °C | | | |
| | Junction temperature: –40 to + 125 °C | | | |
| Package | LQFP64(9) | LQFP100(9)<br>WLCSP100(10) | LQFP144<br>UFBGA144(10) | UFBGA176<br>LQFP176 |

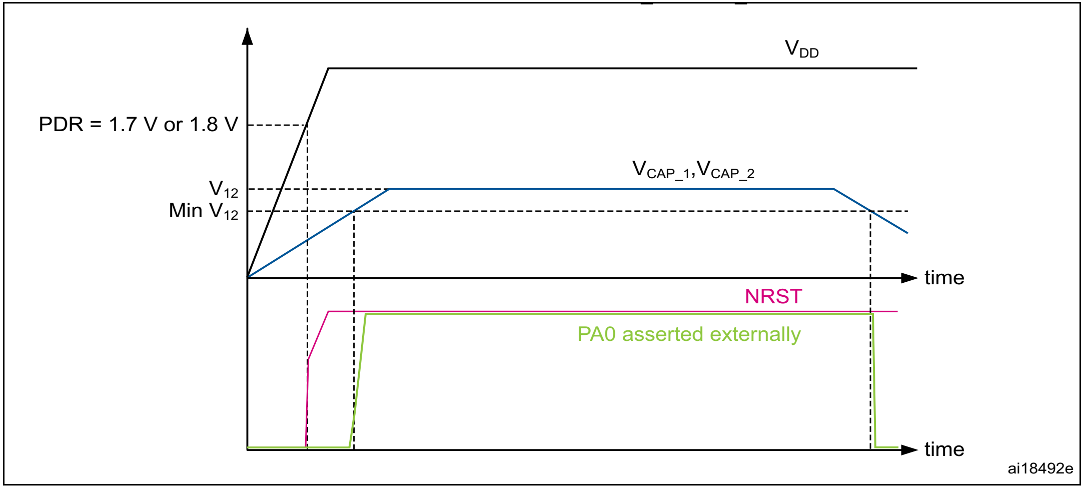
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. On the STM32F723xx device packages, except the 176-pin ones, the TIM12 is not available, so there are 9 general-purpose timers.
3. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the $I^2S$ audio mode.
4. USB OTG HS with the ULPI on the STM32F722xx devices and with integrated HS PHY on the STM32F723xx devices.
5. The SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
6. The SDMMC2 is not available on the STM32F723Vx devices.
7. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
8. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.15.2: Internal reset OFF*).
9. Available only on the STM32F722xx devices.
10. Available only on the STM32F723xx devices.

### Figure 12. Startup in regulator OFF: slow $V_{DD}$ slope - power-down reset risen after $V_{CAP\_1}/V_{CAP\_2}$ stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

### Figure 13. Startup in regulator OFF mode: fast $V_{DD}$ slope - power-down reset risen before $V_{CAP\_1}/V_{CAP\_2}$ stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

All the RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

## 2.18 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  - Normal mode (default mode when MR or LPR is enabled)
  - Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup and the LPTIM1 asynchronous interrupt).

**Table 5. Voltage regulator modes in stop mode**

| Voltage regulator configuration | Main regulator (MR) | Low-power regulator (LPR) |
|---|---|---|
| Normal mode | MR ON | LPR ON |
| Under-drive mode | MR in under-drive mode | LPR in under-drive mode |

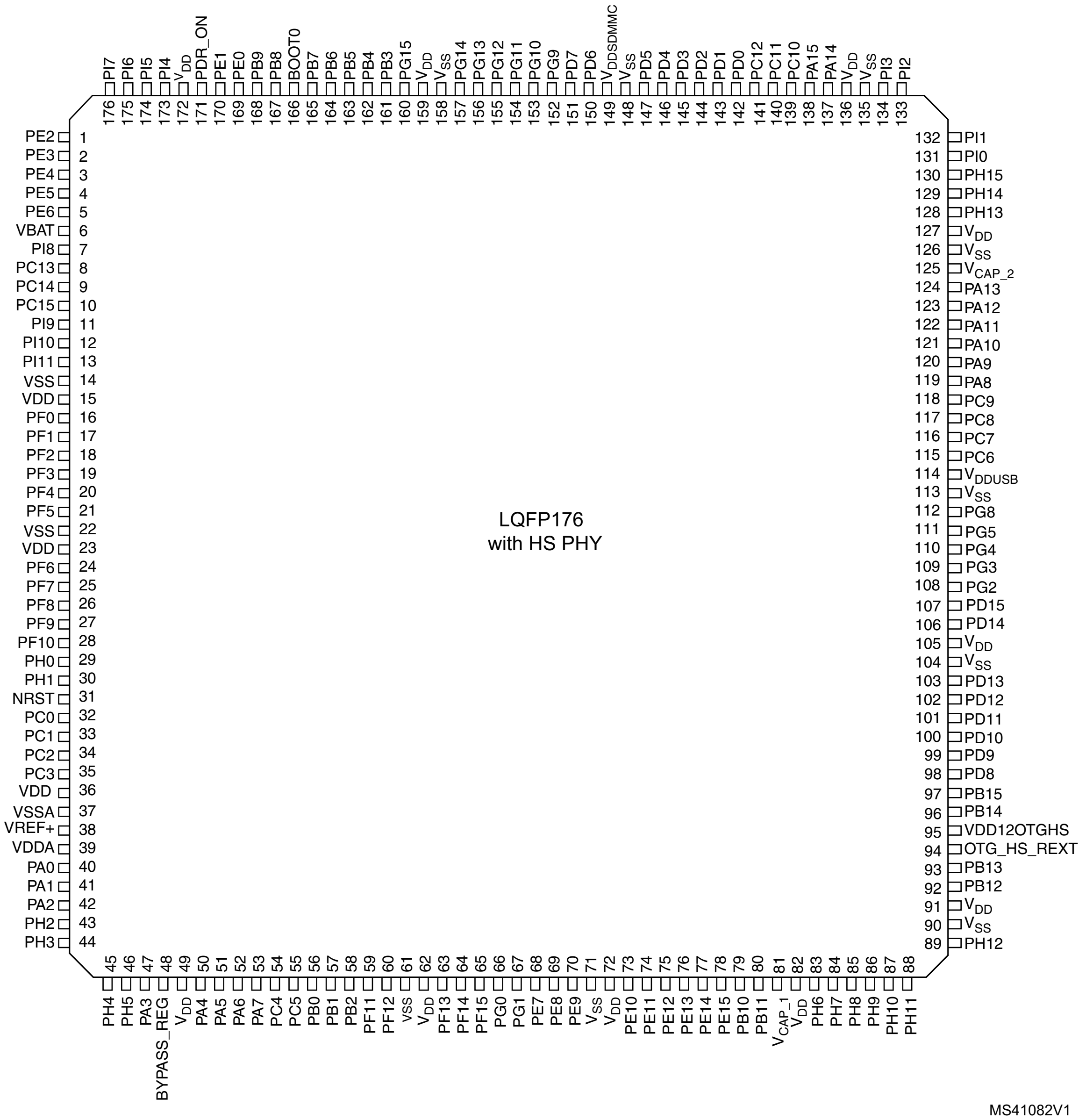
- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

  The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

### Figure 21. STM32F723xx LQFP176 pinout



1. The above figure shows the package top view.

### Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F722xx | | | | | STM32F723xx | | | | | | | | | | |
| LQFP64 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | WLCSP100 | UFBGA176 | UFBGA144 | LQFP144 | LQFP176 | | | | | | |
| 35 | 53 | 75 | R14 | 94 | - | - | - | - | - | PB14 | I/O | FT | - | TIM1_CH2N, TIM8_CH2N, SPI2_MISO, USART3_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT | - |
| - | - | - | - | - | J1 | R14 | L11 | 77 | 96 | PB14 | I/O | FT | - | OTG_HS_DM | - |
| 36 | 54 | 76 | R15 | 95 | - | - | - | - | - | PB15 | I/O | FT | - | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT | - |
| - | - | - | - | - | H1 | R15 | L12 | 78 | 97 | PB15 | I/O | FT | - | OTG_HS_DP | - |
| - | 55 | 77 | P15 | 96 | - | P15 | L9 | 79 | 98 | PD8 | I/O | FT | - | USART3_TX, FMC_D13, EVENTOUT | - |
| - | 56 | 78 | P14 | 97 | - | P14 | K9 | 80 | 99 | PD9 | I/O | FT | - | USART3_RX, FMC_D14, EVENTOUT | - |
| - | 57 | 79 | N15 | 98 | - | N15 | J9 | 81 | 100 | PD10 | I/O | FT | - | USART3_CK, FMC_D15, EVENTOUT | - |

### Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F722xx | | | | | STM32F723xx | | | | | | | | | | |
| LQFP64 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | WLCSP100 | UFBGA176 | UFBGA144 | LQFP144 | LQFP176 | | | | | | |
| - | 58 | 80 | N14 | 99 | F3 | N14 | H9 | 82 | 101 | PD11 | I/O | FT | - | USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT | - |
| - | 59 | 81 | N13 | 100 | F2 | N13 | L10 | 83 | 102 | PD12 | I/O | FT | - | TIM4_CH1, LPTIM1_IN1, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT | - |
| - | 60 | 82 | M15 | 101 | E3 | M15 | K10 | 84 | 103 | PD13 | I/O | FT | - | TIM4_CH2, LPTIM1_OUT, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT | - |
| - | - | 83 | - | 102 | - | - | G8 | 85 | 104 | VSS | S | - | - | - | - |
| - | - | 84 | J13 | 103 | - | J13 | F8 | 86 | 105 | VDD | S | - | - | - | - |
| - | 61 | 85 | M14 | 104 | F1 | M14 | K11 | 87 | 106 | PD14 | I/O | FT | - | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT | - |
| - | 62 | 86 | L14 | 105 | E2 | L14 | K12 | 88 | 107 | PD15 | I/O | FT | - | TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT | - |
| - | - | 87 | L15 | 106 | - | L15 | J12 | 89 | 108 | PG2 | I/O | FT | - | FMC_A12, EVENTOUT | - |
| - | - | 88 | K15 | 107 | - | K15 | J11 | 90 | 109 | PG3 | I/O | FT | - | FMC_A13, EVENTOUT | - |

### Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset)(1) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F722xx | | | | | STM32F723xx | | | | | | | | | | |
| LQFP64 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | WLCSP100 | UFBGA176 | UFBGA144 | LQFP144 | LQFP176 | | | | | | |
| 39 | 65 | 98 | G14 | 117 | D2 | G14 | F11 | 98 | 117 | PC8 | I/O | FT | - | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, SDMMC1_D0, EVENTOUT | - |
| 40 | 66 | 99 | F14 | 118 | D1 | F14 | E11 | 99 | 118 | PC9 | I/O | FTf | - | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, EVENTOUT | - |
| 41 | 67 | 100 | F15 | 119 | D3 | F15 | E12 | 100 | 119 | PA8 | I/O | FTf | - | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, EVENTOUT | - |
| 42 | 68 | 101 | E15 | 120 | C3 | E15 | D12 | 101 | 120 | PA9 | I/O | FT | - | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT | OTG_FS_VBUS |
| 43 | 69 | 102 | D15 | 121 | C2 | D15 | D11 | 102 | 121 | PA10 | I/O | FT | - | TIM1_CH3, USART1_RX, OTG_FS_ID, EVENTOUT | - |
| 44 | 70 | 103 | C15 | 122 | C1 | C15 | C12 | 103 | 122 | PA11 | I/O | FT | - | TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT | - |
| 45 | 71 | 104 | B15 | 123 | B2 | B15 | B12 | 104 | 123 | PA12 | I/O | FT | - | TIM1_ETR, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, EVENTOUT | - |
| 46 | 72 | 105 | A15 | 124 | B1 | A15 | A12 | 105 | 124 | PA13(JTMS-SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |

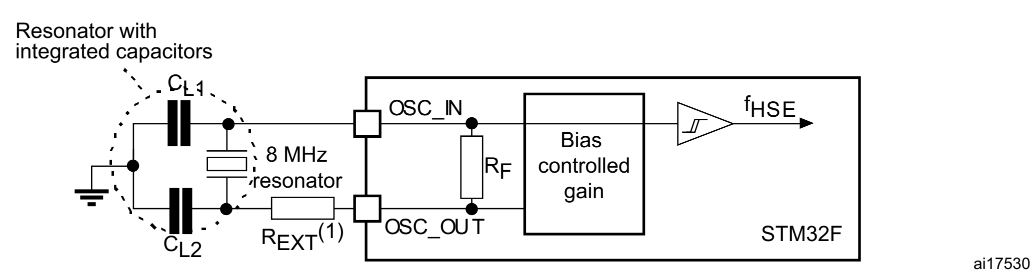
### Table 13. STM32F722xx and STM32F723xx register boundary addresses[1] (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4008 0000- 0x4FFF FFFF | Reserved |
| AHB1 | 0x4004 0000 - 0x4007 FFFF | USB OTG HS |
| | 0x4002 6800- 0x4003 FFFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 5000 - 0X4002 5FFF | Reserved |
| | 0x4002 4000 - 0x4002 4FFF | BKPSRAM |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0X4002 3400 - 0X4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0X4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 38*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

**Figure 38. Typical application with an 8 MHz crystal**



1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 42*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 42. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00<br>Low drive capability | - | 250 | - | nA |
| | | LSEDRV[1:0]=10<br>Medium low drive capability | - | 300 | - | |
| | | LSEDRV[1:0]=01<br>Medium high drive capability | - | 370 | - | |
| | | LSEDRV[1:0]=11<br>High drive capability | - | 480 | - | |

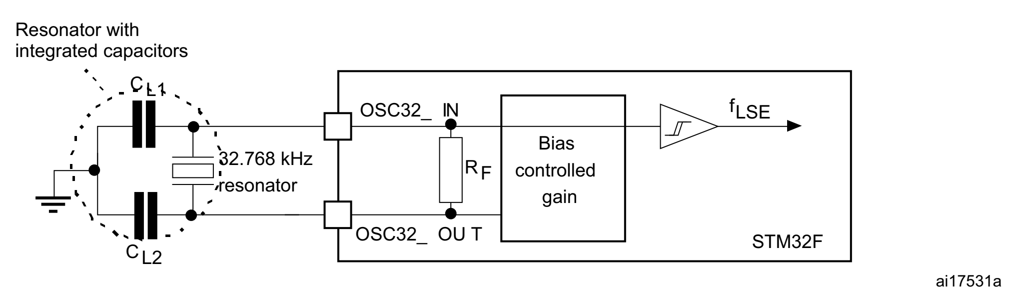
**Table 42. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_m$_crit_max | Maximum critical crystal $g_m$ | LSEDRV[1:0]=00<br>Low drive capability | - | - | 0.48 | µA/V |
| | | LSEDRV[1:0]=10<br>Medium low drive capability | - | - | 0.75 | |
| | | LSEDRV[1:0]=01<br>Medium high drive capability | - | - | 1.7 | |
| | | LSEDRV[1:0]=11<br>High drive capability | - | - | 2.7 | |
| $t_{SU}$(2) | start-up time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST Microelectronics website www.st.com.*

**Figure 39. Typical application with a 32.768 kHz crystal**



## 5.3.15 USB HS PHY external resistor characteristics (on STM32F723xx devices)

**Table 52. USB HS PHY external resistor characteristics (on STM32F723xx devices)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| REXT | External calibration resistor connected (to GND) from OTG_HS_REXT | Required if using USB HS PHY | 2.97 | 3.00 | 3.03 | kΩ |

## 5.3.16 Memory characteristics

### Flash memory

The characteristics are given at TA = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 53. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode, $V_{DD}$ = 1.7 V | - | 6.7 | - | mA |
| | | Write / Erase 16-bit mode, $V_{DD}$ = 2.1 V | - | 9.2 | - | |
| | | Write / Erase 32-bit mode, $V_{DD}$ = 3.3 V | - | 12.6 | - | |

**Table 54. Flash memory programming**

| Symbol | Parameter | Conditions | Min[(1)] | Typ | Max[(1)] | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word programming time | Program/erase parallelism (PSIZE) = x 8/16/32 | - | 16 | 100[(2)] | µs |
| $t_{ERASE16KB}$ | Sector (16 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 346 | 418 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 252 | 312 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 208 | 265 | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1953 | 2500 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 1252 | 1639 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 927 | 1322 | |
| $t_{ERASE64KB}$ | Sector (64 KB) erase time | Program/erase parallelism (PSIZE) = x 8 | - | 1027 | 1298 | ms |
| | | Program/erase parallelism (PSIZE) = x 16 | - | 675 | 840 | |
| | | Program/erase parallelism (PSIZE) = x 32 | - | 505 | 682 | |

- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 58. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{CPU}$] | Unit |
|---|---|---|---|---|---|
| | | | | 25/200 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, LQFP176 package, conforming to IEC61967-2 ART/L1-cache OFF, over-drive ON, all peripheral clocks enabled, clock dithering disabled. | 0.1 MHz to 30 MHz | 23 | dBµV |
| | | | 30 MHz to 130 MHz | 20 | |
| | | | 130 MHz to 1 GHz | 34 | |
| | | | 1 GHz to 2 GHz | 24 | |
| | | | EMI Level | 4 | - |

## 5.3.18 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/ESDA/JEDEC JS-001-2012 and ANSI/ESD S5.3.1-2009 standards.

**Table 59. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to ANSI/ESDA/JEDEC JS-001-2012 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESD STM5.3.1-2009, all the packages excepted WLCSP100 | 3 | 250 | |

1. Guaranteed by characterization results.

**Table 62. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | All pins except for PA10/PB12 (OTG_FS_ID,OTG_HS_ID) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10/PB12 (OTG_FS_ID,OTG_HS_ID) | | 7 | 10 | 14 | |
| $R_{PD}$ | Weak pull-down equivalent resistor(7) | All pins except for PA10/PB12 (OTG_FS_ID,OTG_HS_ID) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | |
| | | PA10/PB12 (OTG_FS_ID,OTG_HS_ID) | | 7 | 10 | 14 | |
| $C_{IO}$(8) | I/O pin capacitance | | - | - | 5 | - | pF |

1. Guaranteed by design.
2. Tested in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 61: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 61: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 44*.

Unless otherwise specified, the parameters given in *Table 64* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 64. I/O AC characteristics(1)(2)**

| OSPEEDRy [1:0] bit value(1) | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 00 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD} \geq 2.7$ V | - | - | 4 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq 1.7$ V | - | - | 2 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 8 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.8$ V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 3 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ = 1.7 V to 3.6 V | - | - | 100 | ns |
| 01 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 50 pF, $V_{DD} \geq 2.7$ V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD} \geq 1.8$ V | - | - | 12.5 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq 1.7$ V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.8$ V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 12.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD} \geq 2.7$ V | - | - | 10 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 6 | |
| | | | $C_L$ = 50 pF, $V_{DD} \geq 1.7$ V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency(3) | $C_L$ = 40 pF, $V_{DD} \geq 2.7$ V | - | - | 50(4) | MHz |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 100(4) | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq 1.7$ V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.8$ V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 42.5 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD} \geq 2.7$ V | - | - | 6 | ns |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 2.7$ V | - | - | 4 | |
| | | | $C_L$ = 40 pF, $V_{DD} \geq 1.7$ V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD} \geq 1.7$ V | - | - | 6 | |

### Table 82. SPI dynamic characteristics[1] (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tsu(MI) | Data input setup time | Master mode | 4 | - | - | ns |
| tsu(SI) | | Slave mode | 3.5 | - | - | |
| th(MI) | Data input hold time | Master mode | 3 | - | - | |
| th(SI) | | Slave mode | 1 | - | - | |
| ta(SO) | Data output access time | Slave mode | 7 | 9 | 21 | |
| tdis(SO) | Data output disable time | Slave mode | 5 | 7 | 12 | |
| tv(SO) | Data output valid time | Slave mode 2.7≤VDD≤3.6V | - | 6.5 | 10 | |
| | | Slave mode 1.71≤VDD≤3.6V | - | 6.5 | 13.5 | |
| tv(MO) | | Master mode | - | 2 | 3 | |
| th(SO) | Data output hold time | Slave mode 1.71≤VDD≤3.6V | 4.5 | - | - | |
| th(MO) | | Master mode | 0 | - | - | |

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO=PA5. In this configuration, the maximum achievable frequency is 40 MHz.
3. Maximum frequency of the slave transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge.This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.

### Figure 52. SPI timing diagram - slave mode and CPHA = 0

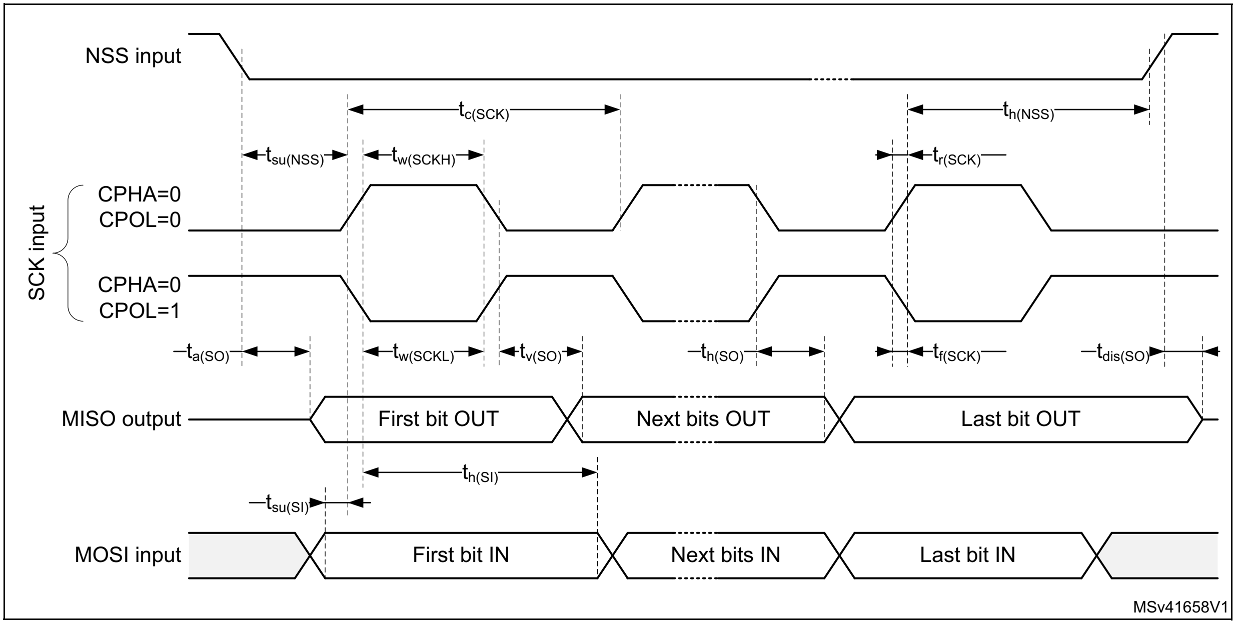


**Table 90. Dynamic characteristics: USB ULPI(1)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SC}$ | Control in (ULPI_DIR, ULPI_NXT) setup time | - | 1.5 | - | - | ns |
| $t_{HC}$ | Control in (ULPI_DIR, ULPI_NXT) hold time | - | 1 | - | - | |
| $t_{SD}$ | Data in setup time | - | 1.5 | - | - | |
| $t_{HD}$ | Data in hold time | - | 1 | - | - | |
| $t_{DC}/t_{DD}$ | Data/control output delay | 2.7 V < $V_{DD}$ < 3.6 V, $C_L$ = 20 pF and OSPEEDRy[1:0] = 11 | - | 6 | 7.5 | |
| | | - | - | 9.5 | 11 | |
| | | 1.7 V < $V_{DD}$ < 3.6 V, $C_L$ = 15 pF and OSPEEDRy[1:0] = 11 | - | | | |

1. Guaranteed by characterization results.

### USB high speed (HS) characteristics (Embedded PHY High speed in STM32F723xx devices)

**Table 91. USB OTG high speed DC electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{hssq}$ | High speed squelch detection threshold | - | 100 | - | 150 | mV |
| $V_{hsdsc}$ | High speed disconnect detection threshold | - | 525 | - | 625 | mV |
| $V_{hsdif}$ | High speed differential detection threshold | - | 100 | - | - | mV |
| $V_{hscm}$ | High speed data signalling common mode voltage range | - | -50 | - | 500 | mV |
| $V_{hsoi}$ | High speed idle level | - | -10 | - | 10 | mV |
| $V_{hsoh}$ | High speed data signaling high | - | 360 | - | 440 | mV |
| $V_{hsol}$ | High speed data signaling low | - | -10 | - | 10 | mV |
| $V_{chirpj}$ | Chirp J level | - | 700 | - | 1100 | mV |
| $V_{chirpk}$ | Chirp K level | - | -900 | - | -500 | mV |

**Table 92. USB OTG high speed electrical characteristics**

| Parameter | Comments | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{lr}$ | Rise time | - | 0.5 | - | - | ns |
| $t_{lf}$ | Fall time | - | 0.5 | - | - | ns |
| $t_{lrfm}$ | Setup time from INHSDRIVERENABLE=1 to the transition on INHSDATAP/INHSDATAN | - | 10 | - | - | ns |
| $Z_{drv}$ | Driver output impedance | - | 40.5 | - | 49.5 | Ω |

### Table 108. SDRAM read timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | 2Thclk -0.5 | 2Thclk +0.5 | ns |
| $t_{su(SDCLKH\ \_Data)}$ | Data input setup time | 1.5 | - | |
| $t_{h(SDCLKH\_Data)}$ | Data input hold time | 2 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 1.5 | |
| $t_{d(SDCLKL\text{-}\ SDNE)}$ | Chip select valid time | - | 1.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0.5 | - | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | - | 1 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0.5 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

### Table 109. LPSDR SDRAM read timings(1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | 2Thclk -0.5 | 2Thclk +0.5 | ns |
| $t_{su(SDCLKH\_Data)}$ | Data input setup time | 0 | - | |
| $t_{h(SDCLKH\_Data)}$ | Data input hold time | 4.5 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 1.5 | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip select valid time | - | 1.5 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNRAS}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

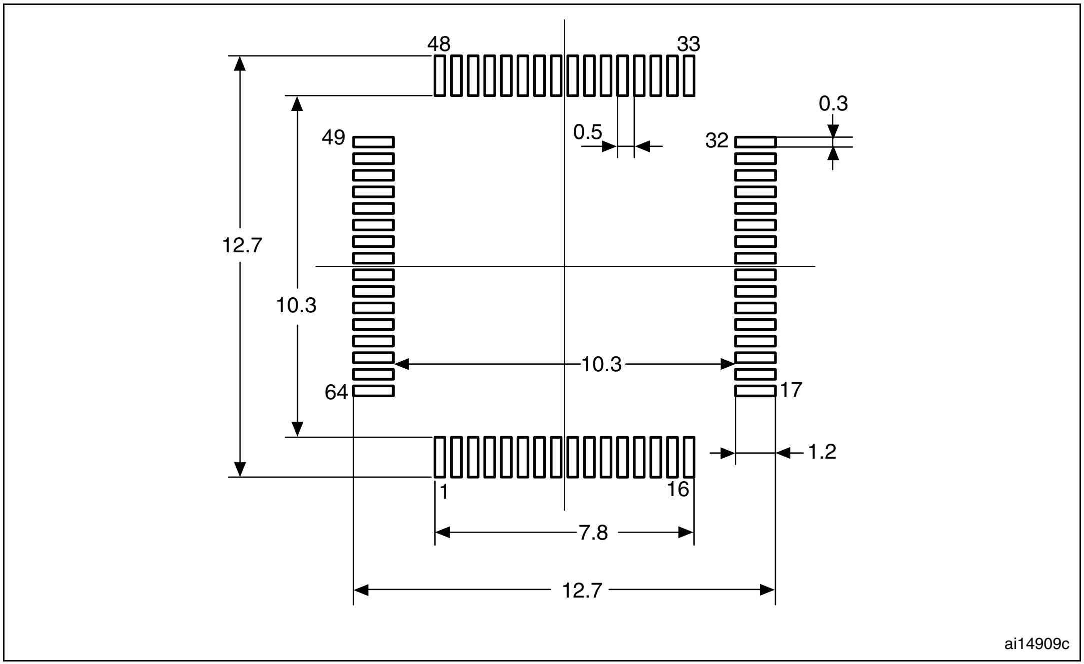
1. Guaranteed by characterization results.

### Table 116. LQFP64 – 10 x 10 mm, low-profile quad flat package mechanical data (continued)

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| c | 0.09 | - | 0.20 | 0.0035 | | 0.0079 |
| D | - | 12.00 | - | - | 0.4724 | - |
| D1 | - | 10.00 | - | - | 0.3937 | - |
| D3 | - | 7.50 | - | - | 0.2953 | - |
| E | - | 12.00 | - | - | 0.4724 | - |
| E1 | - | 10.00 | - | - | 0.3937 | - |
| E3 | - | 7.50 | - | - | 0.2953 | - |
| e | - | 0.50 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.00 | - | - | 0.0394 | - |
| ccc | - | - | 0.08 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 80. LQFP64 – 10 x 10 mm, low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.