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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 138 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f723iet6 |

2. Available only on the STM32F723xx devices.

# 2 Functional overview

## 2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (8 Kbytes of I-cache and 8 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It supports single precision FPU (floating point unit), speeds up software development by using metalanguage development tools, while avoiding saturation.

*Figure 5* shows the general block diagram of the STM32F722xx and STM32F723xx family.

*Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.*

## 2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

## 2.3 Embedded Flash memory

The STM32F722xx and STM32F723xx devices embed a Flash memory of up to 512 Kbytes available for storing programs and data.

The flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: No access (read, erase, program) to the Flash memory or backup SRAM can be performed while the debug feature is connected or while booting from RAM or system memory bootloader
  - Level 2: debug/chip read protection disabled.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): Flash memory user sectors (0 to 7) can be protected against D-bus read accesses by using the proprietary readout protection (PCROP). The protected area is execute-only.

## 2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 256 Kbytes:
  - SRAM1 on AHB bus Matrix: 176 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 64 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripheral DMAs through the specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.

## 2.19 $V_{BAT}$ operation

The $V_{BAT}$ pin allows to power the device $V_{BAT}$ domain from an external battery, an external supercapacitor, or from $V_{DD}$ when no external battery and an external supercapacitor are present.

The $V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The $V_{BAT}$ pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

*When the PDR_ON pin is connected to $V_{SS}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and the $V_{BAT}$ pin should be connected to $V_{DD}$.*

## 2.20 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

*Table 6* compares the features of the advanced-control, general-purpose and basic timers.

### 2.20.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 2.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 2.20.6 Window watchdog

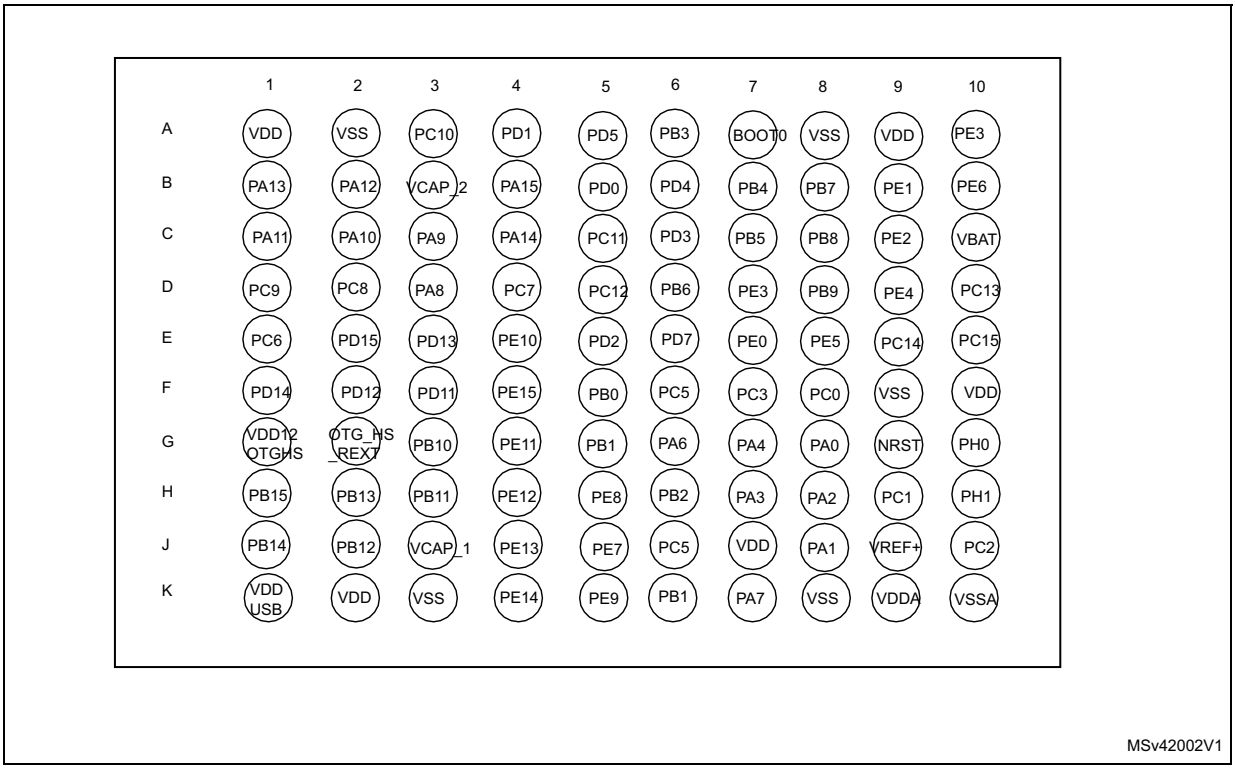
The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### 2.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

**Figure 16. STM32F723xx WLCSP100 ballout (with OTG PHY HS)**




1. The above figure shows the package top view.

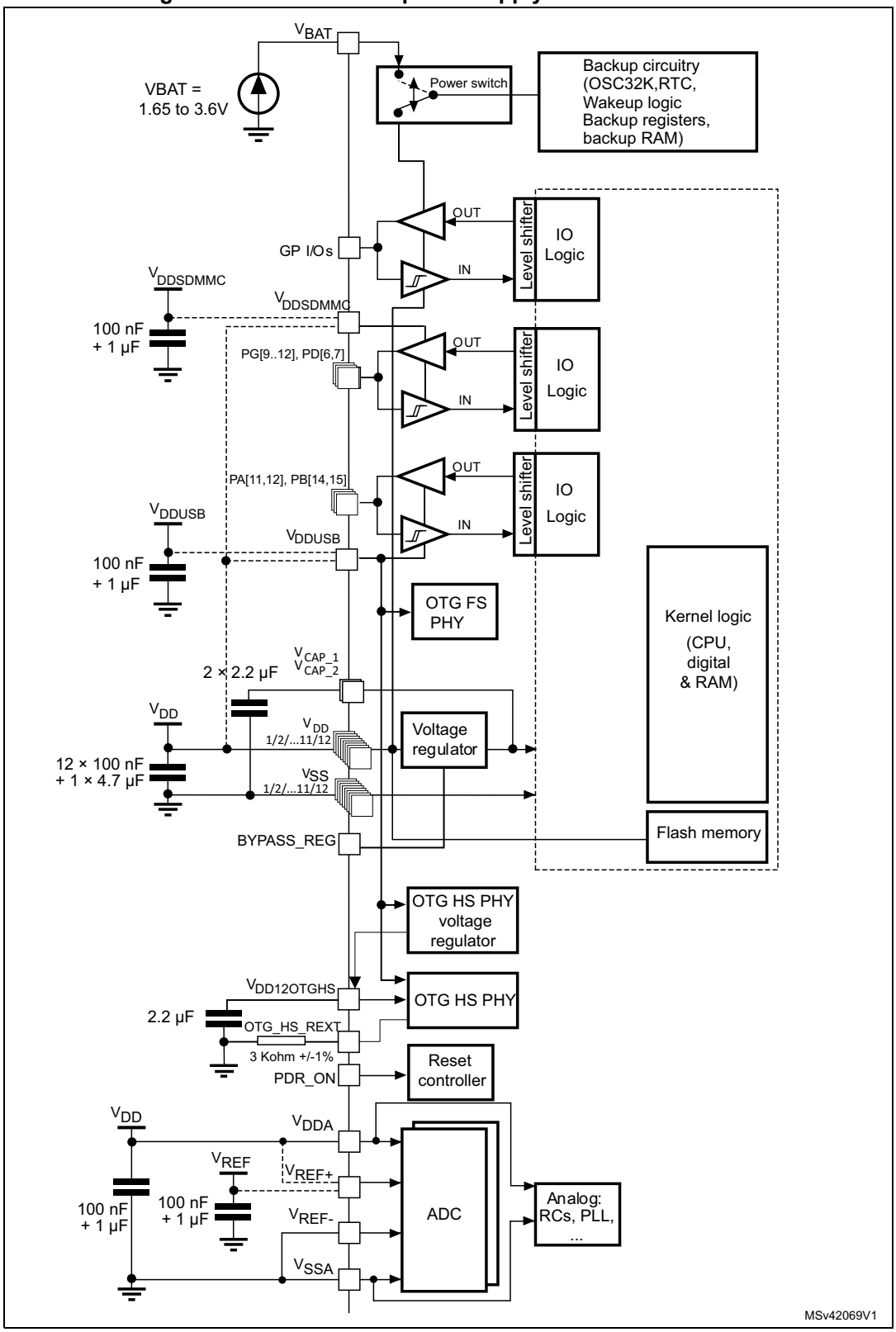
Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F722xx | | | | | STM32F723xx | | | | | | | | | | |
| LQFP64 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | WLCSP100 | UFBGA176 | UFBGA144 | LQFP144 | LQFP176 | | | | | | |
| - | - | - | M13 | 86 | - | M13 | - | - | 86 | PH9 | I/O | FT | - | I2C3_SMBA, TIM12_CH2, FMC_D17, EVENTOUT | - |
| - | - | - | L13 | 87 | - | L13 | - | - | 87 | PH10 | I/O | FT | - | TIM5_CH1, FMC_D18, EVENTOUT | - |
| - | - | - | L12 | 88 | - | L12 | - | - | 88 | PH11 | I/O | FT | - | TIM5_CH2, FMC_D19, EVENTOUT | - |
| - | - | - | K12 | 89 | - | K12 | - | - | 89 | PH12 | I/O | FT | - | TIM5_CH3, FMC_D20, EVENTOUT | - |
| - | - | - | H12 | 90 | - | H12 | - | - | 90 | VSS | S | - | - | - | - |
| - | - | - | J12 | 91 | K2 | J12 | - | - | 91 | VDD | S | - | - | - | - |
| 33 | 51 | 73 | P12 | 92 | J2 | P12 | M11 | 73 | 92 | PB12 | I/O | FT | (4) | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, OTG_HS_ULPI_D5, OTG_HS_ID, EVENTOUT | - |
| 34 | 52 | 74 | P13 | 93 | H2 | P13 | M12 | 74 | 93 | PB13 | I/O | FT | (4) | TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, OTG_HS_ULPI_D6, EVENTOUT | OTG_HS_VBUS |
| - | - | - | - | - | G2 | J15 | H11 | 75 | 94 | OTG_HS_REXT | - | - | - | USB HS OTG PHY calibration resistor | |
| - | - | - | - | - | G1 | J14 | H10 | 76 | 95 | VDD12OTGHS | - | - | - | - | - |

Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

| Pin Number | | | | | | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STM32F722xx | | | | | STM32F723xx | | | | | | | | | | |
| LQFP64 | LQFP100 | LQFP144 | UFBGA176 | LQFP176 | WLCSP100 | UFBGA176 | UFBGA144 | LQFP144 | LQFP176 | | | | | | |
| - | - | 125 | B10 | 153 | - | B10 | D8 | 125 | 153 | PG10 | I/O | FT | - | SAI2_SD_B, SDMMC2_D1, FMC_NE3, EVENTOUT | - |
| - | - | 126 | B9 | 154 | - | B9 | C8 | 126 | 154 | PG11 | I/O | FT | - | SDMMC2_D2, FMC_INT, EVENTOUT | - |
| - | - | 127 | B8 | 155 | - | B8 | B8 | 127 | 155 | PG12 | I/O | FT | - | LPTIM1_IN1, USART6_RTS, SDMMC2_D3, FMC_NE4, EVENTOUT | - |
| - | - | 128 | A8 | 156 | - | A8 | D7 | 128 | 156 | PG13 | I/O | FT | - | TRACED0, LPTIM1_OUT, USART6_CTS, FMC_A24, EVENTOUT | - |
| - | - | 129 | A7 | 157 | - | A7 | C7 | 129 | 157 | PG14 | I/O | FT | - | TRACED1, LPTIM1_ETR, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, EVENTOUT | - |
| - | - | 130 | D7 | 158 | - | D7 | - | 130 | 158 | VSS | S | - | - | - | - |

**Figure 28. STM32F723xx power supply scheme**




1. The $V_{DDUSB}$ allows supplying the PHY FS in PA11/PA12 and the PHY HS on PB14/PB15.

**Table 23. reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 2.92 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V |
| $V_{PVDhyst}$(1) | PVD hysteresis | - | - | 100 | - | mV |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Falling edge | 1.60 | 1.68 | 1.76 | V |
| | | Rising edge | 1.64 | 1.72 | 1.80 | V |
| $V_{PDRhyst}$(1) | PDR hysteresis | - | - | 40 | - | mV |
| $V_{BOR1}$ | Brownout level 1 threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |
| $V_{BOR2}$ | Brownout level 2 threshold | Falling edge | 2.44 | 2.50 | 2.56 | V |
| | | Rising edge | 2.53 | 2.59 | 2.63 | V |
| $V_{BOR3}$ | Brownout level 3 threshold | Falling edge | 2.75 | 2.83 | 2.88 | V |
| | | Rising edge | 2.85 | 2.92 | 2.97 | V |
| $V_{BORhyst}$(1) | BOR hysteresis | - | - | 100 | - | mV |
| $T_{RSTTEMPO}$(1)(2) | POR reset temporization | - | 0.5 | 1.5 | 3.0 | ms |
| $I_{RUSH}$(1) | InRush current on voltage regulator power-on (POR or wakeup from Standby) | - | - | 160 | 250 | mA |
| $E_{RUSH}$(1) | InRush energy on voltage regulator power-on (POR or wakeup from Standby) | $V_{DD}$ = 1.7 V, $T_A$ = 105 °C, $I_{RUSH}$ = 171 mA for 31 µs | - | - | 5.4 | µC |

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to $f_{HCLK}$ frequency and $V_{DD}$ range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when $f_{HCLK}$ is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and for $T_A$= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and a maximum ambient temperature ($T_A$) unless otherwise specified.
- For the voltage range 1.7 V ≤ $V_{DD}$ ≤ 3.6 V, the maximum frequency is 180 MHz.

**Table 25. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 156 | 170(4) | 180(4) | 200 | mA |
| | | | 200 | 144 | 154 | 164.6 | 183 | |
| | | | 180 | 127 | 134(4) | 143(4) | 158(4) | |
| | | | 168 | 113 | 119 | 127.4 | 141 | |
| | | | 144 | 86 | 96 | 112.6 | 126 | |
| | | | 60 | 41 | 44 | 52.8 | 65 | |
| | | | 25 | 22 | 24 | 33.5 | 45 | |
| | | All peripherals disabled(3) | 216 | 99 | 110(4) | 119.6(4) | 138.5 | |
| | | | 200 | 92 | 102 | 113.1 | 132 | |
| | | | 180 | 81 | 90(4) | 96.7(4) | 125(4) | |
| | | | 168 | 72 | 78 | 86.5 | 100.1 | |
| | | | 144 | 55 | 61 | 77.1 | 90.8 | |
| | | | 60 | 24 | 25 | 38.5 | 50.3 | |
| | | | 25 | 12 | 13 | 26.3 | 38.1 | |

1. Guaranteed by characterization results.

### 5.3.13 USB OTG HS PHY PLLs characteristics (on STM32F723xx devices)

The parameters given in *Table 49* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 49. USB OTG HS PLL1 characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL1\_IN}$ | PLL1 input clock | - | 12, 12.5, 16, 24, 25 | | | MHz |
| $f_{PLL1\_OUT}$ | PLL1 output clock(2) | - | - | 60 | - | |
| $f_{VCO\_OUT}$ | PLL1 VCO output | - | 600 | - | 720 | |
| $t_{LOCK}$ | PLL1 lock time(2) | - | - | - | 22 | µs |
| $I_{DD(PLL1)}$ | PLL1 digital power consumption | - | - | - | 1.8 | mA |
| $I_{DDA(PLL1)}$ | PLL1 analog power consumption | - | - | - | 2.75 | |

1. Guaranteed by design.
2. Based on test during characterization.

**Table 50. USB OTG HS PLL2 characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL2\_IN}$ | PLL2 input clock | - | - | 60 | - | MHz |
| $f_{PLL2\_OUT}$ | PLL2 output clock(2) | - | - | 480 | - | |
| $f_{VCO\_OUT}$ | PLL2 VCO output | - | - | 480 | - | |
| $t_{LOCK}$ | PLL2 lock time(2) | - | - | - | 91 | µs |
| $I_{DD(PLL2)}$ | PLL2 digital power consumption | - | - | - | 2.1 | mA |
| $I_{DDA(PLL2)}$ | PLL2 analog power consumption | - | - | - | 1.5 | |

1. Guaranteed by design.
2. Based on test during characterization.

### 5.3.14 USB OTG HS PHY regulator characteristics (on STM32F723xx devices)

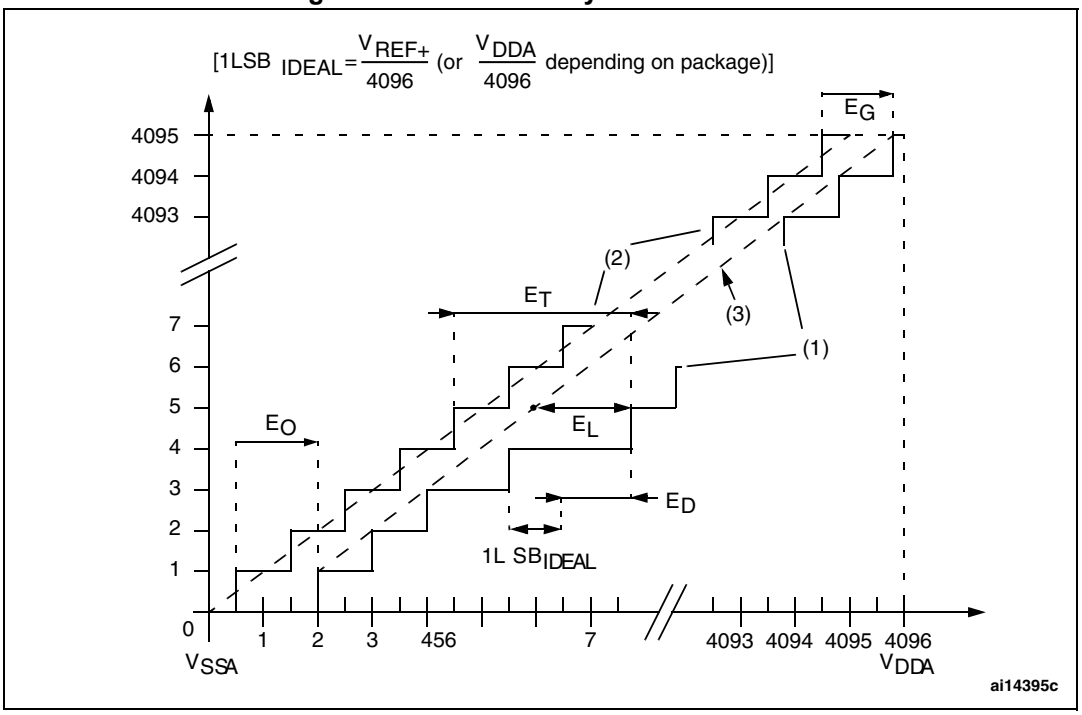
The parameters given in *Table 51* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

**Table 51. USB OTG HS PHY regulator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD12OTGHS}$ | 1.2 V internal voltage on $V_{DD12OTGHS}$ | - | 1.18 | 1.2 | 1.24 | V |
| CEXT | External capacitor on $V_{DD12OTGHS}$ | - | 1.1 | 2.2 | 3.3 | µF |
| $I_{DDPHYHSREG}$ | Regulator power consumption | - | 100 | 120 | 125 | µA |

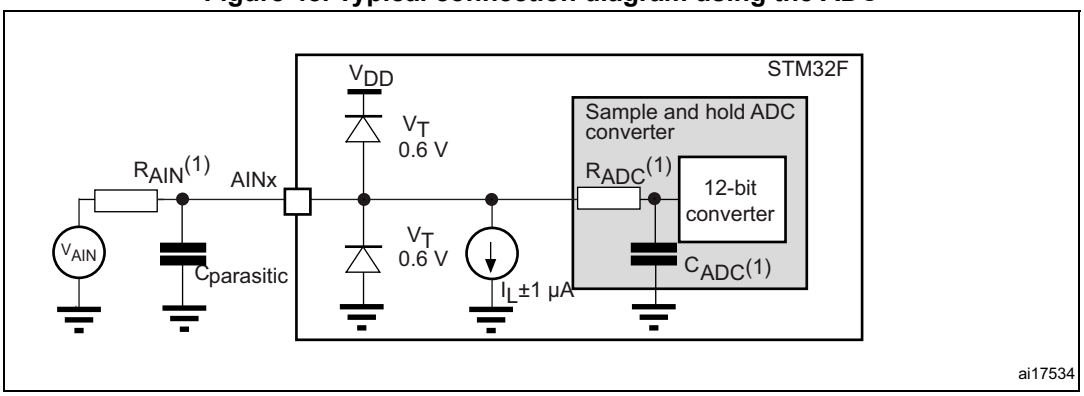
1. Based on test during characterization.

**Figure 47. ADC accuracy characteristics**




1. See also *Table 70*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. $E_T$ = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 48. Typical connection diagram using the ADC**




1. Refer to *Table 68* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 82* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 82. SPI dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode<br>SPI1,4,5<br>2.7≤VDD≤3.6 | - | - | 54(2) | MHz |
| | | Master mode<br>SPI1,4,5<br>1.71≤VDD≤3.6 | - | - | 27 | |
| | | Master transmitter mode<br>SPI1,4,5<br>1.71≤VDD≤3.6 | - | - | 54 | |
| | | Slave receiver mode<br>SPI1,4,5<br>1.71≤VDD≤3.6 | - | - | 54 | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5<br>2.7≤VDD≤3.6 | - | - | 50(3) | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5<br>1.71≤VDD≤3.6 | - | - | 37(3) | |
| | | Master & Slave mode<br>SPI2,3<br>1.71≤VDD≤3.6 | - | - | 27 | |
| tsu(NSS) | NSS setup time | Slave mode, SPI presc = 2 | 4xTpclk | - | - | ns |
| th(NSS) | NSS hold time | Slave mode, SPI presc = 2 | 2xTpclk | - | - | |
| tw(SCKH)<br>tw(SCKL) | SCK high and low time | Master mode | Tpclk-1 | Tpclk | Tpclk+1 | |

**Table 93. USB FS PHY BCD electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DDUSB}$ | Primary detection mode consumption | - | - | - | 300 | µA |
| | Secondary detection mode consumption | - | - | - | 300 | |
| $R_{DAT\_LKG}$ | Data line leakage resistance | - | 300 | - | - | kΩ |
| $V_{DAT\_LKG}$ | Data line leakage voltage | - | 0.0 | - | 3.6 | V |
| $R_{DCP\_DAT}$ | Dedicated charging port resistance across D+/D- | - | - | - | 200 | Ω |
| $V_{LGC\_HI}$ | Logic high | - | 2.0 | - | 3.6 | V |
| $V_{LGC\_LOW}$ | Logic low | - | - | - | 0.8 | |
| $VL_{GC}$ | Logic threshold | - | 0.8 | - | 2.0 | |
| $V_{DAT\_REF}$ | Data detect voltage | - | 0.25 | - | 3.6 | |
| $V_{DP\_SRC}$ | D+ source voltage | - | 0.5 | - | 3.6 | |
| $V_{DM\_SRC}$ | D- source voltage | - | 0.5 | - | 3.6 | |
| $I_{DM\_SINK}$ | D- sink current | - | 25 | - | 175 | µA |
| $I_{DP\_SINK}$ | D+ sink current | - | 25 | - | 175 | |
| $I_{DP\_SRC}$ | Data contact detect current source | - | 7 | - | 30 | |

### CAN (controller area network) interface

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

## 5.3.30 FMC characteristics

Unless otherwise specified, the parameters given in *Table 94* to *Table 107* for the FMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.20: I/O port characteristics* for more details on the input/output characteristics.

### Asynchronous waveforms and timings

*Figure 61* through *Figure 64* represent asynchronous waveforms and *Table 94* through *Table 101* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capcitive load CL = 30 pF

In all timing tables, the $T_{HCLK}$ is the HCLK clock period

**Table 97. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | 8Thclk -1 | 8Thclk +1 | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | 6Thclk -1.5 | 6Thclk +0.5 | |
| $t_{su(NWAIT\_NE)}$ | FMC_NWAIT valid before FMC_NEx high | 6Thclk -1 | - | |
| $t_{h(NE\_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | 4Thclk + 2 | - | |

1. Guaranteed by characterization results.

**Figure 63. Asynchronous multiplexed PSRAM/NOR read waveforms**

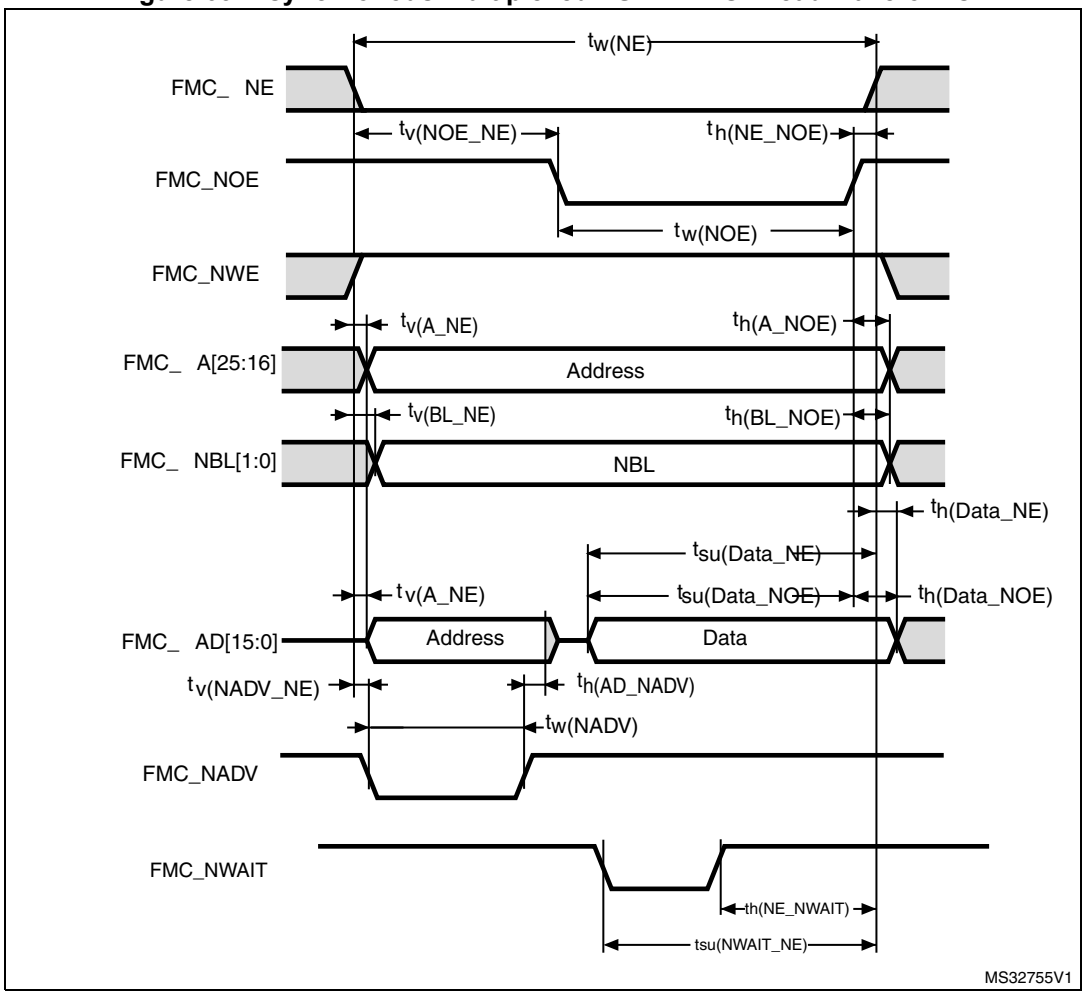


**Table 105. Synchronous non-multiplexed PSRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{(CLK)}$ | FMC_CLK period | 2Thclk - 0.5 | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2 | |
| $t_{(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | Thclk +0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 3 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | Thclk | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{d(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | Thclk +1 | - | |
| $t_{d(CLKL-Data)}$ | FMC_D[15:0] valid data after FMC_CLK low | - | 3 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | - | 2 | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | Thclk +1 | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 3.5 | - | |

1. Guaranteed by characterization results.

### NAND controller waveforms and timings

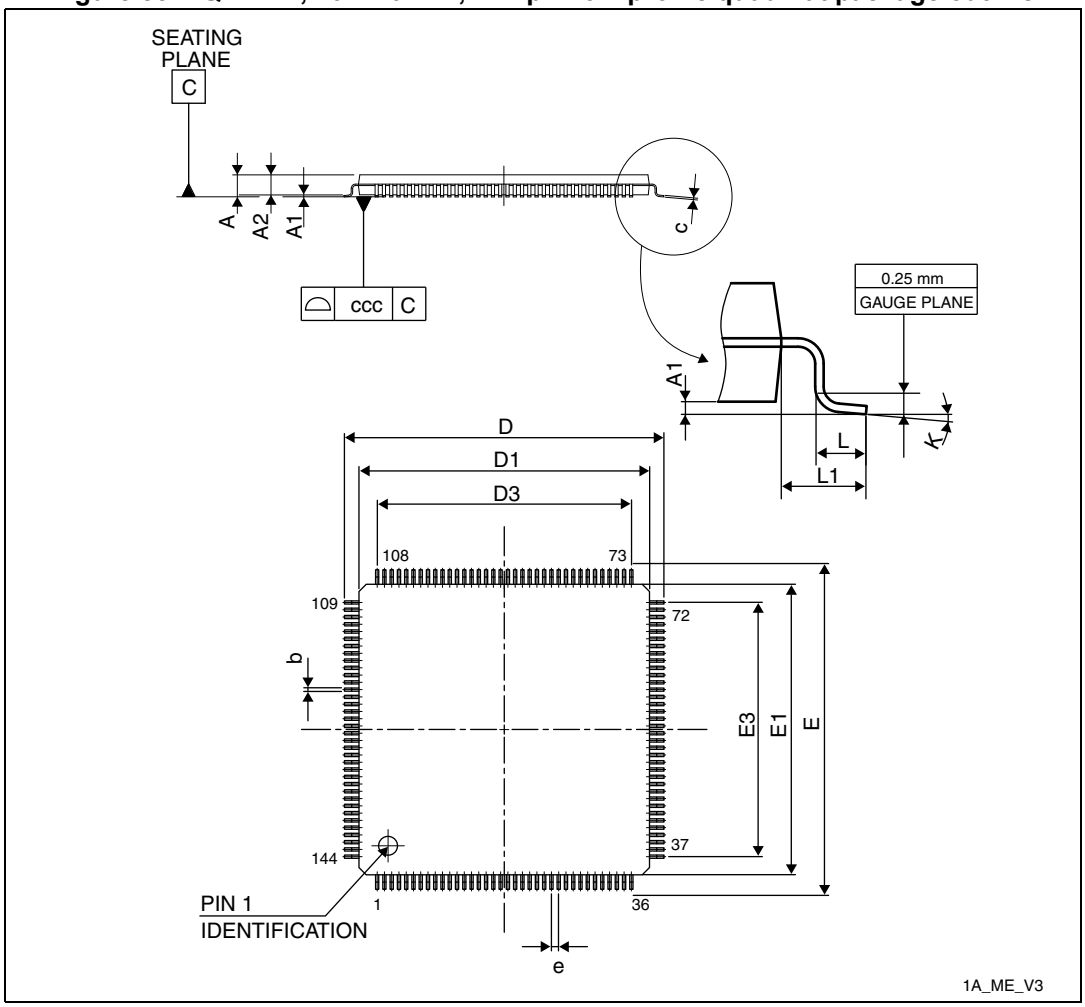
*Figure 69* through *Figure 72* represent synchronous waveforms, and *Table 106* and *Table 107* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x01;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x01;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the $T_{HCLK}$ is the HCLK clock period.

## 6.3 LQFP144, 20 x 20 mm low-profile quad flat package information

**Figure 85. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline**



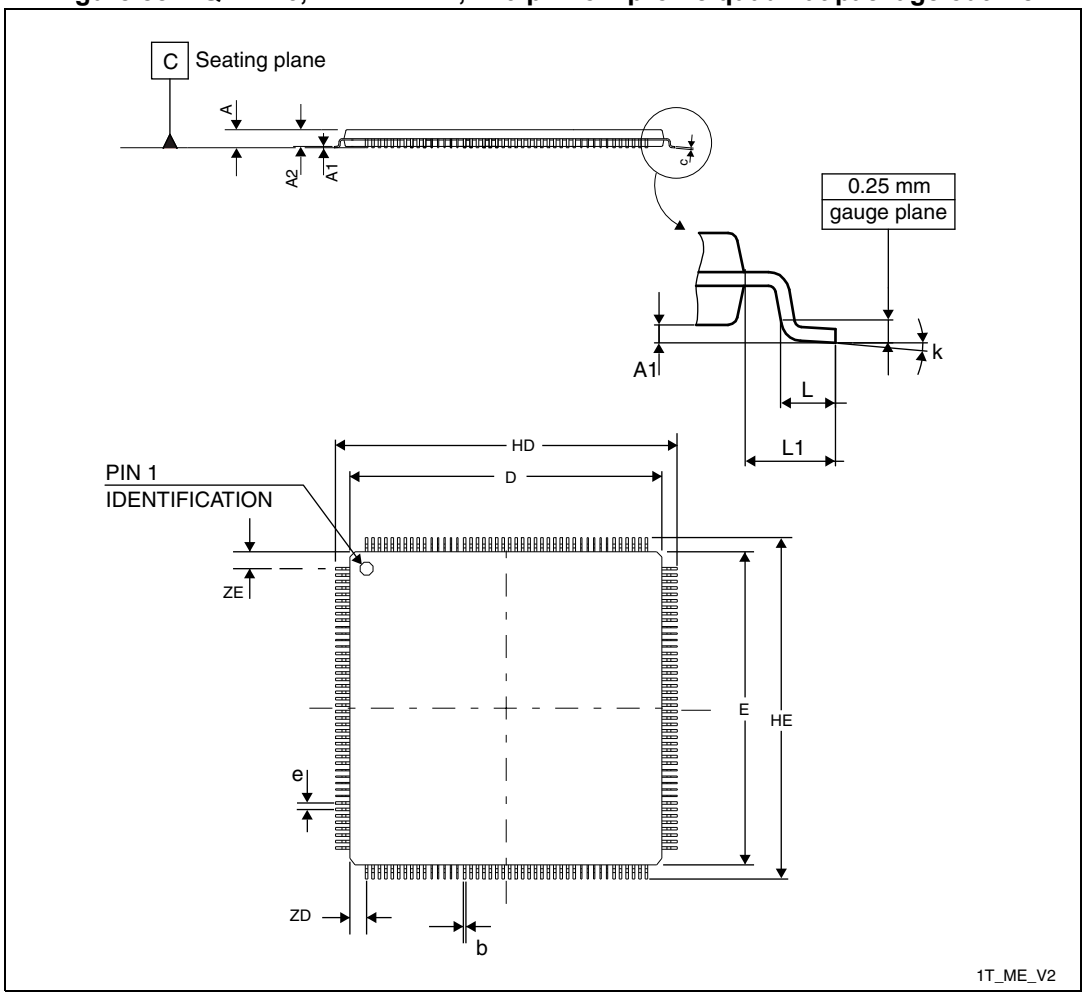

1. Drawing is not to scale.

**Table 118. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |

## 6.4 LQFP176 24 x 24 mm low-profile quad flat package information

**Figure 88. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 119. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | - | 1.450 | 0.0531 | - | 0.0060 |
| b | 0.170 | - | 0.270 | 0.0067 | - | 0.0106 |
| C | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |

**Table 124. WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Typ | Min | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.17 | - | - | 0.0067 | - |
| A2 | - | 0.38 | - | - | 0.0150 | - |
| A3[2] | - | 0.025 | - | - | 0.0010 | - |
| Ø b[3] | 0.22 | 0.25 | 0.28 | - | 0.0098 | 0.0110 |
| D | 4.166 | 4.201 | 4.236 | - | 0.1654 | 0.1668 |
| E | 4.628 | 4.663 | 4.698 | - | 0.1836 | 0.1850 |
| e | - | 0.4 | - | - | 0.0157 | - |
| e1 | - | 3.6 | - | - | 0.1417 | - |
| e2 | - | 3.6 | - | - | 0.1417 | - |
| F | - | 0.3005 | - | - | 0.0118 | - |
| G | - | 0.5315 | - | - | 0.0209 | - |
| N | - | 100 | - | - | 3.9370 | - |
| aaa | - | 0.1 | - | - | 0.0039 | - |
| bbb | - | 0.1 | - | - | 0.0039 | - |
| ccc | - | 0.1 | - | - | 0.0039 | - |
| ddd | - | 0.05 | - | - | 0.0020 | - |
| eee | - | 0.05 | - | - | 0.0020 | - |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

# Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- $V_{BAT}$ functionality is no more available and VBAT pin should be connected to $V_{DD}$.
- The over-drive mode is not supported.

## A.1 Operating conditions

**Table 128. Limitations depending on the operating power supply range**

| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum Flash memory access frequency with wait states (1)(2) | I/O operation | Possible Flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz | 180 MHz with 8 wait states and over-drive OFF | – No I/O compensation | 8-bit erase and program operations only |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 2.15.1: Internal reset ON*).