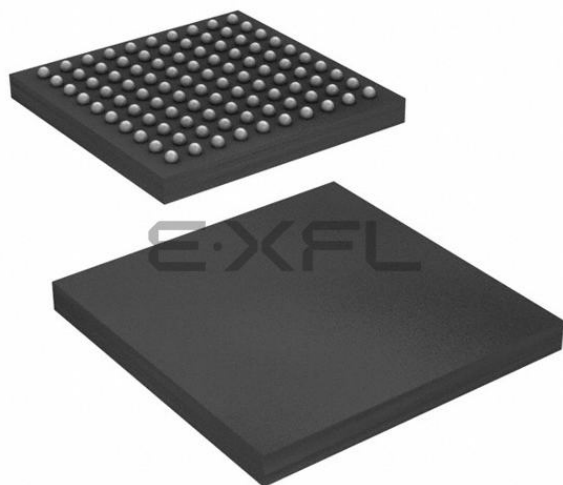




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	216MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA, WLCSP
Supplier Device Package	100-WLCSP (4.2x4.7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f723vey6tr

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Table 3. Voltage regulator configuration mode versus device operating mode⁽¹⁾

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode ⁽²⁾	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.

2. The over-drive mode is not available when $V_{DD} = 1.7$ to 2.1 V.

2.16.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. The two $2.2\ \mu\text{F}$ ceramic capacitors should be replaced by two $100\ \text{nF}$ decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12} . An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. The PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

All the RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.18 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5: Voltage regulator modes in stop mode](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup and the LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

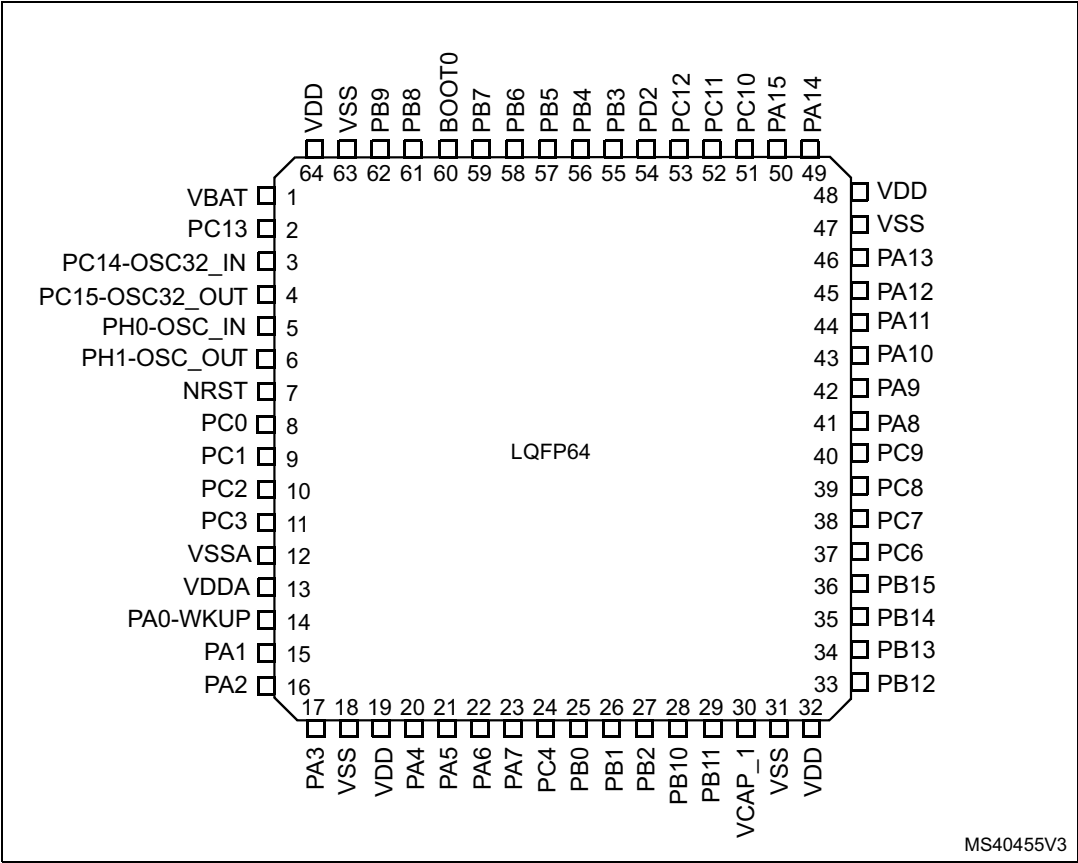
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

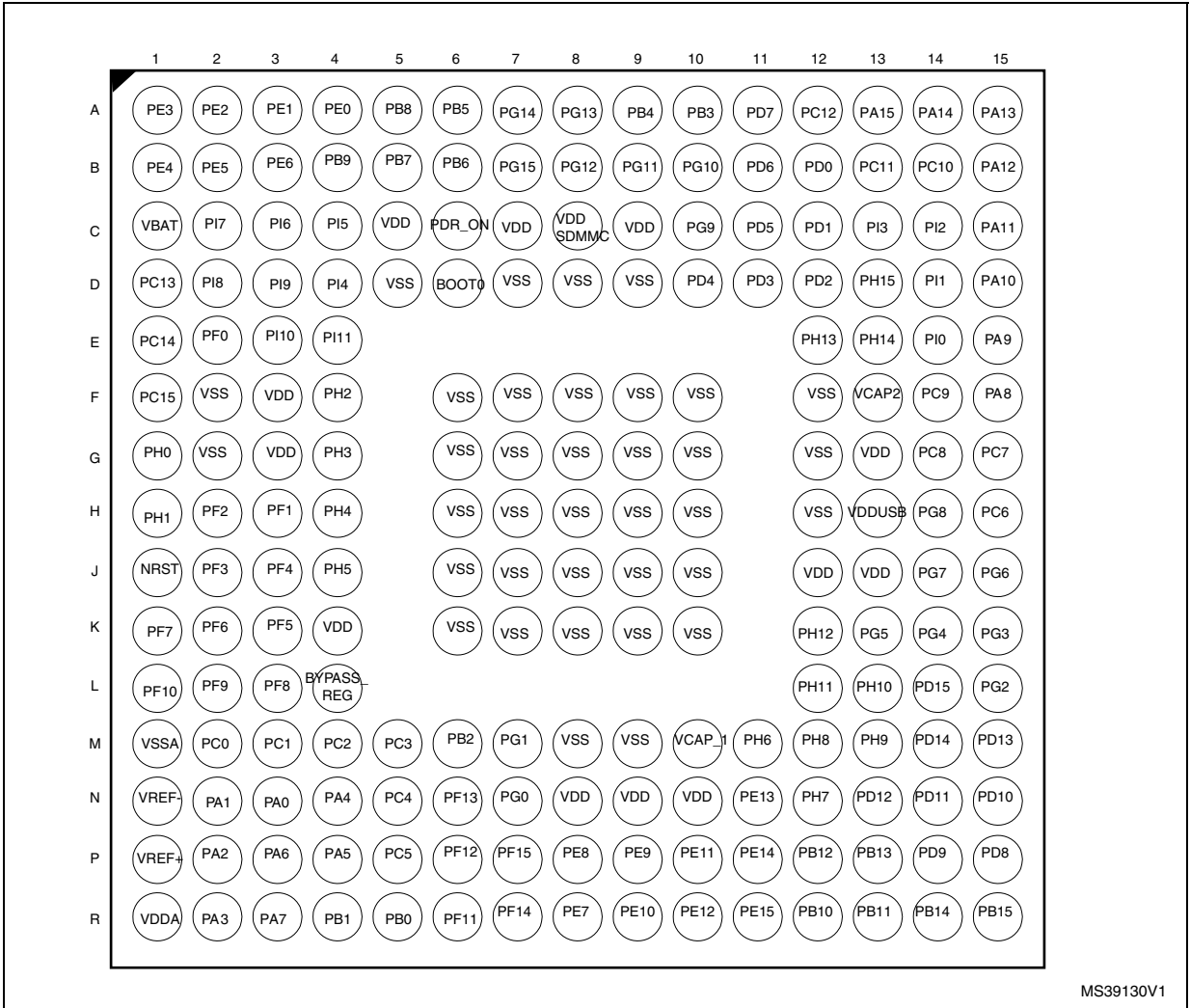
3 Pinouts and pin description

Figure 14. STM32F722xx LQFP64 pinout



1. The above figure shows the package top view.

Figure 22. STM32F723xx UFBGA176 ballout



MS39130V1

1. The above figure shows the package top view.



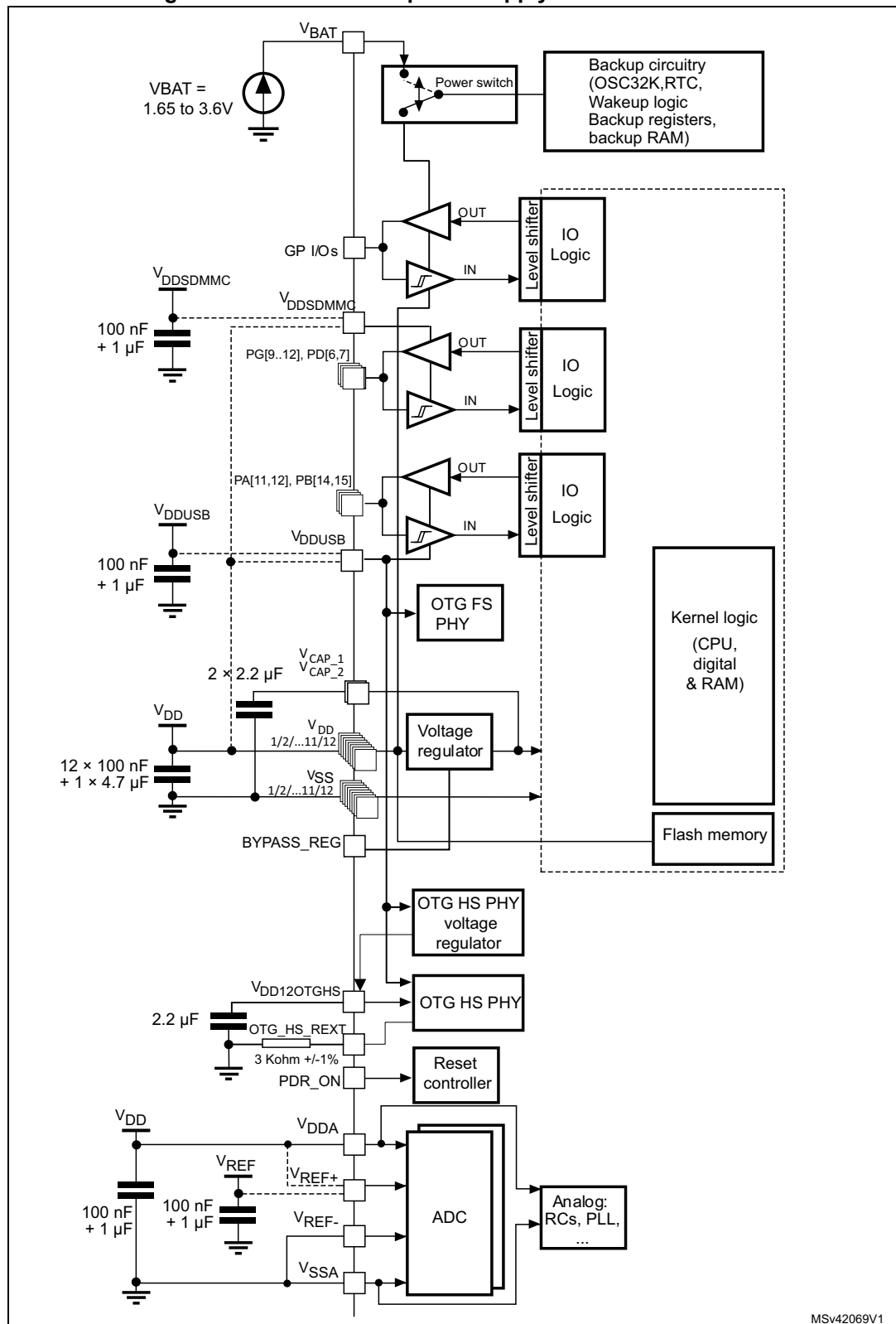
Table 10. STM32F722xx and STM32F723xx pin and ball definition (continued)

Pin Number										Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F722xx					STM32F723xx										
LQFP64	LQFP100	LQFP144	UFBGA176	LQFP176	WLCSP100	UFBGA176	UFBGA144	LQFP144	LQFP176						
54	83	116	D12	144	E5	D12	E9	116	144	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, EVENTOUT	-
-	84	117	D11	145	C6	D11	D9	117	145	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, EVENTOUT	-
-	85	118	D10	146	B6	D10	C9	118	146	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
-	86	119	C11	147	A5	C11	B9	119	147	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	-	120	D8	148	-	D8	E7	120	148	VSS	S	-	-	-	-
-	-	121	C8	149	-	C8	F7	121	149	VDDSDMMC	S	-	-	-	-
-	87	122	B11	150	D6	B11	A8	122	150	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, SDMMC2_CK, FMC_NWAIT, EVENTOUT	-
-	88	123	A11	151	E6	A11	A9	123	151	PD7	I/O	FT	-	USART2_CK SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	124	C10	152	-	C10	E8	124	152	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, EVENTOUT	-

Table 12. STM32F722xx and STM32F723xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1	I2C1/2/3/USART1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5	SPI2/I2S2/SPI3/I2S3/SAI1/UART4	SPI2/I2S2/SPI3/I2S3/USART1/2/3/UART5	SAI2/USART6/UART4/5/7/8/OTG1_FS	CAN1/TIM12/13/14/QUADSPI/FMC/OTG2_HS	SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS	SDMMC2	UART7/FMC/SDMMC1/OTG2_FS	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	EVEN TOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	EVEN TOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	EVEN TOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	EVEN TOUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	EVEN TOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	EVEN TOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVEN TOUT
	PG7	-	-	-	-	-	-	-	-	USART6_CK	-	-	-	FMC_INT	EVEN TOUT
	PG8	-	-	-	-	-	-	-	-	USART6_RTS	-	-	-	FMC_SCLK	EVEN TOUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	SDMMC2_D0	FMC_NE2/FMC_NCE	EVEN TOUT
	PG10	-	-	-	-	-	-	-	-	-	-	SAI2_SD_B	SDMMC2_D1	FMC_NE3	EVEN TOUT

Figure 28. STM32F723xx power supply scheme



1. The V_{DDUSB} allows supplying the PHY FS in PA11/PA12 and the PHY HS on PB14/PB15.

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	- 65 to +150	°C
T_J	Maximum junction temperature	125	

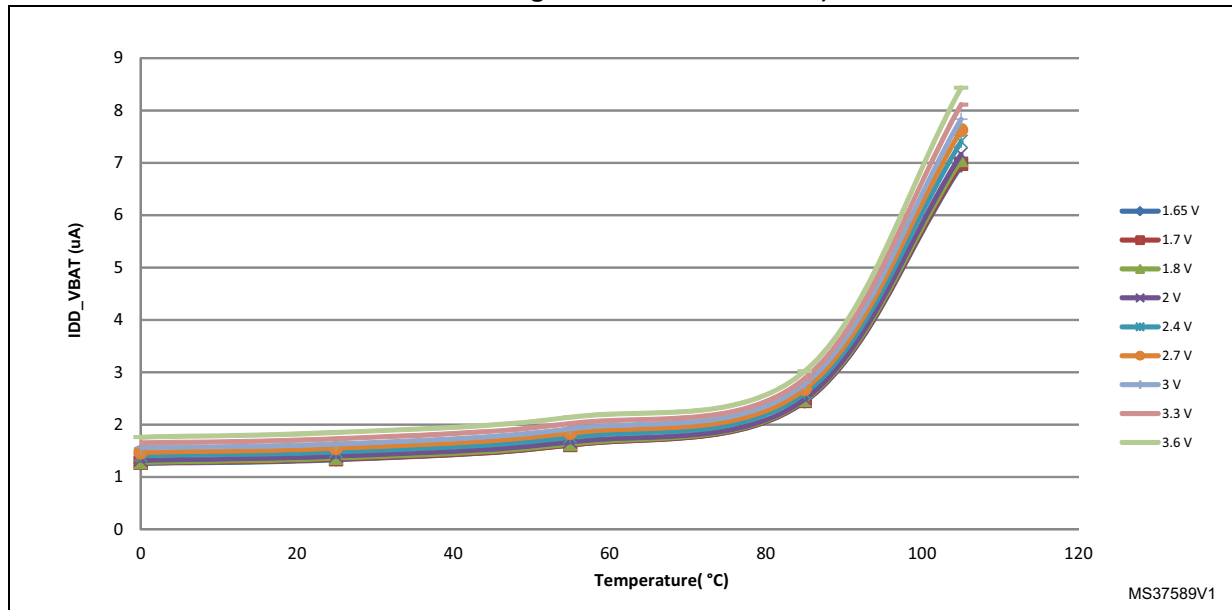
5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF	0	-	144	MHz
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	0	-	168	
				-	180	
		Power Scale 1 (VOS[1:0] bits in PWR_CR register = 0x11), Regulator ON	0	-	180	
				-	216 ⁽²⁾	
f_{PCLK1}	Internal APB1 clock frequency	Over-drive OFF	0	-	45	
		Over-drive ON	0	-	54	
f_{PCLK2}	Internal APB2 clock frequency	Over-drive OFF	0	-	90	
		Over-drive ON	0	-	108	
V_{DD}	Standard operating voltage	-	1.7 ⁽³⁾	-	3.6	V
$V_{DDA}^{(4)(5)}$	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as $V_{DD}^{(6)}$	1.7 ⁽³⁾	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins)	USB not used	1.7	3.3	3.6	
		USB used	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	
$V_{DDSDMMC}$	SDMMC2 supply voltage (supply voltage for PG[12:9] and PD6 pins)	It can be different from V_{DD}	1.7	-	3.6	

Figure 35. Typical V_{BAT} current consumption (RTC ON/BKP SRAM OFF and LSE in high medium drive mode)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 62: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 36: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O

Table 68. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	$V_{\text{DDA}} = 1.7^{(1)}$ to 2.4 V	0.6	15	18	MHz
		$V_{\text{DDA}} = 2.4$ to 3.6 V	0.6	30	36	MHz
$f_{\text{TRIG}}^{(2)}$	External trigger frequency	$f_{\text{ADC}} = 30$ MHz, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{\text{ADC}}$
V_{AIN}	Conversion voltage range ⁽³⁾	-	0 (V_{SSA} or V_{REF} - tied to ground)	-	$V_{\text{REF+}}$	V
$R_{\text{AIN}}^{(2)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{\text{ADC}}^{(2)(4)}$	Sampling switch resistance	-	-	-	6	k Ω
$C_{\text{ADC}}^{(2)}$	Internal sample and hold capacitor	-	-	4	7	pF
$t_{\text{lat}}^{(2)}$	Injection trigger conversion latency	$f_{\text{ADC}} = 30$ MHz	-	-	0.100	μs
		-	-	-	3 ⁽⁵⁾	$1/f_{\text{ADC}}$
$t_{\text{latr}}^{(2)}$	Regular trigger conversion latency	$f_{\text{ADC}} = 30$ MHz	-	-	0.067	μs
		-	-	-	2 ⁽⁵⁾	$1/f_{\text{ADC}}$
$t_{\text{S}}^{(2)}$	Sampling time	$f_{\text{ADC}} = 30$ MHz	0.100	-	16	μs
		-	3	-	480	$1/f_{\text{ADC}}$
$t_{\text{STAB}}^{(2)}$	Power-up time	-	-	2	3	μs
$t_{\text{CONV}}^{(2)}$	Total conversion time (including sampling time)	$f_{\text{ADC}} = 30$ MHz 12-bit resolution	0.50	-	16.40	μs
		$f_{\text{ADC}} = 30$ MHz 10-bit resolution	0.43	-	16.34	μs
		$f_{\text{ADC}} = 30$ MHz 8-bit resolution	0.37	-	16.27	μs
		$f_{\text{ADC}} = 30$ MHz 6-bit resolution	0.30	-	16.20	μs
		9 to 492 (t_{S} for sampling +n-bit resolution for successive approximation)				$1/f_{\text{ADC}}$
$f_{\text{S}}^{(2)}$	Sampling rate ($f_{\text{ADC}} = 36$ MHz, and $t_{\text{S}} = 3$ ADC cycles)	12-bit resolution Single ADC	-	-	2.4	Msp/s
		12-bit resolution Interleave Dual ADC mode	-	-	4.5	Msp/s
		12-bit resolution Interleave Triple ADC mode	-	-	7.2	Msp/s

Table 68. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VREF+}^{(2)}$	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	μA
$I_{VDDA}^{(2)}$	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

- V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 2.17.2: Internal reset OFF](#)).
- Guaranteed by characterization results.
- V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
- R_{ADC} maximum value is given for $V_{DD}=1.7$ V, and minimum value for $V_{DD}=3.3$ V.
- For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 68](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. $N = 12$ (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 69. ADC static accuracy at $f_{ADC} = 18$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to 3.6 V $V_{REF} = 1.7$ to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	± 3	± 4	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 1	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 2	± 3	

- Guaranteed by characterization results.

Table 70. ADC static accuracy at $f_{ADC} = 30$ MHz

Symbol	Parameter	Test conditions	Typ	Max ⁽¹⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 30$ MHz, $R_{AIN} < 10$ k Ω , $V_{DDA} = 2.4$ to 3.6 V, $V_{REF} = 1.7$ to 3.6 V, $V_{DDA} - V_{REF} < 1.2$ V	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 4	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

- Guaranteed by characterization results.

Table 82. SPI dynamic characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tsu(MI)	Data input setup time	Master mode	4	-	-	ns
tsu(SI)		Slave mode	3.5	-	-	
th(MI)	Data input hold time	Master mode	3	-	-	
th(SI)		Slave mode	1	-	-	
ta(SO)	Data output access time	Slave mode	7	9	21	
tdis(SO)	Data output disable time	Slave mode	5	7	12	
tv(SO)	Data output valid time	Slave mode $2.7 \leq VDD \leq 3.6V$	-	6.5	10	
		Slave mode $1.71 \leq VDD \leq 3.6V$	-	6.5	13.5	
tv(MO)		Master mode	-	2	3	
th(SO)	Data output hold time	Slave mode $1.71 \leq VDD \leq 3.6V$	4.5	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Excepting SPI1 with SCK IO=PA5. In this configuration, the maximum achievable frequency is 40 MHz.
3. Maximum frequency of the slave transmitter is determined by sum of Tv(SO) and Tsu(MI) intervals which has to fit into SCK level phase preceding the SCK sampling edge. This value can be achieved when it communicates with a Master having Tsu(MI)=0 while signal Duty(SCK)=50%.

Figure 52. SPI timing diagram - slave mode and CPHA = 0

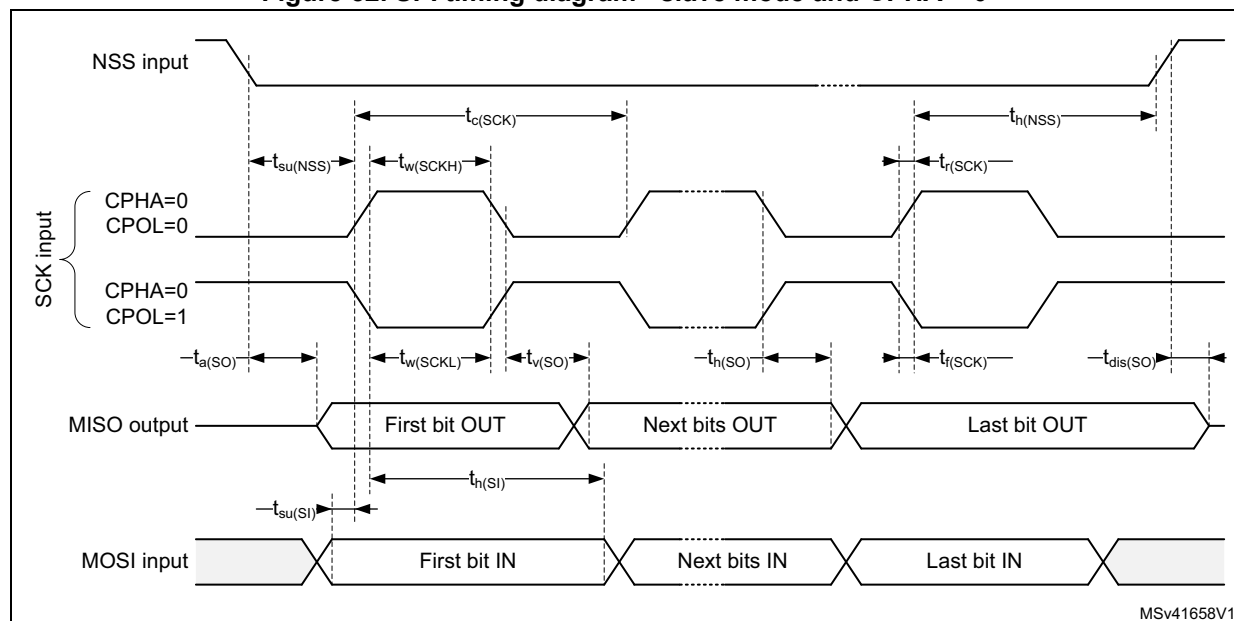
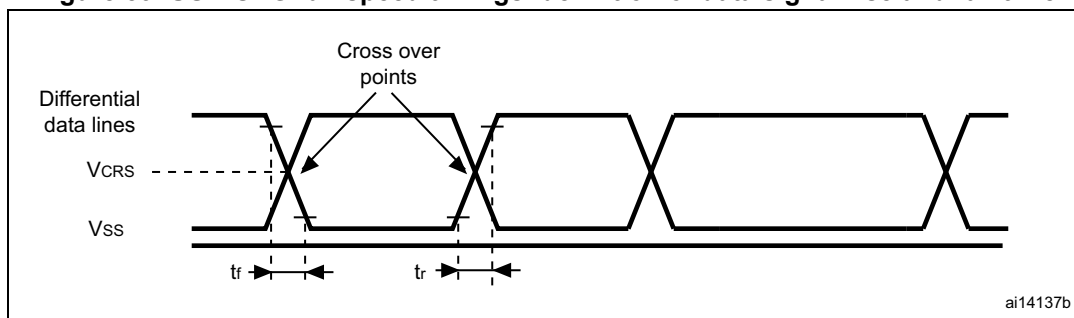


Figure 59. USB OTG full speed timings: definition of data signal rise and fall time**Table 87. USB OTG full speed electrical characteristics⁽¹⁾**

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50 \text{ pF}$	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V
Z_{DRV}	Output driver impedance ⁽³⁾	Driving high or low	28	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

USB high speed (HS) characteristics (through ULPI in STM32F722xx devices)

Unless otherwise specified, the parameters given in [Table 90](#) for ULPI are derived from tests performed under the ambient temperature, f_{HCLK} frequency summarized in [Table 89](#) and V_{DD} supply voltage conditions summarized in [Table 88](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 11$, unless otherwise specified
- Capacitive load $C = 20 \text{ pF}$, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to [Section 5.3.20: I/O port characteristics](#) for more details on the input/output characteristics.

Table 88. USB HS DC electrical characteristics

Symbol	Parameter	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input level V_{DD}	USB OTG HS operating voltage	1.7	3.6	V

1. All the voltages are measured from the local ground potential.

1. Guaranteed by characterization results.

Table 101. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9Thclk - 1	9Thclk + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	7Thclk - 0.5	7Thclk + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	6Thclk + 2	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4Thclk - 1	-	

1. Guaranteed by characterization results.

Synchronous waveforms and timings

[Figure 65](#) through [Figure 68](#) represent synchronous waveforms and [Table 102](#) through [Table 105](#) provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM
- CL = 30 pF on data and address lines. CL = 10 pF on FMC_CLK unless otherwise specified.

In all timing tables, the T_{HCLK} is the HCLK clock period.

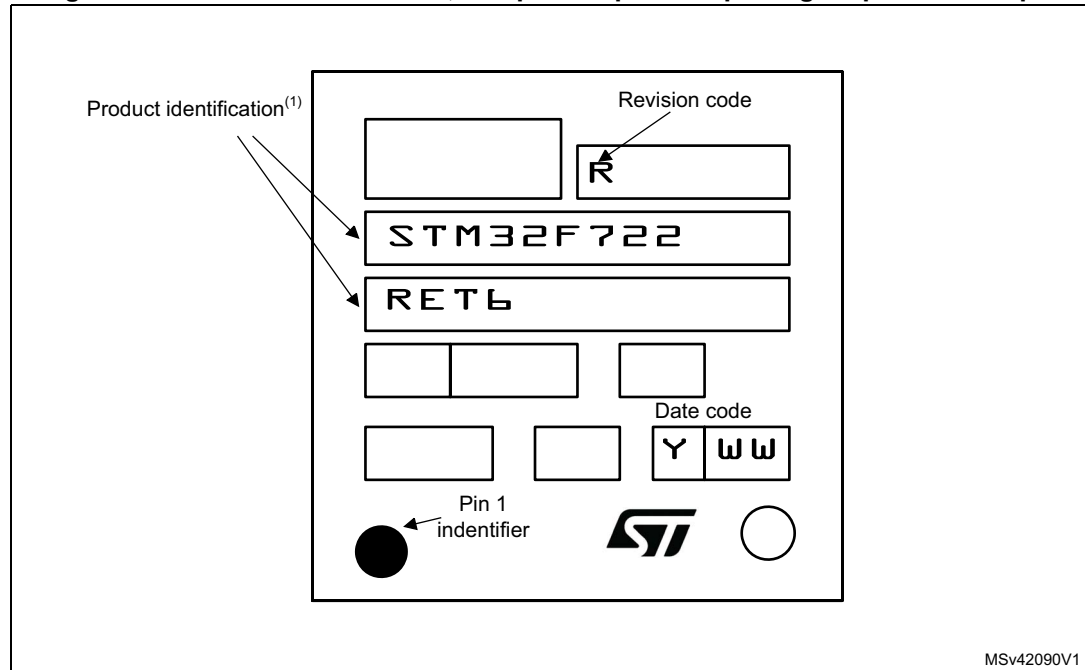
- For $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, maximum FMC_CLK = 108 MHz at CL=20 pF or 90 MHz at CL=30 pF (on FMC_CLK).
- For $1.71\text{ V} \leq V_{DD} < 2.7\text{ V}$, maximum FMC_CLK = 70 MHz at CL=10 pF (on FMC_CLK).

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

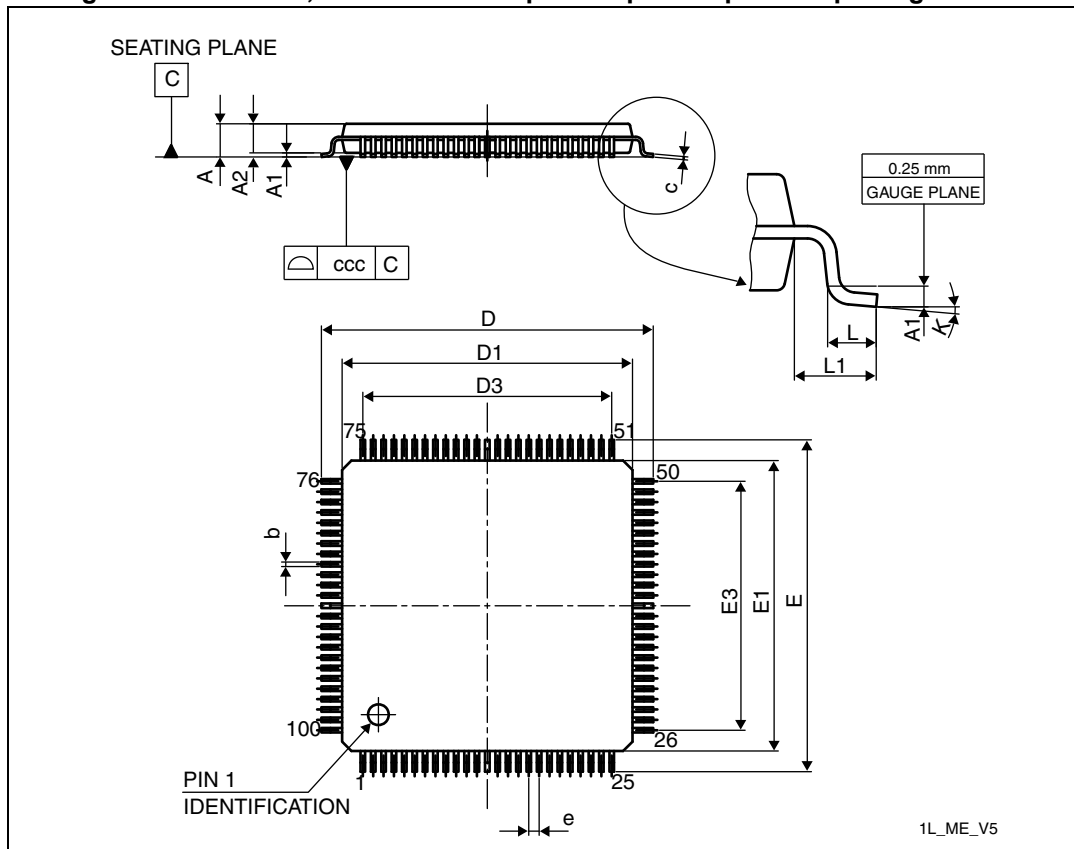
Figure 81. LQFP64 – 10 x 10 mm, low-profile quad flat package top view example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.2 LQFP100, 14 x 14 mm low-profile quad flat package information

Figure 82. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



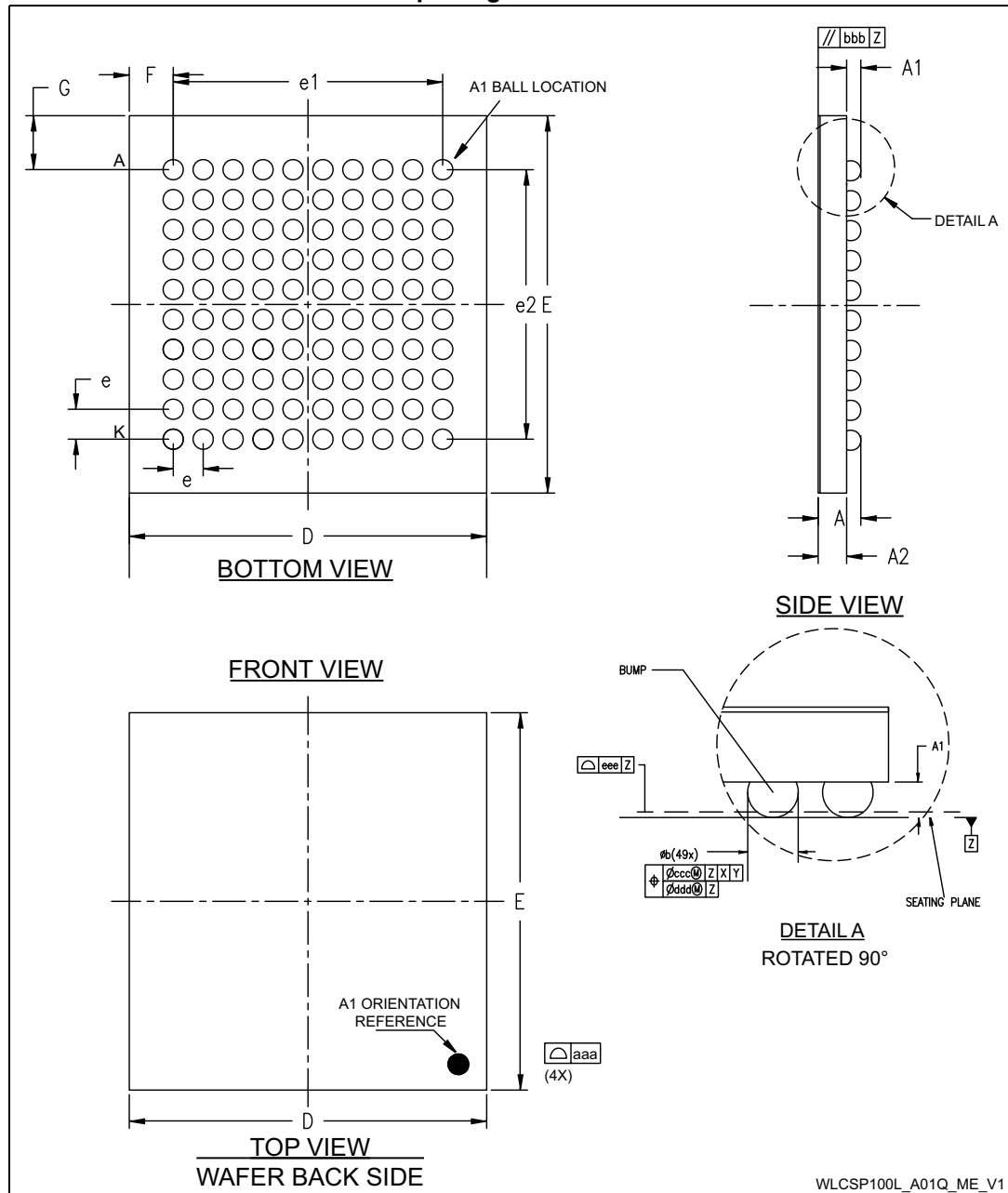
1. Drawing is not to scale.

Table 117. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

6.7 WLCSP100 - 0.4 mm pitch wafer level chip scale package information

Figure 97.WLCSP100 – 100L, 4.166 x 4.628 mm 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

7 Ordering information

Table 127. Ordering information scheme

Example:	STM32	F	722	V	C	T	6	xxx
Device family								
STM32 = ARM-based 32-bit microcontroller								
Product type								
F = general-purpose								
Device subfamily								
722 = STM32F722xx, no OTG PHY HS 723 = STM32F723xx, with OTG PHY HS								
Pin count								
R = 64 pins V = 100 pins Z = 144 pins I = 176 pins								
Flash memory size								
C = 256 Kbytes of Flash memory E = 512 Kbytes of Flash memory								
Package								
T = LQFP K = UFBGA (10 x 10 mm) I = UFBGA (7 x 7 mm) Y = WLCSP								
Temperature range								
6 = Industrial temperature range, −40 to 85 °C. 7 = Industrial temperature range, −40 to 105 °C.								
Options								
xxx = programmed parts TR = tape and reel								

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact the nearest ST sales office.