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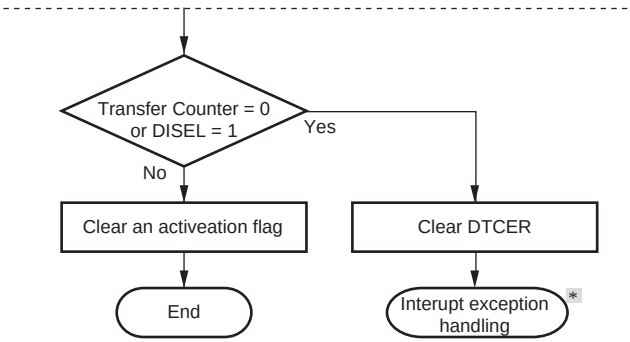
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2265fa13v

Item	Page	Revision (See Manual for Details)
5.6.5 IRQ Interrupt	102	5.6.5 added
5.6.6 NMI Interrupt Usage Notes	102	5.6.6 added
6.3.4 Operation in Transitions to Power-Down Modes	107	Description deleted • When the SLEEP instruction causes a transition from high speed mode to subactive mode (figure 6.2 (B)).
8.2.5 DTC Transfer Count Register A (CRA)	119	Description amended In repeat mode or block transfer mode, the CRA is divided into two parts: the upper 8 bits (CRAH) and the lower 8 bits (CRAL). In repeat mode, CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). In block transfer mode, CRAH holds the block size while CRAL functions as an 8-bit block size counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00. This operation is repeated.
8.5 Operation Figure 8.5 Flowchart of DTC Operation	127	Figure amended  Note: * For details, see section related to each peripheral module.
9.1.1 Port 1 Data Direction Register (P1DDR)	145	Description added P1DDR specifies input or output of the port 1 pins using the individual bits. P1DDR cannot be read; if it is, an undefined value will be read. The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Section 2 CPU

The H8S/2000 CPU is a high-speed central processing unit with an internal 32-bit architecture that is upward-compatible with the H8/300 and H8/300H CPUs. The H8S/2000 CPU has sixteen 16-bit general registers, can address a 16-Mbyte linear address space, and is ideal for realtime control. This section describes the H8S/2000 CPU. The usable modes and address spaces differ depending on the product. For details on each product, refer to section 3, MCU Operating Modes.

2.1 Features

- Upward-compatible with H8/300 and H8/300H CPU
  - Can execute H8/300 and H8/300H CPU object programs
- General-register architecture
  - Sixteen 16-bit general registers also usable as sixteen 8-bit registers or eight 32-bit registers
- Sixty-five basic instructions
  - 8/16/32-bit arithmetic and logic instructions
  - Multiply and divide instructions
  - Powerful bit-manipulation instructions
- Eight addressing modes
  - Register direct [Rn]
  - Register indirect [@ERn]
  - Register indirect with displacement [@(d:16,ERn) or @(d:32,ERn)]
  - Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]
  - Absolute address [@aa:8, @aa:16, @aa:24, or @aa:32]
  - Immediate [#xx:8, #xx:16, or #xx:32]
  - Program-counter relative [@(d:8,PC) or @(d:16,PC)]
  - Memory indirect [@@aa:8]
- 16-Mbyte address space
  - Program: 16 Mbytes
  - Data: 16 Mbytes
- High-speed operation
  - All frequently-used instructions execute in one or two states
  - 8/16/32-bit register-register add/subtract: 1 state
  - 8 × 8-bit register-register multiply: 12 states
  - 16 ÷ 8-bit register-register divide: 12 states

3.4 Address Map

Figure 3.1 shows the address map in each operating mode.

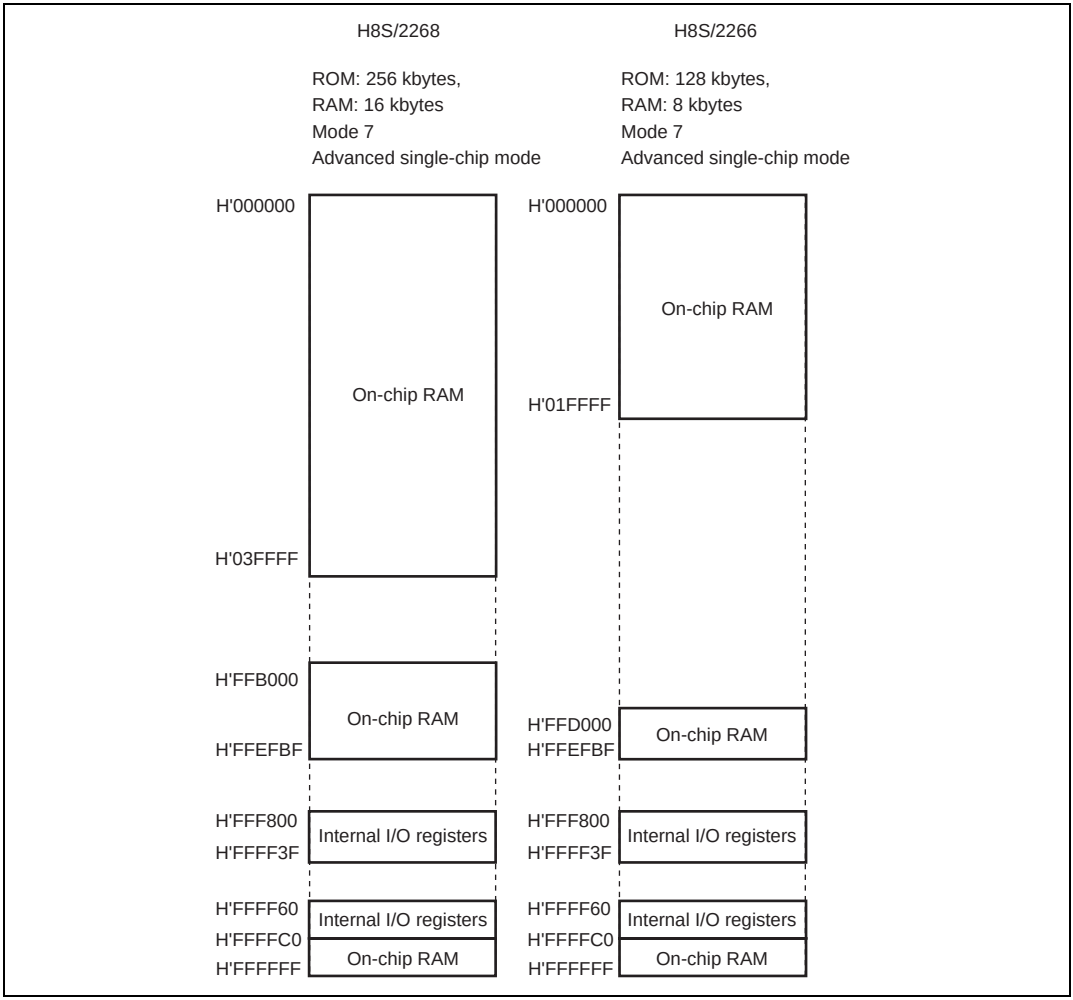


Figure 3.1 Address Map (1)

6.4.6 I Bit Set by LDC, ANDC, ORC, or XORC Instruction

When the I bit is set by an LDC, ANDC, ORC, or XORC instruction, a PC break interrupt becomes valid two states after the end of the executing instruction. If a PC break interrupt is set for the instruction following one of these instructions, since interrupts, including NMI, are disabled for a 3-state period in the case of LDC, ANDC, ORC, and XOR, the next instruction is always executed. For details, see section 5, Interrupt Controller.

6.4.7 PC Break Set for Instruction Fetch at Address Following Bcc Instruction

When a PC break is set for an instruction fetch at an address following a Bcc instruction:

A PC break interrupt is generated if the instruction at the next address is executed in accordance with the branch condition, and is not generated if the instruction at the next address is not executed.

6.4.8 PC Break Set for Instruction Fetch at Branch Destination Address of Bcc Instruction

When a PC break is set for an instruction fetch at the branch destination address of a Bcc instruction:

A PC break interrupt is generated if the instruction at the branch destination is executed in accordance with the branch condition, and is not generated if the instruction at the branch destination is not executed.

Table 8.3 Register Information in Normal Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register A	CRA	Designates transfer count
DTC transfer count register B	CRB	Not used

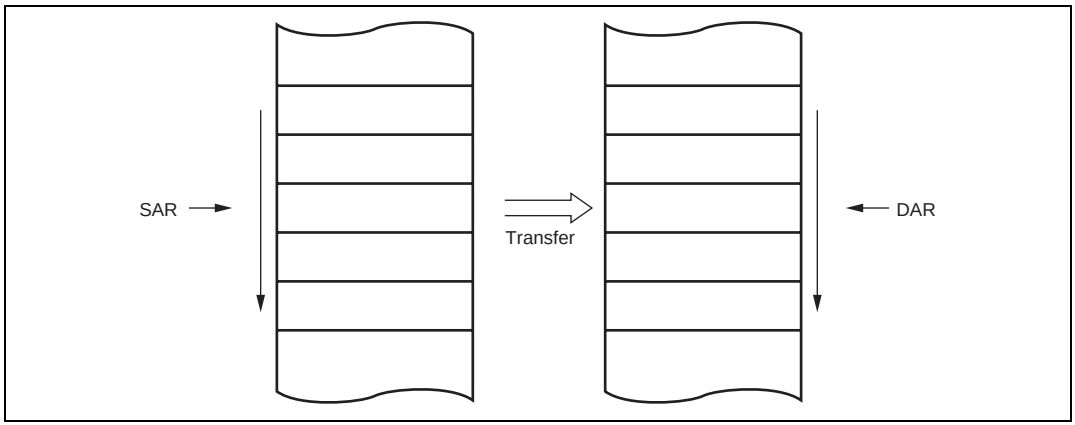


Figure 8.6 Memory Mapping in Normal Mode

8.5.2 Repeat Mode

In repeat mode, one operation transfers one byte or one word of data.

From 1 to 256 transfers can be specified. Once the specified number of transfers have ended, the initial state of the transfer counter and the address register specified as the repeat area is restored, and transfer is repeated. In repeat mode the transfer counter value does not reach H'00, and therefore CPU interrupts cannot be requested when DISEL = 0.

Table 8.4 lists the register information in repeat mode. Figure 8.7 shows the memory mapping in repeat mode.

- PH0/COM1

  The pin function is switched as shown below according to the combination of the SGS3 to SGS0 bits in LPCR of the LCD controller/driver and the PH0DDR bit.

SGS3 to SGS0	B'0000		H8S/2268 Group: B'0001, B'001X or B'010X H8S/2264 Group: B'001X or B'010X
PH0DDR	0	1	—
Pin functions	PH0 input pin	PH0 output pin	COM1 output pin

Legend:
X: Don't care

9.8 Port J

Port J is an 8-bit I/O port and has the following registers.

- Port J data direction register (PJDDR)
- Port J data register (PJDR)
- Port J register (PORTJ)
- Port J pull-up MOS control register (PJPCR)
- Wakeup control register (WPCR)

9.9.3 Port K Register (PORTK)

PORTK shows port K pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PK7	—*	R	If a port K read is performed while PKDDR bits are set to 1, the PKDR values are read. If a port K read is performed while PKDDR bits are cleared to 0, the pin states are read.
6	PK6	—*	R	
5	PK5	—*	R	
4	PK4	—*	R	
3	PK3	—*	R	
2	PK2	—*	R	
1	PK1	—*	R	
0	PK0	—*	R	

Note: * Determined by the states of pins PK7 to PK0.

9.9.4 Pin Functions

Port K pins also function as LCD driver segment output pins (SEG16 to SEG9). Port K pin functions are shown below.

- PKn/SEGn + 9

  The pin function is switched as shown below according to the combination of the SGS3 to SGS0 bits in LPCR of the LCD driver/controller and PKnDDR bit.

SGS3 to SGS0	H8S/2268 Group: B'00XX H8S/2264 Group: B'0000 or B'001X		B'010X
PKnDDR	0	1	—
Pin functions	PKn input pin	PKn output pin	SEGn + 9 output pin

Legend:
X: Don't care
Note: n = 7 to 0

10.2 Input/Output Pins

Table 10.2 TPU Pins

Channel	Symbol	I/O	Function
All	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input*)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input*)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input*)
	TCLKD*	Input	External clock D input pin (Channel 2 phase counting mode B phase input*)
0*	TIOCA0	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOCB0	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOCC0	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOCD0	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	I/O	TGRB_2 input capture input/output compare output/PWM output pin

Note: * Supported only by the H8S/2268 Group.

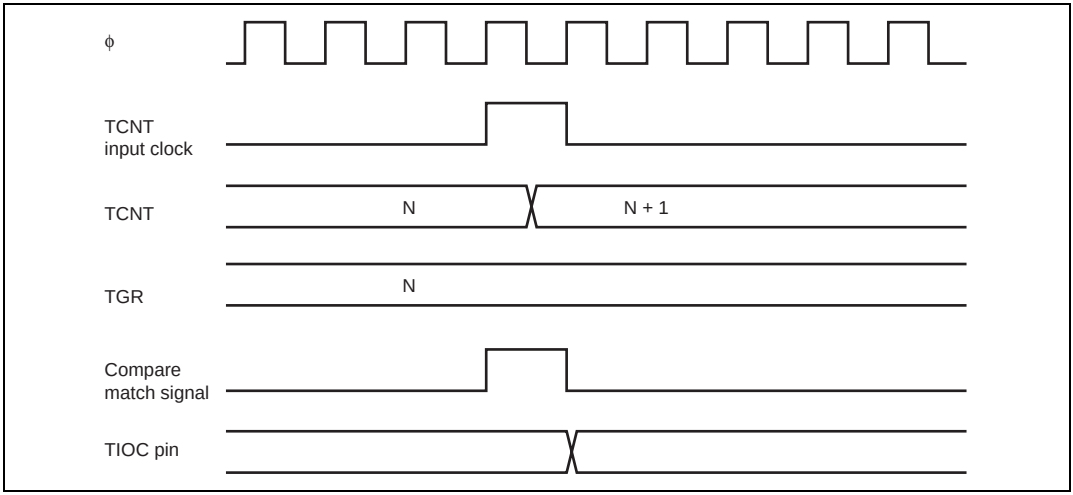


Figure 10.33 Output Compare Output Timing

Input Capture Signal Timing: Figure 10.34 shows input capture signal timing.

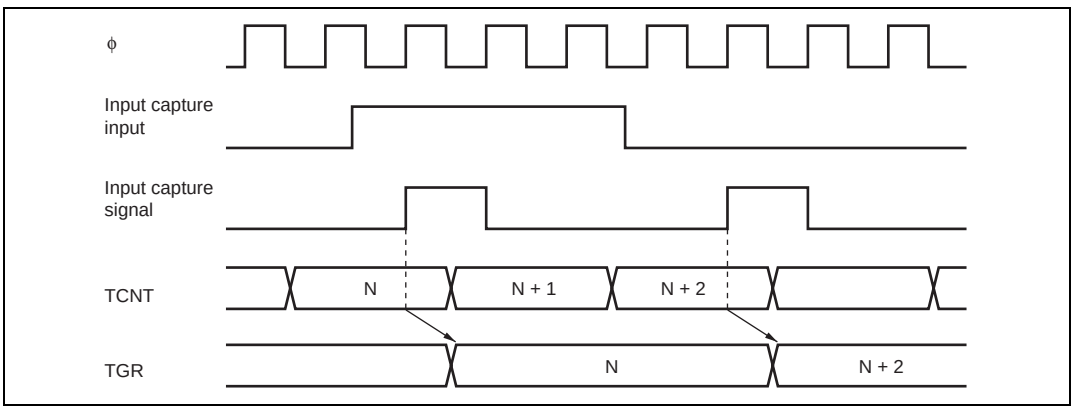


Figure 10.34 Input Capture Input Signal Timing

11.4 Operation

11.4.1 Pulse Output

Figure 11.2 shows an example of arbitrary duty pulse output.

1. Set TCR in CCR1 to 0 and CCLR0 to 1 to clear TCNT by a TCORA compare-match.
2. Set OS3 to OS0 bits in TCSR to B'0110 to output 1 by a TCORA compare-match and 0 by a TCORB compare-match.

By the above settings, waveforms with the cycle of TCORA and the pulse width of TCORB can be output without software intervention.

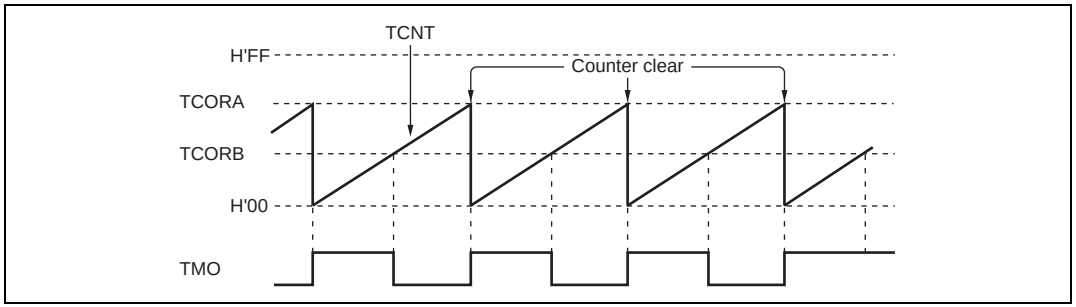


Figure 11.2 Example of Pulse Output

(2) Writing to RSTCSR

Use word transfer operations to write to RSTCSR. This register cannot be written using byte transfer instructions. This is shown in figure 12.8.

The method used to write a 0 to the WOVF bit and the method used to write the RSTE and RSTS bits are different.

To write a 0 to the WOVF bit, set the upper byte to H'A5 and the lower byte to H'00 and transfer that data. This will clear the WOVF bit to 0. This operation does not affect the RSTE and RSTS bits. To write the RSTE and RSTS bits, set the upper byte to H'5A and the lower byte to the data to be written and transfer that data. This will write the data in bits 6 and 5 of the lower byte to the RSTE and RSTS bits. This operation does not affect the WOVF bit.

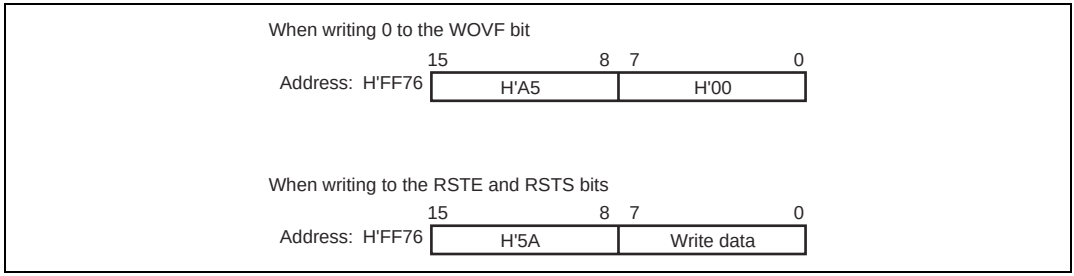


Figure 12.8 Writing to RSTCSR

(3) Reading TCNT, TCSR, and RSTCSR (WDT_0)

These registers are read in the same way as other registers. The read addresses are H'FF74 for TCSR and H'FF77 for RSTCSR.

12.5.2 Contention between Timer Counter (TCNT) Write and Increment

If a timer counter clock pulse is generated during the T2 state of a TCNT write cycle, the write takes priority and the timer counter is not incremented. Figure 12.9 shows this operation.

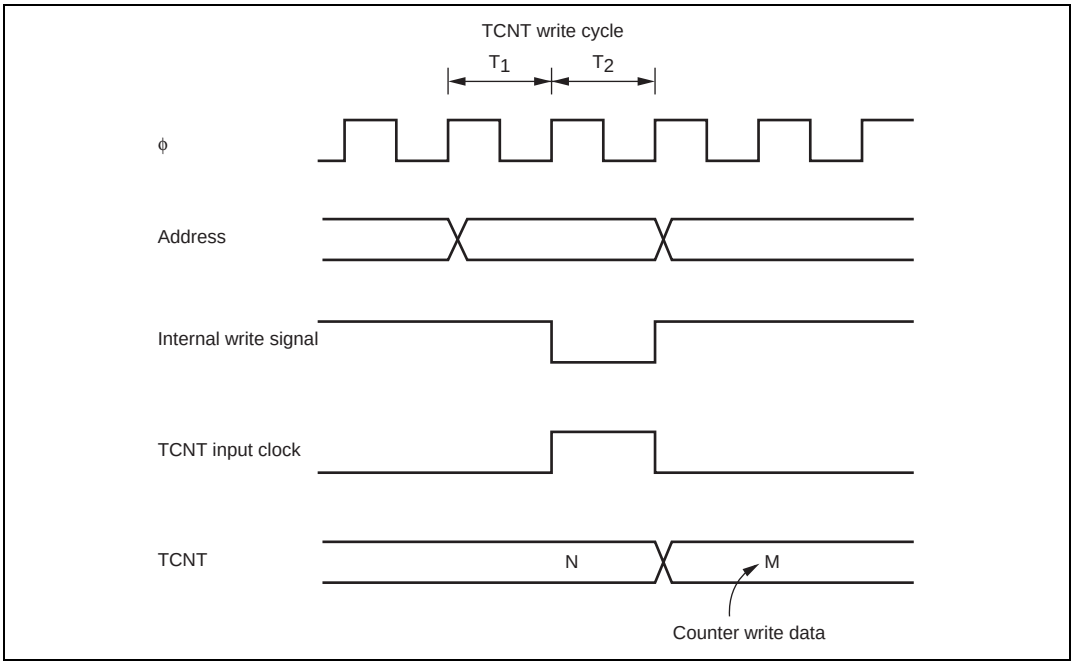


Figure 12.9 Contention between TCNT Write and Increment

12.5.3 Changing Value of CKS2 to CKS0

If bits CKS0 to CKS2 in TCSR are written to while the WDT is operating, errors could occur in the incrementation. Software must be used to stop the watchdog timer (by clearing the TME bit to 0) before changing the value of bits CKS0 to CKS2.

12.5.4 Switching between Watchdog Timer Mode and Interval Timer Mode

If the mode is switched from watchdog timer to interval timer while the WDT is operating, errors could occur in the incrementation. Software must be used to stop the watchdog timer (by clearing the TME bit to 0) before switching the mode.

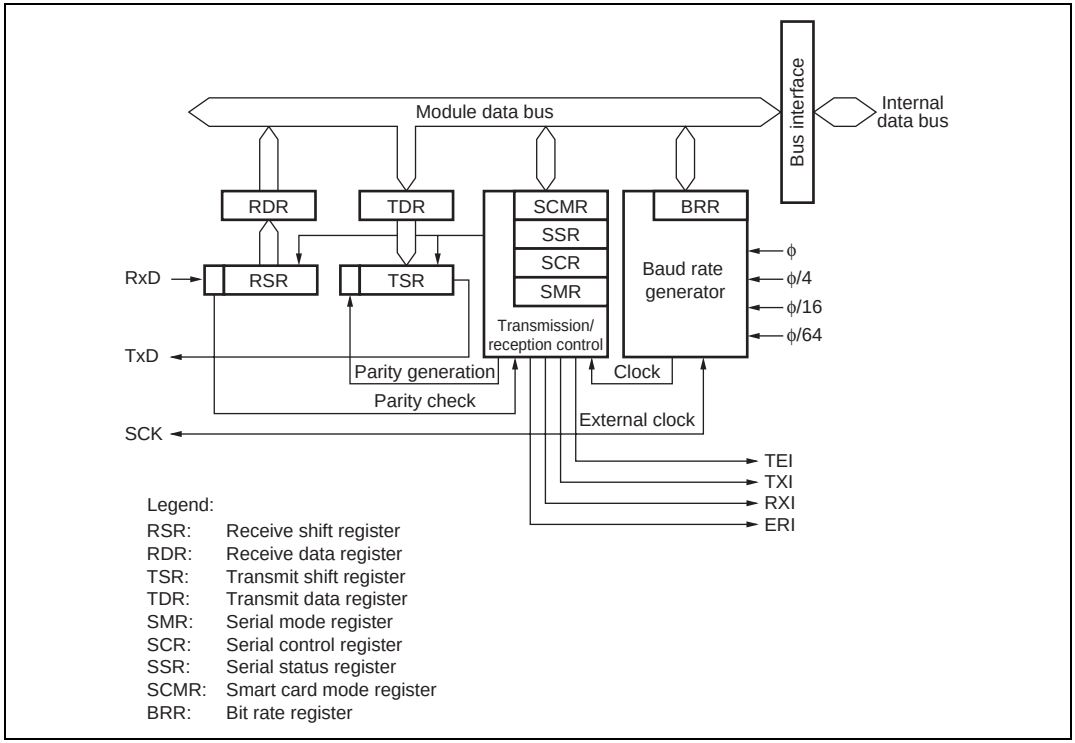


Figure 13.2 Block Diagram of SCI_1 or SCI_2

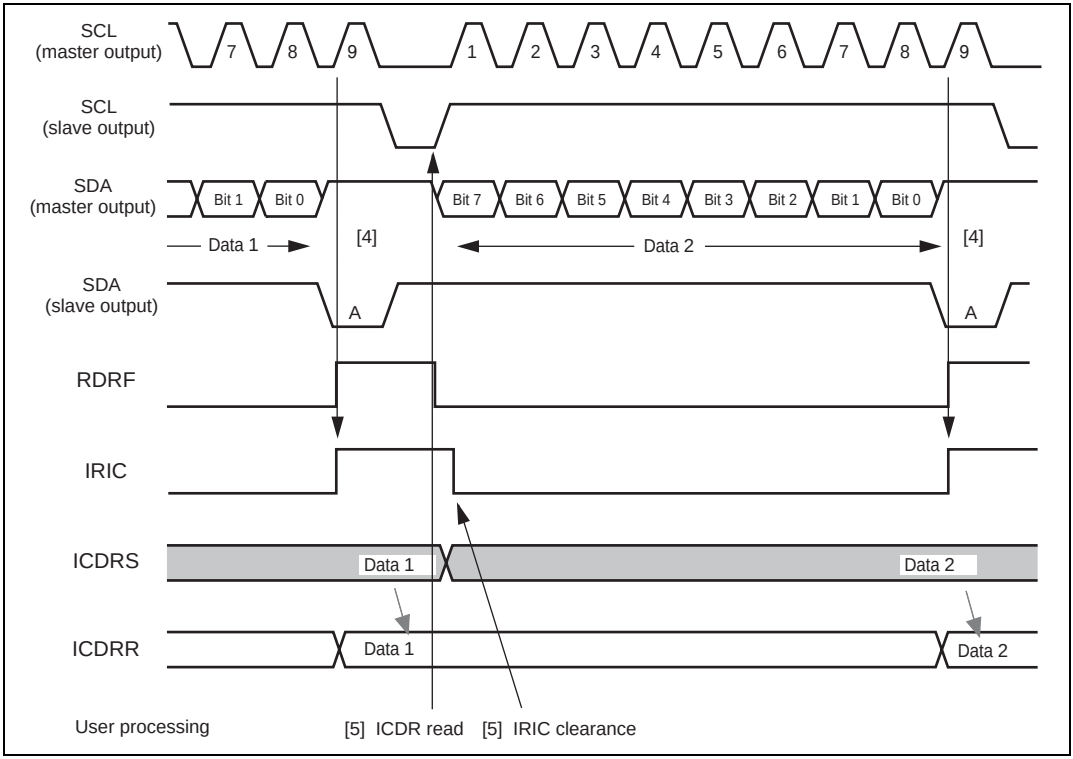


Figure 14.16 Example of Slave Receive Mode Operation Timing (2) (MLS = ACKB = 0)

14.4.9 Noise Canceler

The logic levels at the SCL and SDA pins are routed through noise cancellors before being latched internally. Figure 14.20 shows a block diagram of the noise cancelled circuit.

The noise cancellor consists of two cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on the system clock, but is not passed forward to the next circuit unless the outputs of both latches agree. If they do not agree, the previous value is held.

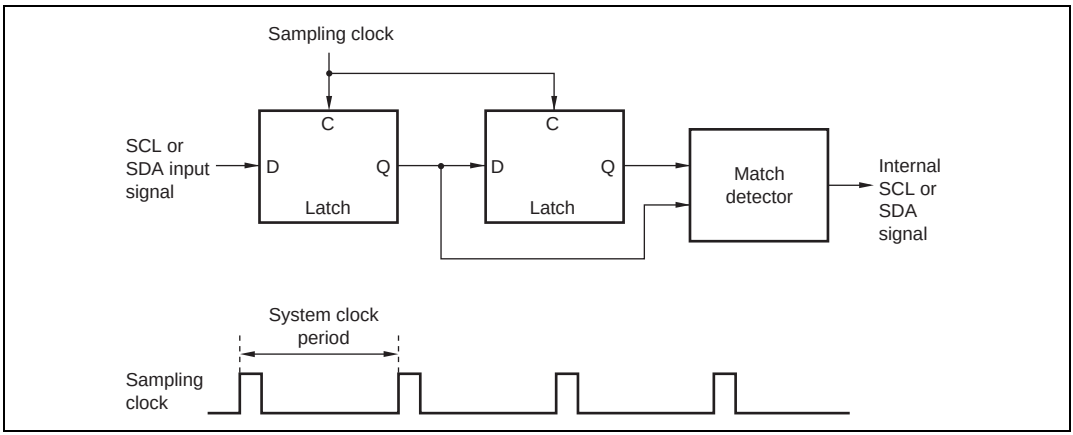


Figure 14.20 Block Diagram of Noise Cancellor

14.4.10 Initialization of Internal State

The IIC has a function for forcible initialization of its internal state if a deadlock occurs during communication.

Initialization is executed by (1) setting bits CLR3 to CLR0 in the DDCSWR register or (2) clearing the ICE bit. For details of settings for bits CLR3 to CLR0, see section 14.3.8, DDC Switch Register (DDCSWR).

Scope of Initialization: The initialization executed by this function covers the following items:

- TDRE and RDRF internal flags
- Transmit/receive sequencer and internal operating clock counter
- Internal latches for retaining the output state of the SCL and SDA pins (wait, clock, data output, etc.)

Section 18 DTMF Generation Circuit

The H8S/2268 Group contains a Dual-Tone Multi-Frequency generation circuit to generate DTMF signals. It is not contained in the H8S/2264 Group.

The DTMF signal consists of two types of sine waveforms and is used to access a switch device. The function of the DTMF signal is shown in the frequency matrix in figure 18.1. The DTMF generation circuit produces the frequencies corresponding to the numbers and symbols in the figure.

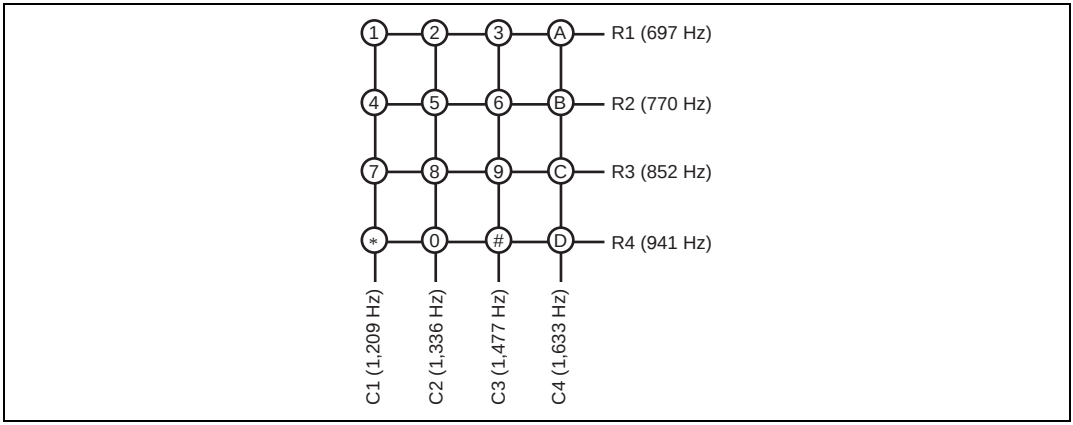


Figure 18.1 DTMF Frequencies

18.1 Features

- Generating DTMF frequency sine waveform from the system clock (ϕ)
  The system clock (2.0 to 20.4 MHz, with 400-kHz steps) is divided to produce a 400-kHz clock signal. This clock signal is then supplied to the feedback loop, comprised of a variant program divider and sine waveform counter to generate a DTMF frequency sine waveform.
- Producing low distortion, stable sine waveforms
  Sine waveforms signals are output from the high-precision resistor rudder-type D/A converter. In addition, one cycle is divided into 32, resulting in low-distortion stable signal waveforms.
- Synthesis or single waveform output selectable
  Synthesized row and column output, row output, or column output are selectable.
- Module stop mode can be set.

Figure 18.2 shows the block diagram for the DTMF generation circuit.

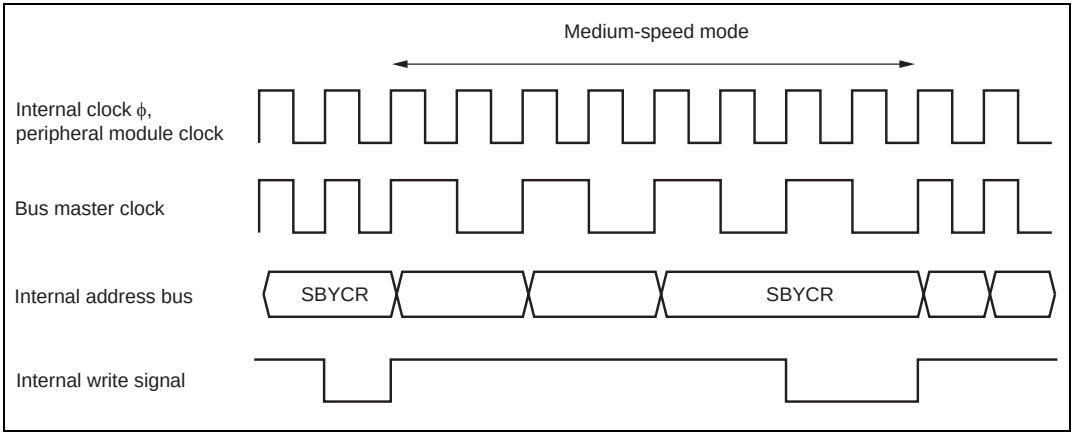


Figure 22.2 Medium-Speed Mode Transition and Clearance Timing

22.3 Sleep Mode

22.3.1 Sleep Mode

When the SLEEP instruction is executed while the SBYCR SSBY bit = 0 and the LPWRCR LSON bit = 0, the CPU enters the sleep mode. In sleep mode, CPU operation stops but the contents of the CPU's internal registers are retained. Other peripheral modules do not stop.

22.3.2 Exiting Sleep Mode

Sleep mode is exited by any interrupt, or signals at the $\overline{\text{RES}}$, or $\overline{\text{STBY}}$ pins.

- Exiting Sleep Mode by Interrupts

  When an interrupt occurs, sleep mode is exited and interrupt exception processing starts. Sleep mode is not exited if the interrupt is disabled, or interrupts other than NMI are masked by the CPU.
- Exiting Sleep Mode by $\overline{\text{RES}}$ pin

  Setting the $\overline{\text{RES}}$ pin level low selects the reset state. After the stipulated reset input duration, driving the $\overline{\text{RES}}$ pin high starts the CPU performing reset exception processing.
- Exiting Sleep Mode by $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

22.9 Sub-Active Mode

22.9.1 Transition to Sub-Active Mode

When the SLEEP instruction is executed in high-speed mode with the SBYCR SSBY bit = 1, LPWRCR DTON bit = 1, LSON bit = 1, and TCSR_1 (WDT_1) PSS bit = 1, CPU operation shifts to sub-active mode. When an interrupt occurs in watch mode, and if the LSON bit of LPWRCR is 1, a transition is made to sub-active mode. And if an interrupt occurs in sub-sleep mode, a transition is made to sub-active mode.

In sub-active mode, the CPU operates at low speed on the subclock, and the program is executed step by step. Peripheral modules other than PBC*, TMR_0, TMR_1, TMR_2 to TMR_4*, WDT_0, WDT_1, and LCD are also stopped.

When operating the CPU in sub-active mode, the SCKCR SCK2 to SCK0 bits must be set to 0.

Note: * Supported only by the H8S/2268 Group.

22.9.2 Exiting Sub-Active Mode

Sub-active mode is exited by the SLEEP instruction or the $\overline{\text{RES}}$ or $\overline{\text{STBY}}$ pins.

- Exiting Sub-Active Mode by SLEEP Instruction

  When the SLEEP instruction is executed with the SBYCR SSBY bit = 1, LPWRCR DTON bit = 0, and TCSR_1 (WDT_1) PSS bit = 1, the CPU exits sub-active mode and a transition is made to watch mode. When the SLEEP instruction is executed with the SBYCR SSBY bit = 0, LPWRCR LSON bit = 1, and TCSR (WDT_1) PSS bit = 1, a transition is made to sub-sleep mode. Finally, when the SLEEP instruction is executed with the SBYCR SSBY bit = 1, LPWRCR DTON bit = 1, LSON bit = 0, and TCSR (WDT_1) PSS bit = 1, a direct transition is made to high-speed mode (SCK0 to SCK2 all 0).
- Exiting Sub-Active Mode by $\overline{\text{RES}}$ Pins

  For exiting sub-active mode by the $\overline{\text{RES}}$ pins, see section 22.4.2, Clearing Software Standby Mode.
- Exiting Sub-Active Mode by $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

Table 25.15 DC Characteristics (2)

Condition D (Masked-ROM version): V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$, $\overline{IRQ4}$, $\overline{WKP0}$ to $\overline{WKP7}$	VT^-	V_{CC} × 0.2	—	—	V	
		VT^+	—	—	V_{CC} × 0.8	V	
		$VT^+ - VT^-$	V_{CC} × 0.05	—	—	V	
Input high voltage	$\overline{RES}$, $\overline{STBY}$,NMI, FWE, MD2, MD1	V_{IH}	V_{CC} × 0.9	—	V_{CC} + 0.3	V	
	EXTAL, Ports 1, 3, 7, F, H, J to L		V_{CC} × 0.8	—	V_{CC} + 0.3	V	
	Ports 4*4, 9		V_{CC} × 0.8	—	AV_{CC} + 0.3*4	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$,FWE, MD2, MD1	V_{IL}	- 0.3	—	V_{CC} × 0.1	V	
	NMI, EXTAL, Ports 1, 3, 4, 7, 9, F, H, J to L		- 0.3	—	V_{CC} × 0.2	V	
Output high voltage	All output pins except P34 and P35	V_{OH}	V_{CC} - 0.5	—	—	V	I_{OH} = - 200 μA
			V_{CC} - 1.0	—	—	V	I_{OH} = - 1 mA
	P34 and P35*2		V_{CC} - 2.7	—	—	V	I_{OH} = - 100 μA
Output low voltage	All output pins*3	V_{OL}	—	—	0.4	V	I_{OL} = 0.8 mA
	Port 7		—	—	1.0	V	I_{OL} = 10 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0.5 to V_{CC} - 0.5 V
	$\overline{STBY}$, NMI, FWE, MD2, MD1		—	—	1.0	μA	
	Ports 4, 9		—	—	1.0	μA	V_{in} = 0.5 to AV_{CC} - 0.5 V
	PH7		—	—	1.0	μA	V_{in} = 0.5 to V_{CC} - 0.5 V
Three-state leakage current (off state)	Ports 1, 3, 7, F, J to L, PH0 to PH3	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0.5 to V_{CC} - 0.5 V
Input pull-up MOS current	Port J	$-I_P$	50	—	300	μA	V_{in} = 0 V

Product Type			Product Code	Mark Code	Package (Renesas Package Code)	Operating Voltage
H8S/2262	Masked-ROM version	Version with on-chip I^2C bus interface	HD6432262W	HD6432262W(A**)TF	100-pin TQFP (TFP-100G, TFP-100GV)	2.7 V to 5.5 V
				HD6432262W(A**)FA	100-pin QFP (FP-100B, FP-100BV)	
				HD6432262W(F**)TF	100-pin TQFP (TFP-100G, TFP-100GV)	4.0 V to 5.5 V
				HD6432262W(F**)FA	100-pin QFP (FP-100B, FP-100BV)	

Legend:

(A**), (F**): ROM code

Note: Some products above are in the developing or planning stage. Please contact Renesas agency to confirm the present state of each product.