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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2265fa20v

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Section 1 Overview

1.1 Features

- High-speed H8S/2000 central processing unit with an internal 16-bit architecture
  - Upward-compatible with H8/300 and H8/300H CPUs on an object level
  - Sixteen 16-bit general registers
  - 65 basic instructions
- Various peripheral functions
  - Interrupt controller
  - PC break controller (supported only by the H8S/2268 Group)
  - Data transfer controller (DTC) (supported only by the H8S/2268 Group)
  - 16-bit timer-pulse unit (TPU)
  - 8-bit timer (TMR)
  - Watchdog timer (WDT)
  - Serial communication interface (SCI)
  - I^2C bus interface (IIC) (supported as an option by H8S/2264 Group)
  - A/D converter
  - D/A converter (supported only by the H8S/2268 Group)
  - LCD controller/driver
  - DTMF generation circuit (supported only by the H8S/2268 Group)
- On-chip memory

  H8S/2268 Group:

ROM	Model	ROM	RAM	Remarks
Flash memory version	HD64F2268	256 kbytes	16 kbytes	
	HD64F2266	128 kbytes	8 kbytes	
	HD64F2265	128 kbytes	4 kbytes	

  H8S/2264 Group:

ROM	Model	ROM	RAM	Remarks
Masked ROM version	HD6432264	128 kbytes	4 kbytes	
	HD6432264W	128 kbytes	4 kbytes	
	HD6432262	64 kbytes	2 kbytes	
	HD6432262W	64 kbytes	2 kbytes	

Table 2.11 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:32,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24/@aa:32
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

2.7.1 Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

2.7.2 Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn) which contains the address of the operand on memory. If the address is a program instruction address, the lower 24 bits are valid and the upper 8 bits are all assumed to be 0 (H'00).

2.7.3 Register Indirect with Displacement—@(d:16, ERn) or @(d:32, ERn)

A 16-bit or 32-bit displacement contained in the instruction is added to an address register (ERn) specified by the register field of the instruction, and the sum gives the address of a memory operand. A 16-bit displacement is sign-extended when added.

Section 4 Exception Handling

4.1 Exception Handling Types and Priority

As table 4.1 indicates, exception handling may be caused by a reset, trace*, trap instruction, or interrupt. Exception handling is prioritized as shown in table 4.1. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Trap instruction exception handling requests are accepted at all times in program execution state.

Exception sources, the stack structure, and operation of the CPU vary depending on the interrupt control mode set by the INTM0 and INTM1 bits in SYSCR.

Table 4.1 Exception Types and Priority

Priority	Exception Type	Start of Exception Handling
High ↑ Low	Reset	Starts immediately after a low-to-high transition at the $\overline{\text{RES}}$ pin, or when the watchdog timer overflows. The CPU enters the reset state when the $\overline{\text{RES}}$ pin is low.
	Trace*	Starts when execution of the current instruction or exception handling ends, if the trace (T) bit in the EXR is set to 1. Traces are enabled only in interrupt control mode 2. Trace exception handling is not executed after execution of an RTE instruction.
	Interrupt	Starts when execution of the current instruction or exception handling ends, if an interrupt request has been issued. Interrupt detection is not performed on completion of ANDC, ORC, XORC, or LDC instruction execution, or on completion of reset exception handling.
	Trap instruction	Started by execution of a trap instruction (TRAPA). Trap instruction exception handling requests are accepted at all times in program execution state.

Note: * Supported only by the H8S/2268 Group.

Table 5.9 Interrupt Source Selection and Clear Control

Settings		Interrupt Source Selection and Clear Control	
DTC			
DTCE	DESEL	DTC	CPU
0	*	X	#
1	0	#	X
	1	O	#

Legend:

#: Corresponding interrupt is used. Interrupt source is cleared.
(The CPU should clear the source flag in the interrupt processing routine.)

O: Corresponding interrupt is used. Interrupt source is not cleared.

X: Corresponding interrupt cannot be used.

*: Don't care

Usage note: Interrupt sources of the SCI and A/D converter are cleared when the DTC reads or writes prescribed register, and they do not depend on the DTCE or DISEL bit.

5.6 Usage Notes

5.6.1 Contention between Interrupt Generation and Disabling

When an interrupt enable bit is cleared to 0 to disable interrupt requests, the disabling becomes effective after execution of the instruction.

When an interrupt enable bit is cleared to 0 by an instruction such as BCLR or MOV, and if an interrupt is generated during execution of the instruction, the interrupt concerned will still be enabled on completion of the instruction, and so interrupt exception handling for that interrupt will be executed on completion of the instruction. However, if there is an interrupt request of higher priority than that interrupt, interrupt exception handling will be executed for the higher-priority interrupt, and the lower-priority interrupt will be ignored.

The same also applies when an interrupt source flag is cleared to 0.

Figure 5.13 shows an example in which the CMIEA bit in the TCR register of the 8-bit timer is cleared to 0.

The above contention will not occur if an enable bit or interrupt source flag is cleared to 0 while the interrupt is masked.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	—	Undefined	—	Reserved These bits have no effect on DTC operation. The write value should always be 0.

8.2.3 DTC Source Address Register (SAR)

SAR is a 24-bit register that designates the source address of data to be transferred by the DTC. For word-size transfer, specify an even source address.

8.2.4 DTC Destination Address Register (DAR)

DAR is a 24-bit register that designates the destination address of data to be transferred by the DTC. For word-size transfer, specify an even destination address.

8.2.5 DTC Transfer Count Register A (CRA)

CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC.

In normal mode, the entire CRA functions as a 16-bit transfer counter (1 to 65536). It is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

In repeat mode or block transfer mode, the CRA is divided into two parts: the upper 8 bits (CRAH) and the lower 8 bits (CRAL). In repeat mode, CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). In block transfer mode, CRAH holds the block size while CRAL functions as an 8-bit block size counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00. This operation is repeated.

8.2.6 DTC Transfer Count Register B (CRB)

CRB is a 16-bit register that designates the number of times data is to be transferred by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65536) that is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.

Port	Description	Port and Other Functions Name	Input/Output and Output Type
Port 9	General input port also functioning as A/D converter analog input and D/A converter analog output pins	P97/AN9/DA1	
		P96/AN8/DA0	
Port F	General I/O port also functioning as interrupt input pins and an A/D converter input pins	PF3/$\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$	Schmitt trigger input ($\overline{\text{IRQ3}}$)
Port H	General input port	PH7	
	General I/O port also functioning as LCD common output pins	PH3/COM4	
		PH2/COM3	
		PH1/COM2	
		PH0/COM1	
Port J	General I/O port also functioning as wakeup input pins and LCD segment output pins	PJ7/$\overline{\text{WKP7}}$/SEG8	Built-in input pull-up MOS Schmitt trigger input ($\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$)
		PJ6/$\overline{\text{WKP6}}$/SEG7	
		PJ5/$\overline{\text{WKP5}}$/SEG6	
		PJ4/$\overline{\text{WKP4}}$/SEG5	
		PJ3/$\overline{\text{WKP3}}$/SEG4	
		PJ2/$\overline{\text{WKP2}}$/SEG3	
		PJ1/$\overline{\text{WKP1}}$/SEG2	
		PJ0/$\overline{\text{WKP0}}$/SEG1	
Port K	General I/O port also functioning as LCD segment output pins	PK7/SEG16	
		PK6/SEG15	
		PK5/SEG14	
		PK4/SEG13	
		PK3/SEG12	
		PK2/SEG11	
		PK1/SEG10	
		PK0/SEG9	

TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag B (CMFB) in TCSR is set. Note, however, that comparison is disabled during the T2 state of a TCORB write cycle.

The timer output from the TMO pin can be freely controlled by the compare-match signal B and the settings of output select bits OS1 and OS0 in TCSR.

The initial value of TCORB is H'FF.

11.3.4 Timer Control Register (TCR)

TCR selects the TCNT clock source and the time at which TCNT is cleared, and controls interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare-Match Interrupt Enable B Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt request (CMIB) is disabled 1: CMFB interrupt request (CMIB) is enabled
6	CMIEA	0	R/W	Compare-Match Interrupt Enable A Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt request (CMIA) is disabled 1: CMFA interrupt request (CMIA) is enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether the OVF interrupt request (OVI) is enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt request (OVI) is disabled 1: OVF interrupt request (OVI) is enabled
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	0	R/W	These bits select the method by which TCNT is cleared 00: Clearing is disabled 01: Cleared on compare-match A 10: Cleared on compare-match B 11: Cleared on rising edge of external reset input

Bit	Bit Name	Initial Value	R/W	Description
5	OVF	0	R/(W)*1	Timer Overflow Flag [Setting condition] When TCNT overflows from H'FF to H'00 [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF
4	—	0	R/W	Reserved This bit is a readable/writable bit, but the write value should always be 0.
3	OS3	0	R/W	Output Select 3 and 2
2	OS2	0	R/W	These bits specify how the timer output level is to be changed by a compare-match B of TCORB and TCNT. 00: No change when compare-match B occurs 01: 0 is output when compare-match B occurs 10: 1 is output when compare-match B occurs 11: Output is inverted when compare-match B occurs (toggle output)
1	OS1	0	R/W	Output Select 1 and 0
0	OS0	0	R/W	These bits specify how the timer output level is to be changed by a compare-match A of TCORA and TCNT. 00: No change when compare-match A occurs 01: 0 is output when compare-match A occurs 10: 1 is output when compare-match A occurs 11: Output is inverted when compare-match A occurs (toggle output)

Notes: 1. Only 0 can be written to this bit, to clear the flag.
2. Supported only by the H8S/2268 Group.

12.2.3 Reset Control/Status Register (RSTCSR) (Only WDT_0)

RSTCSR controls the generation of the internal reset signal when TCNT overflows, and selects the type of internal reset signal. RSTCSR is initialized to H'1F by a reset signal from the $\overline{\text{RES}}$ pin, and not by the WDT internal reset signal caused by overflows.

Bit	Bit Name	Initial Value	R/W	Description
7	WOVF	0	R/(W)*	Watchdog Overflow Flag This bit is set when TCNT overflows in watchdog timer mode. This bit cannot be set in interval timer mode, and only 0 can be written, to clear the flag. [Setting condition] Set when TCNT overflows (changed from H'FF to H'00) in watchdog timer mode [Clearing condition] Cleared by reading RSTCSR when WOVF = 1, and then writing 0 to WOVF
6	RSTE	0	R/W	Reset Enable Specifies whether or not a reset signal is generated in the chip if TCNT overflows during watchdog timer operation. 0: Reset signal is not generated even if TCNT overflows (Though this LSI is not reset, TCNT and TCSR in WDT are reset) 1: Reset signal is generated if TCNT overflows
5	—	0	R/W	Reserved This bit can be read from and written to. However, the write value should always be 0.
4 to 0	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

Note: * Only 0 can be written, to clear the flag.

12.3.3 Timing of Setting Overflow Flag (OVF)

The OVF flag is set to 1 if TCNT overflows during interval timer operation. At the same time, an interval timer interrupt (WOVI) is requested. This timing is shown in figure 12.5.

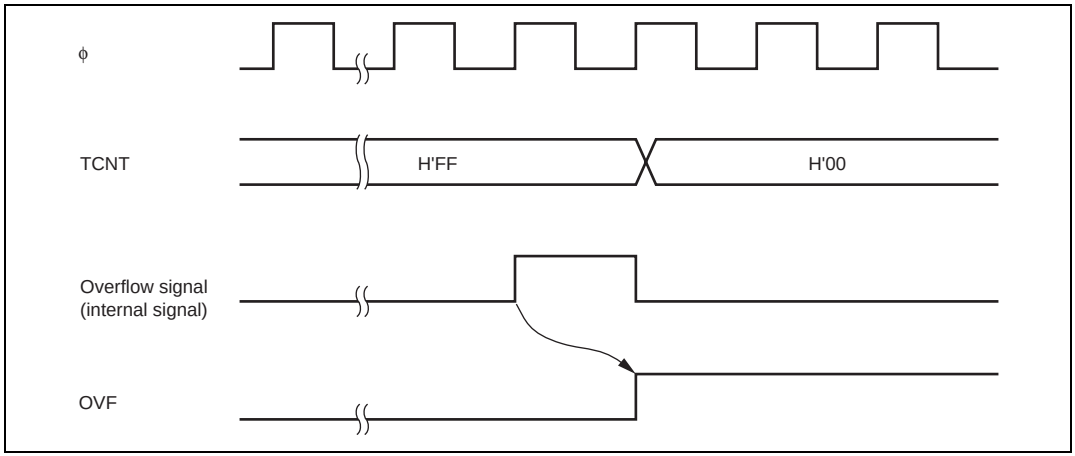


Figure 12.5 Timing of OVF Setting

12.3.4 Timing of Setting Watchdog Timer Overflow Flag (WOVF)

With WDT_0 the WOVF bit in RSTCSR is set to 1 if TCNT overflows in watchdog timer mode. If TCNT overflows while the RSTE bit in RSTCSR is set to 1, an internal is generated for the entire chip. (WOVI interrupt is not generated.) This timing is illustrated in figure 12.6.

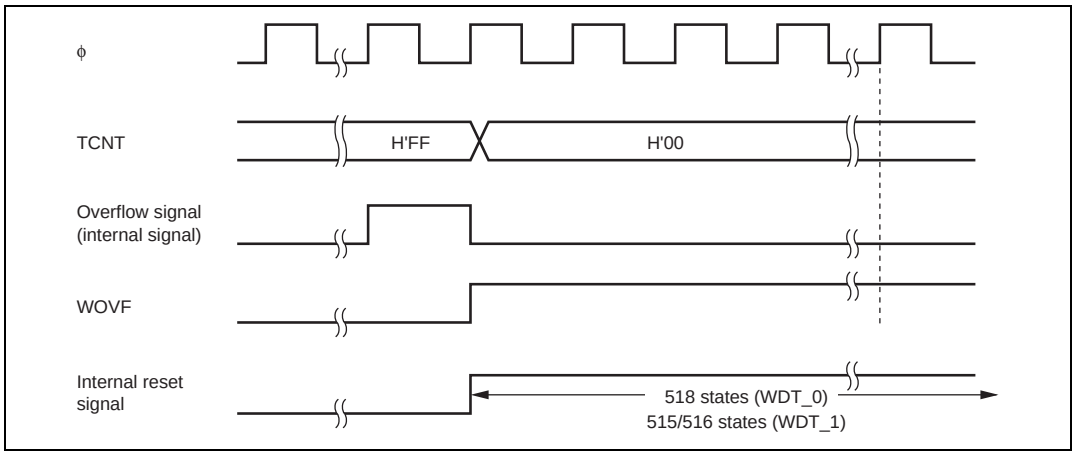


Figure 12.6 Timing of WOVF Setting

3. 8-bit data is sent from the TxD pin synchronized with the output clock when output clock mode has been specified, and synchronized with the input clock when use of an external clock has been specified.
4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated. The SCK pin is fixed high.

Figure 13.20 shows a sample flow chart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (ORER, FER, or PER) is set to 1. Make sure that the receive error flags are cleared to 0 before starting transmission. Note that clearing the RE bit to 0 does not clear the receive error flags.

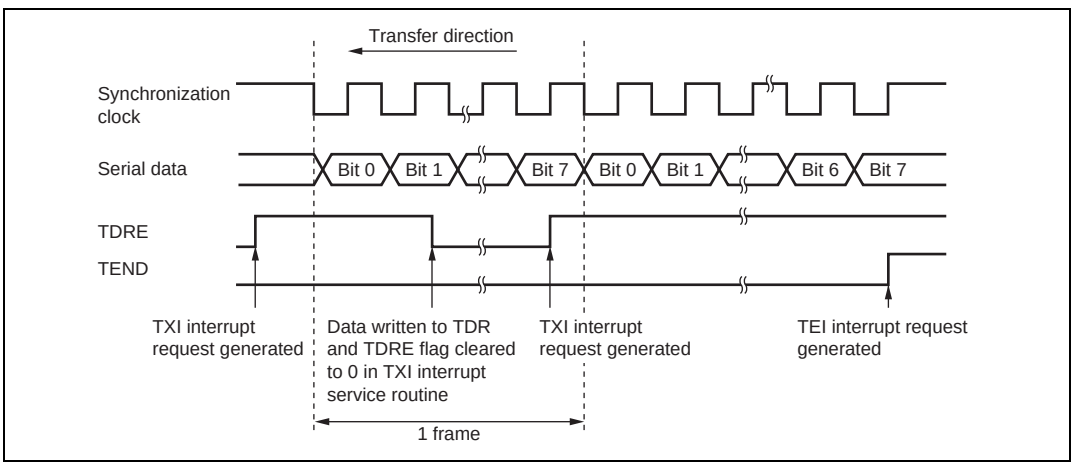
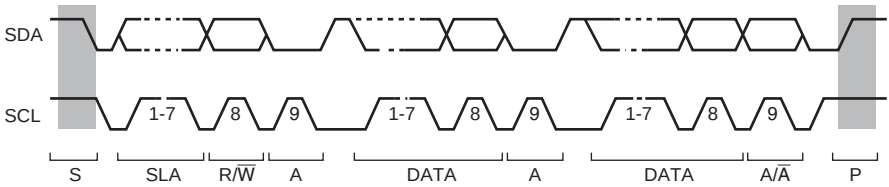


Figure 13.19 Sample SCI Transmission Operation in Clocked Synchronous Mode



Legend:
S: Start condition. The master device drives SDA from high to low while SCL is high
SLA: Slave address
R/$\overline{W}$: Indicates the direction of data transfer: from the slave device to the master device when R/$\overline{W}$ is 1, or from the master device to the slave device when R/$\overline{W}$ is 0
A: Acknowledge. The receiving device drives SDA low to acknowledge a transfer.
DATA: Transferred data
P: Stop condition. The master device drives SDA from low to high while SCL is high

Figure 14.5 I²C Bus Timing

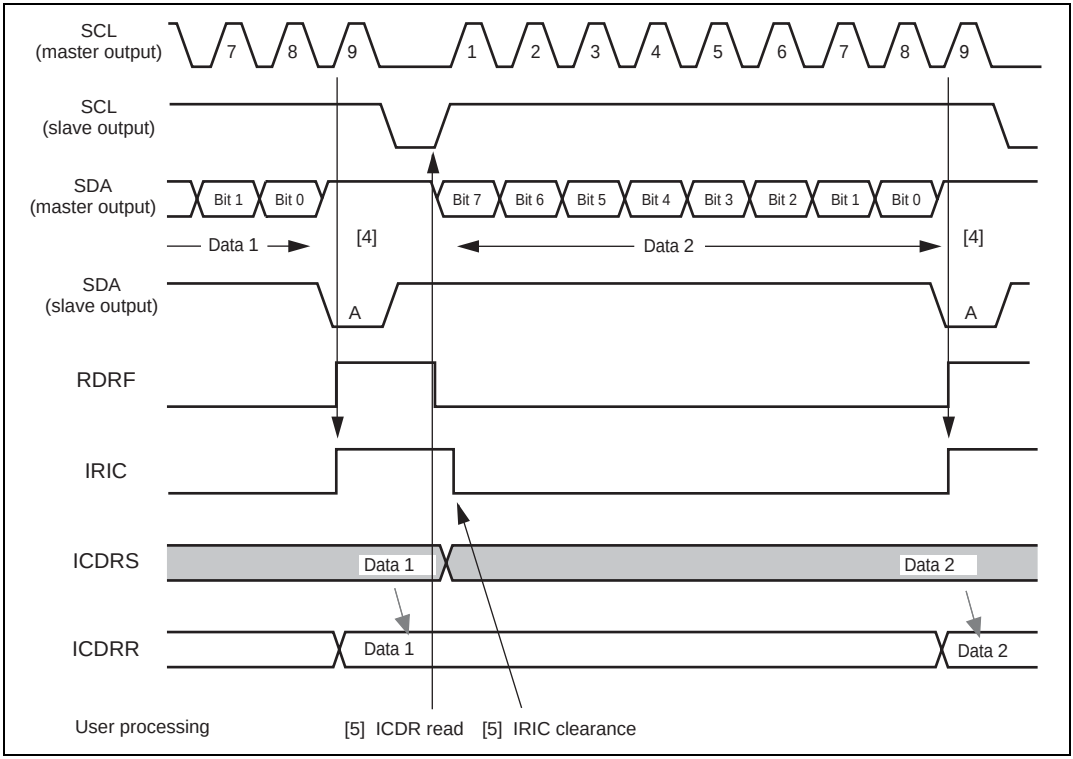


Figure 14.16 Example of Slave Receive Mode Operation Timing (2) (MLS = ACKB = 0)

Table 15.3 A/D Conversion Time (Single Mode)

		CKS1 = 0						CKS1 = 1					
		CKS0 = 0			CKS0 = 1			CKS0 = 0			CKS0 = 1		
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A/D conversion start delay	t_D	18	—	33	10	—	17	6	—	9	4	—	5
Input sampling time	t_{SPL}	—	127	—	—	63	—	—	31	—	—	15	—
A/D conversion time	t_{CONV}	515	—	530	259	—	266	131	—	134	67	—	68

Note: * All values represent the number of states.

Table 15.4 A/D Conversion Time (Scan Mode)

CKS1	CKS0	Conversion Time (State)
0	0	512 (Fixed)
	1	256 (Fixed)
1	0	128 (Fixed)
	1	64 (Fixed)

Table 16.2 D/A Conversion Control

Bit 5	Bit 7	Bit 6	
DAE	**DAOE1**	**DAOE0**	**Description**
0	0	0	Disables D/A Conversion
		1	Enables D/A Conversion for channel 0
	1	0	Enables D/A Conversion for channel 1
		1	Enables D/A Conversion for channels 0 and 1
1	0	0	Disables D/A Conversion
		1	Enables D/A Conversion for channels 0 and 1
	1	0	
		1	

16.4 Operation

Two channels of the D/A converter can perform conversion individually.

When the DAOE bit in DACR is set to 1, D/A conversion is enabled and the conversion results are output.

An example of D/A conversion of channel 0 is shown below. The operation timing is shown in figure 16.2.

1. Write conversion data to DADR0.
2. When the DAOE0 bit in DACR is set to 1, D/A conversion starts. After the interval of t_{DCONV}, the conversion results are output from the analog output pin DA0. The conversion results are output continuously until DADR0 is modified or DAOE0 bit is cleared to 0. The output value is calculated by the following formula:

   (DADR contents)/256 × Vref

3. Conversion starts immediately after DADR0 is modified. After the interval of t_{DCONV}, conversion results are output.
4. When the DAOE bit is cleared to 0, analog output is disabled.

Table 17.6 Output Levels

Data		0	0	1	1
M		**0**	**1**	**0**	**1**
Static	Common output	V1	V_{SS}	V1	V_{SS}
	Segment output	V1	V_{SS}	V_{SS}	V1
1/2 duty	Common output	V2, V3	V2, V3	V1	V_{SS}
	Segment output	V1	V_{SS}	V_{SS}	V1
1/3 duty	Common output	V3	V2	V1	V_{SS}
	Segment output	V2	V3	V_{SS}	V1
1/4 duty	Common output	V3	V2	V1	V_{SS}
	Segment output	V2	V3	V_{SS}	V1

17.4.3 Triple Step-Up Voltage Circuit (Supported Only by the H8S/2268 Group)

The H8S/2268 Group incorporates a triple step-up voltage circuit. Triple voltage of liquid crystal input reference voltage (V_{LCD3}) input from V3 pin can be used for the LCD driver.

Before enabling the step-up voltage circuit, duty cycle (1/3 duty or 1/4 duty), LCD driver or I/O pin function, and display data and frame frequency should be selected. Around 0.1-µF capacitor should be connected between C1 and C2, and voltage specified in section 25.2.6, LCD Characteristics should be applied to V3 pin.

After above settings, by selecting the step-up voltage circuit clock in LCD control register 2 (LCR2) and setting SUPS to 1, the triple step-up voltage circuit operates, voltage double of V_{LCD3} is generated for V2 pin, and voltage triple of V_{LCD3} is generated for V1pin.

Notes: 1. The triple step-up voltage circuit should only be used as LCD drive power of the H8S/2268 Group. To drive large panel, power supply capacitance may be insufficient. In this case, Vcc should be used as power supply or external power supply circuit should be used.
2. When the triple step-up voltage circuit is used, do not specify static or 1/2 duty as duty cycle.
3. Do not use capacitance with polarity such as electrolytic capacitor as capacitance to be connected between C1 and C2.

25.4 Operation Timing

Operation timings are shown below.

25.4.1 Oscillator Settling Timing

Figure 25.4 shows the oscillator settling timing.

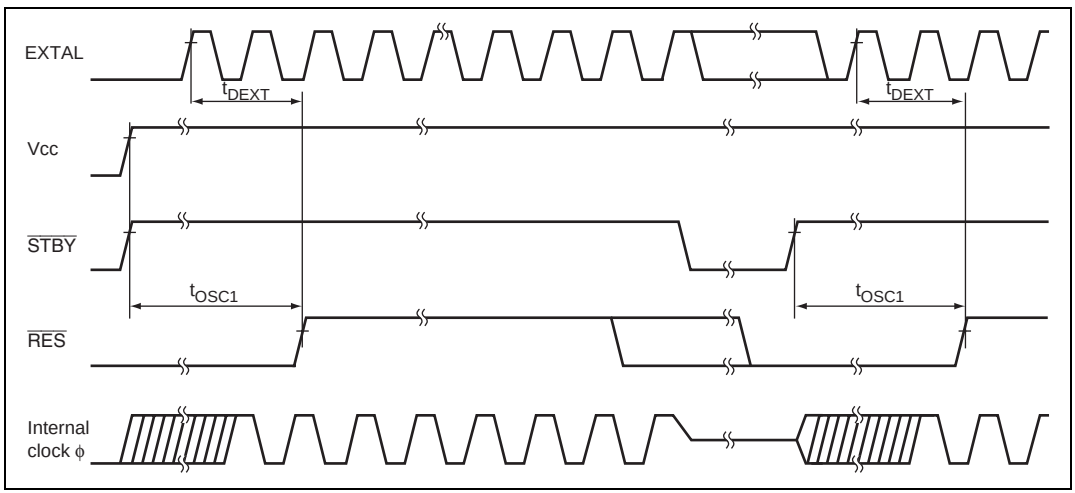


Figure 25.4 Oscillator Settling Timing

25.4.2 Control Signal Timings

Control signal timings are shown below.

- Reset Input Timing
  Figure 25.5 shows the reset input timing.
- Interrupt Input Timing
  Figure 25.6 shows the NMI, $\overline{\text{IRQ}}$ interrupt reset input timing.

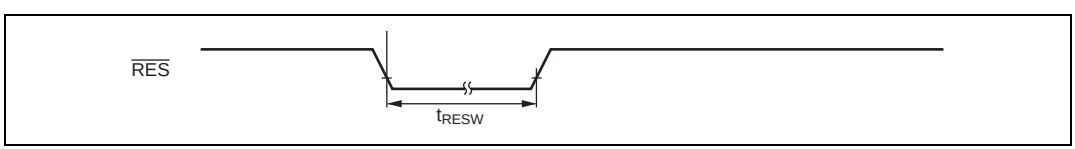


Figure 25.5 Reset Input Timing

Port Name	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Program Execution State Sleep Mode Subsleep Mode
Port M	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG32 to SEG25	SEG32 to SEG25
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
Port N	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG40 to SEG33	SEG40 to SEG33
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port

A.2 I/O Port State in Each Pin State of H8S/2264 Group

Port Name	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Program Execution State Sleep Mode Subsleep Mode
Port 1	T	T	Keep	Keep	I/O port
Port 3	T	T	Keep	Keep	I/O port
Port 4	T	T	T	T	Input port
Port 7	T	T	Keep	Keep	I/O port
Port 9	T	T	T	T	Input port
Port F	T	T	Keep	Keep	I/O port
PH7	T	T	T	T	Input port
PH3 to PH0	T	T	[Common output]	[Common output]	[Common output]
			Port	COM4 to COM1	COM4 to COM1
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
Port J	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG8 to SEG1	SEG8 to SEG1
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port