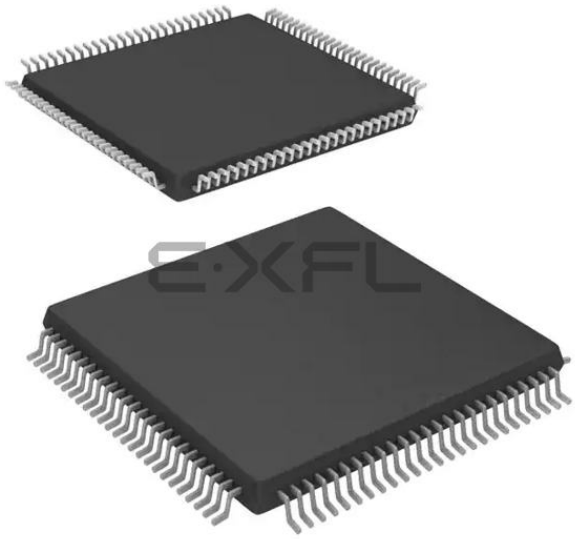

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2265te13v

Section 14 I^2C Bus Interface (IIC) (Supported as an Option by H8S/2264 Group)

1.4 Pin Functions

Table 1.1 lists the pins functions.

Table 1.1 Pin Functions

Type	Symbol	Pin NO.	I/O	Function
Power supply	Vcc	62	Input	Power supply pin. Connect this pin to the system power supply.
	CVcc	12	Input	Connect this pin to Vss via a capacitor (H8S/2268 Group: 0.1 μF/0.2 μF and H8S/2264 Group: 0.2 μF) for voltage stabilization. Note that applying a voltage exceeding 4.3 V, the absolute maximum rating, to the CVcc pin may cause fatal damages on this LSI. Do not connect the power supply to the CVcc pin. See section 23, Power Supply Circuit, for connecting examples.
	V3 V2 V1	85 86 87	Input	Power supply pins for the LCD controller/driver. With an internal power supply division resistor, these pins are normally left open. Power supply should be within the range of Vcc ≥ V1 ≥ V2 ≥ V3 ≥ Vss. When the triple step-up voltage circuit[*1] is used, the V3 pin is used for the LCD input reference power supply.
	Vss	14 64	Input	Ground pins. Connect this pin to the system power supply (0 V).
Clock	XTAL	63	Input	For connection to a crystal resonator. This pin can be also used for external clock input. For examples of crystal resonator connection and external clock input, see section 21, Clock Pulse Generator.
	EXTAL	65	Input	
	OSC1	58	Input	Connects to a 32.768 kHz crystal resonator. See section 21, Clock Pulse Generator, for typical connection diagrams for a crystal resonator.
	OSC2	57	Input	
Operating mode control	MD2, MD1	67 56	Input	Sets the operating mode. Inputs at these pins should not be changed during operation. Be sure to fix the levels of the mode pins (MD2, MD1) by pull-down or pull-up, except for mode changing.

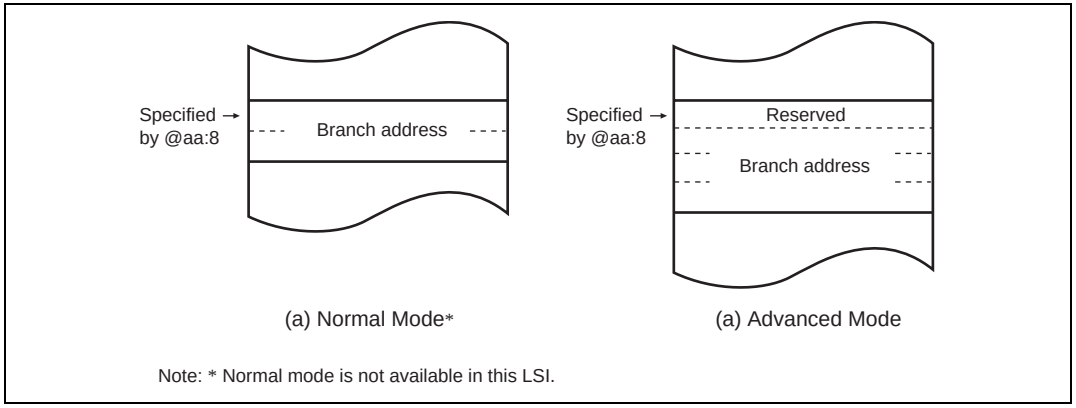


Figure 2.12 Branch Address Specification in Memory Indirect Mode

2.7.9 Effective Address Calculation

Table 2.13 indicates how effective addresses are calculated in each addressing mode. In normal mode the upper 8 bits of the effective address are ignored in order to generate a 16-bit address.

The BSET, BCLR, BNOT, BST and BIST instructions are executed as follows:

1. Data is read in bytes.
2. The operation corresponding to the instruction is applied to the specified bit of the data.
3. The byte produced by the bit-manipulation is written back.

- Consider this example, where the BCLR instruction is executed to clear only bit 4 in P1DDR of Port 1.

  P1DDR is an 8-bit register that consists of write-only bits and specifies input or output for each pin of port 1. Reading of these bits is not valid, since values read are specified as undefined.

  In the following example, the BCLR instruction specifies P14 as an input. Before the operation, P17 to P14 are set as output pins and P13 to P10 are set as input pins. The value of P1DDR is H'F0.

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Output	Input	Input	Input	Input
P1DDR	1	1	1	1	0	0	0	0

  To switch P14 from an output to an input, the value of bit 4 in P1DDR has to be changed from 1 to 0 (H'F0 to H'E0). The BCLR instruction used to clear bit 4 in P1DDR is as follows.

```
BCLR    #4, @P1DDR
```

  However, the above bit-manipulation of the write-only P1DDR register may cause the following problem.

  The data in P1DDR is read in bytes. Data read from P1DDR is undefined. Thus, regardless of whether the value in the register is 0 or 1, it is impossible to tell which value will be read. All bits in P1DDR are write-only, thus read as undefined. The actual value in P1DDR is H'F0. Let us assume that the value read is H'F8, where the value of bit 3 is read as 1 rather than its actual value of 0.

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Output	Input	Input	Input	Input
P1DDR	1	1	1	1	0	0	0	0
Read value	1	1	1	1	1	0	0	0

4.2 Exception Sources and Exception Vector Table

Different vector addresses are assigned to different exception sources. Table 4.2 lists the exception sources and their vector addresses.

Table 4.2 Exception Handling Vector Table

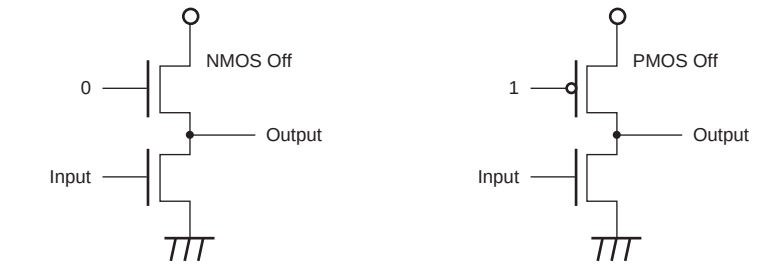
Exception Source		Vector Number	Vector Address Advanced Mode*1
Reset		0	H'0000 to H'0003
Reserved for system use		1	H'0004 to H'0007
		2	H'0008 to H'000B
		3	H'000C to H'000F
		4	H'0010 to H'0013
Trace*4		5	H'0014 to H'0017
Direct transitions*3		6	H'0018 to H'001B
External interrupt (NMI)		7	H'001C to H'001F
Trap instruction (four sources)		8	H'0020 to H'0023
		9	H'0024 to H'0027
		10	H'0028 to H'002B
		11	H'002C to H'002F
Reserved for system use		12	H'0030 to H'0033
		13	H'0034 to H'0037
		14	H'0038 to H'003B
		15	H'003C to H'003F
External interrupt	IRQ0	16	H'0040 to H'0043
	IRQ1	17	H'0044 to H'0047
Reserved for system use		18	H'0048 to H'004B
External interrupt	IRQ3	19	H'004C to H'004F
	IRQ4	20	H'0050 to H'0053
	IRQ5*4	21	H'0054 to H'0057
Reserved for system use		22	H'0058 to H'005B
		23	H'005C to H'005F

9.2.5 Pin Functions

The port 3 pins also function as SCI I/O input pins (TxD0, RxD0, SCK0, TxD1, RxD1, and SCK1), I²C bus interface I/O pins (SCL0, SDA0, SCL1*, and SDA1*), and as external interrupt input pins ($\overline{\text{IRQ4}}$ and $\overline{\text{IRQ5}}$*).

As shown in figure 9.1, when the pins P34, P35, SCK1, SCL0, or SDA0 type open drain output is used, a bus line is not affected even if the power supply for this LSI fails. Use (a) type open drain output when using a bus line having a state in which the power is not supplied to this LSI.

Note: * Supported only by the H8S/2268 Group.



(a) Open drain output type for P34, P35, SCK1, SCL0, and SDA0 pins

(b) Open drain output type for P33 to P30, SCL1*, and SDA1* pins

Note: * Supported only by the H8S/2268 Group.

Figure 9.1 Types of Open Drain Outputs

The NMOS push-pull outputs of the P34, P35, and SCK1 pins do not reach the voltage of Vcc, even when the pins are specified so that they are driven high and regardless of the load.

To output the voltage of Vcc, a pull-up resistor must be externally connected.

Notes: 1. When a pull-up resistor is externally connected, signals take longer to rise and fall. When the input signals take a long time to rise and fall, connect an input circuit that has a noise reduction function, such as a Schmitt trigger circuit.
2. For high-speed operation, use an external circuit such as a level shifter.
3. For output characteristics, see the entries for high output voltage for pins P34 and P35 in table 25.15, DC Characteristics (1). The value of the pull-up resistor should satisfy the specification in table 25.16, Permissible Output Currents.

The functions of port 3 pins are shown below.

9.10 Port L

Port L is an 8-bit I/O port and has the following registers.

- Port L data direction register (PLDDR)
- Port L data register (PLDR)
- Port L register (PORTL)

9.10.1 Port L Data Direction Register (PLDDR)

PLDDR specifies input or output of the port L pins using the individual bits. PLDDR cannot be read; if it is, an undefined value will be read.

The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Bit	Bit Name	Initial Value	R/W	Description
7	PL7DDR	0	W	When a pin is specified as a general purpose I/O port, setting this bit to 1 makes the corresponding port L pin an output port. Clearing this bit to 0 makes the pin an input port.
6	PL6DDR	0	W	
5	PL5DDR	0	W	
4	PL4DDR	0	W	
3	PL3DDR	0	W	
2	PL2DDR	0	W	
1	PL1DDR	0	W	
0	PL0DDR	0	W	

10.5 Operation

10.5.1 Basic Functions

Each channel has a TCNT and TGR register. TCNT performs up-counting, and is also capable of free-running operation, synchronous counting, and external event counting.

Each TGR can be used as an input capture register or output compare register.

Counter Operation: When one of bits CST0 to CST2 in the H8S/2268 Group or one of bits CST1 and CST2 in the H8S/2264 Group is set to 1 in TSTR, the TCNT counter for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

1. Example of count operation setting procedure
   Figure 10.7 shows an example of the count operation setting procedure.

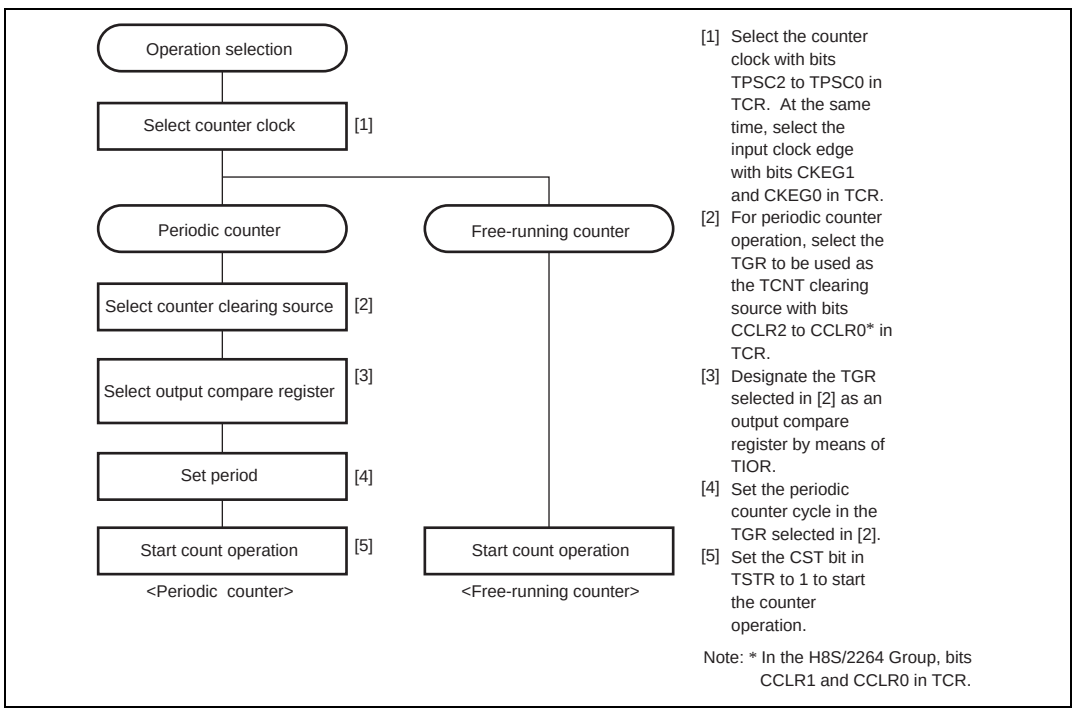


Figure 10.7 Example of Counter Operation Setting Procedure

- Smart Card Interface Mode (When SMIF in SCMR Is 1)

Bit	Bit Name	Initial Value	R/W	Description
7	TDRE	1	R/(W)*1	Transmit Data Register Empty Indicates whether TDR contains transmit data. [Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR and data can be written to TDR [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DTC*2 is activated by a TXI interrupt request and writes data to TDR (H8S/2268 Group only)
6	RDRF	0	R/(W)*1	Receive Data Register Full Indicates that the received data is stored in RDR. [Setting condition] When serial reception ends normally and receive data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RDRF = 1 • When the DTC*2 is activated by an RXI interrupt and transferred data from RDR (H8S/2268 Group only) The RDRF flag is not affected and retains their previous values when the RE bit in SCR is cleared to 0. If reception of the next data is completed while the RDRF flag is still set to 1, an overrun error will occur and the receive data will be lost.

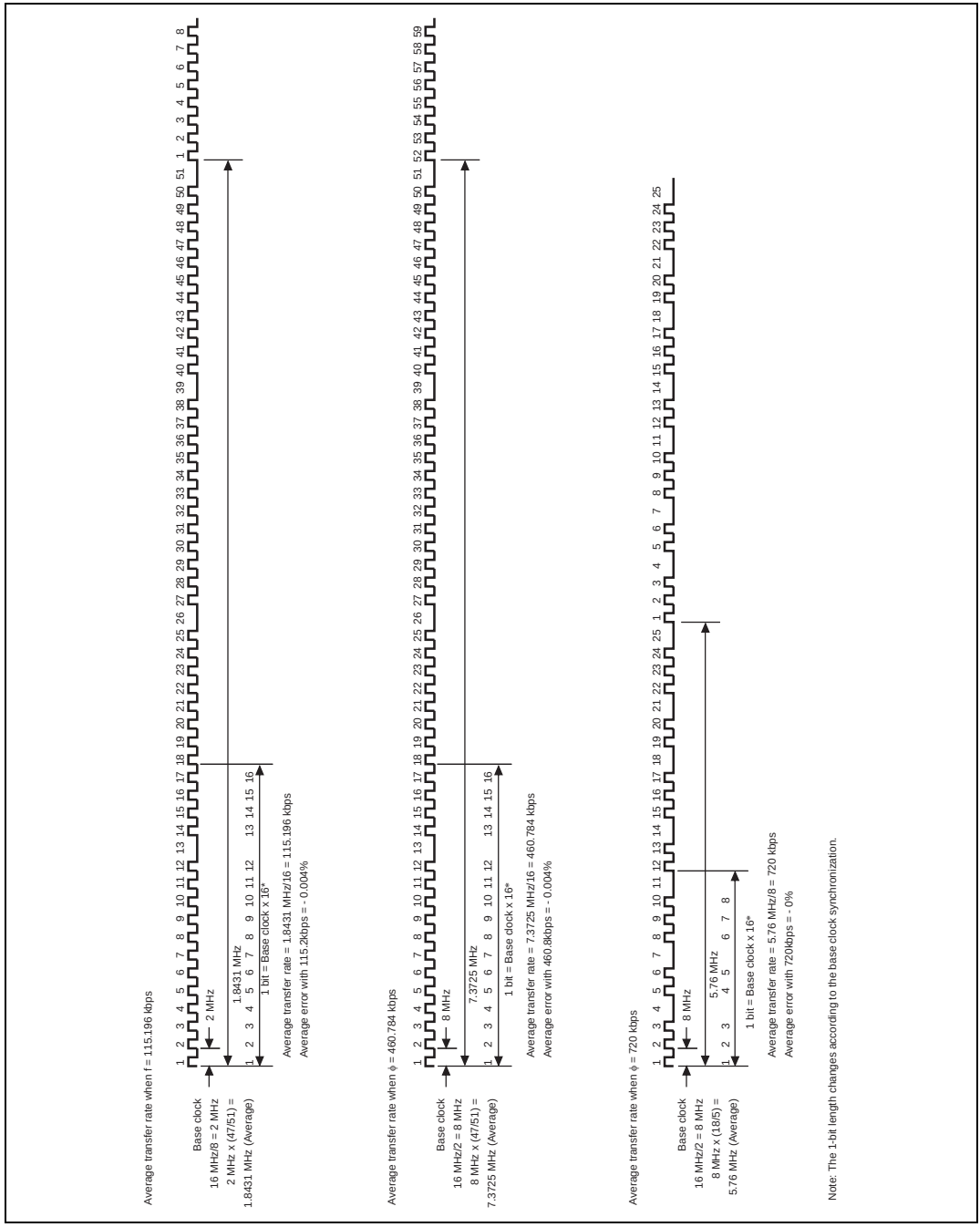


Figure 13.4 Example of Internal Base Clock when Average Transfer Rate Is Selected (2)

- Interrupt sources
  - — Data transfer end (including transmission mode transition with I²C bus format and address reception after loss of master arbitration)
  - — Address match: when any slave address matches or the general call address is received in slave receive mode
  - — Start condition detection (in master mode)
  - — Stop condition detection (in slave mode)
- Selection of 16 internal clocks (in master mode)
- Direct bus drive
  - — Two pins, P35/SCL0 and P34/SDA0, function as NMOS open-drain outputs when the bus drive function is selected.
  - — Two pins – P33/SCL1 and P32/SDA1—function as NMOS-only outputs when the bus drive function is selected. (H8S/2268 Group only)

Figure 14.1 shows a block diagram of the I²C bus interface. Figure 14.2 shows an example of I/O pin connections to external circuits. Channel I/O pins are NMOS open drains, and it is possible to apply voltages in excess of the power supply (Vcc) voltage for this LSI. Set the upper limit of voltage applied to the power supply (Vcc) power supply range +0.3 V, i.e. 5.8 V. Channel 1 (H8S/2268 Group only) I/O pins are driven solely by NMOS, so in terms of appearance they carry out the same operations as an NMOS open drain. However, the voltage which can be applied to the I/O pins depends on the voltage of the power supply (Vcc) of this LSI.

14.3.7 I²C Bus Status Register (ICSR)

ICSR consists of status flags.

Bit	Bit Name	Initial Value	R/W	Description
7	ESTP	0	R/(W)*	Error Stop Condition Detection Flag This bit is valid in I²C bus format slave mode. [Setting condition] When a stop condition is detected during frame transfer. [Clearing conditions] • When 0 is written in ESTP after reading the state of 1 • When the IRIC flag is cleared to 0
6	STOP	0	R/(W)*	Normal Stop Condition Detection Flag This bit is valid in I²C bus format slave mode. [Setting condition] When a stop condition is detected during frame transfer. [Clearing conditions] • When 0 is written in STOP after reading STOP = 1 • When the IRIC flag is cleared to 0
5	IRTR	0	R/(W)*	I²C Bus Interface Continuous Transmission/Reception Interrupt Request Flag [Setting conditions] In I²C bus interface slave mode • When the TDRE or RDRF flag is set to 1 when AASX = 1 In I²C bus interface other modes • When the TDRE or RDRF flag is set to 1 [Clearing conditions] • When 0 is written in IRTR after reading IRTR = 1 • When the IRIC flag is cleared to 0 while ICE is 1

Section 15 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter that allows up to ten analog input channels to be selected. A block diagram of the A/D converter is shown in figure 15.1.

15.1 Features

- 10-bit resolution
- Ten input channels
- Conversion time: 6.3 µs per channel (at 20.5 MHz operation)
- Two operating modes
  Single mode: Single-channel A/D conversion
  Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
  Conversion results are held in a 16-bit data register for each channel.
- Sample and hold function
- Three methods conversion start
  Software
  16-bit timer pulse unit (TPU or TMR) conversion start trigger
  External trigger signal
- Interrupt request
  An A/D conversion end interrupt request (ADI) can be generated.
- Module stop mode can be set
- Selectable range of voltages of analog inputs
  The range of voltages of analog inputs to be converted can be specified using the Vref signal as the analog reference voltage.

17.3.2 LCD Control Register (LCR)

LCR performs LCD power supply split-resistance connection control and display data control, and selects the frame frequency.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	LCD Disable Bit This bit is always read as 1. The write value should always be 0.
6	PSW	0	R/W	LCD Power Supply Split-Resistance Connection Control Bit 6 can be used to disconnect the LCD power supply split-resistance from V_{cc} when LCD display is not required in a power-down mode, or when an external power supply is used. When the ACT bit is cleared to 0, and also in standby mode, the LCD power supply split-resistance is disconnected from V_{cc} regardless of the setting of this bit. 0: LCD power supply split-resistance is disconnected from V_{cc} 1: LCD power supply split-resistance is connected to V_{cc}
5	ACT	0	R/W	Display Function Activate Bit 5 specifies whether or not the LCD controller/driver is used. Clearing this bit to 0 halts operation of the LCD controller/driver. The LCD drive power supply ladder resistance is also turned off, regardless of the setting of the PSW bit. However, register contents are retained. 0: LCD controller/driver operation halted 1: LCD controller/driver operation enabled
4	DISP	0	R/W	Display Data Control Bit 4 specifies whether the LCD RAM contents are displayed or blank data is displayed regardless of the LCD RAM contents. 0: Blank data is displayed 1: LCD RAM data is displayed

The differences between boot mode and user program mode are shown in table 20.1.

Figure 20.3 shows the operation flow for boot mode and figure 20.4 shows that for user program mode.

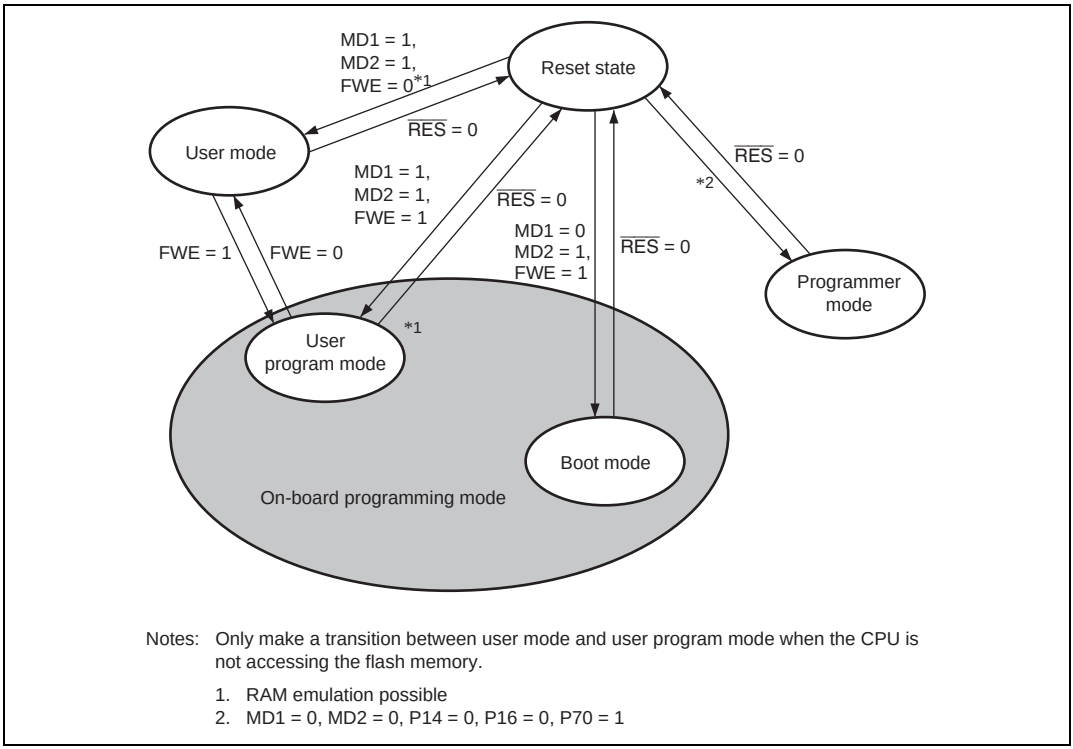


Figure 20.2 Flash Memory State Transitions

Table 20.1 Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Program/program-verify/erase/ erase-verify/emulation

Note: * To be provided by the user, in accordance with the recommended algorithm.

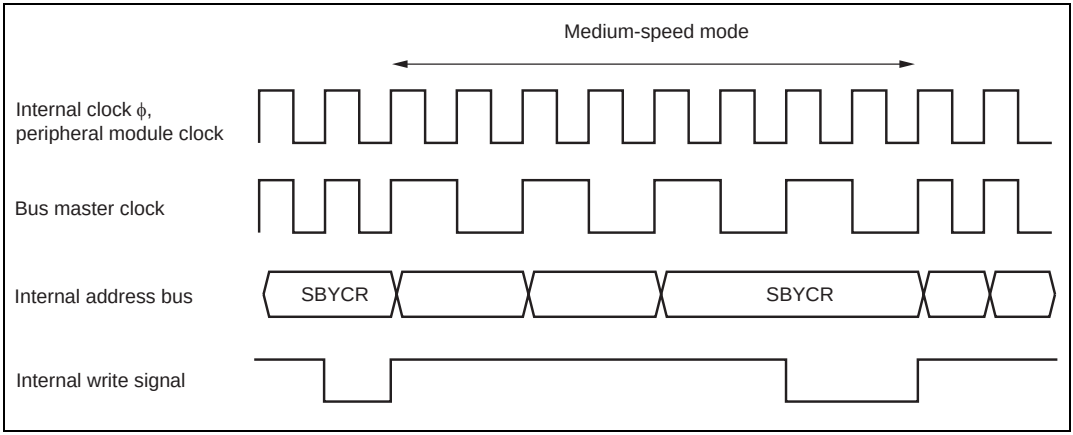


Figure 22.2 Medium-Speed Mode Transition and Clearance Timing

22.3 Sleep Mode

22.3.1 Sleep Mode

When the SLEEP instruction is executed while the SBYCR SSBY bit = 0 and the LPWRCR LSON bit = 0, the CPU enters the sleep mode. In sleep mode, CPU operation stops but the contents of the CPU's internal registers are retained. Other peripheral modules do not stop.

22.3.2 Exiting Sleep Mode

Sleep mode is exited by any interrupt, or signals at the $\overline{\text{RES}}$, or $\overline{\text{STBY}}$ pins.

- Exiting Sleep Mode by Interrupts

  When an interrupt occurs, sleep mode is exited and interrupt exception processing starts. Sleep mode is not exited if the interrupt is disabled, or interrupts other than NMI are masked by the CPU.
- Exiting Sleep Mode by $\overline{\text{RES}}$ pin

  Setting the $\overline{\text{RES}}$ pin level low selects the reset state. After the stipulated reset input duration, driving the $\overline{\text{RES}}$ pin high starts the CPU performing reset exception processing.
- Exiting Sleep Mode by $\overline{\text{STBY}}$ Pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

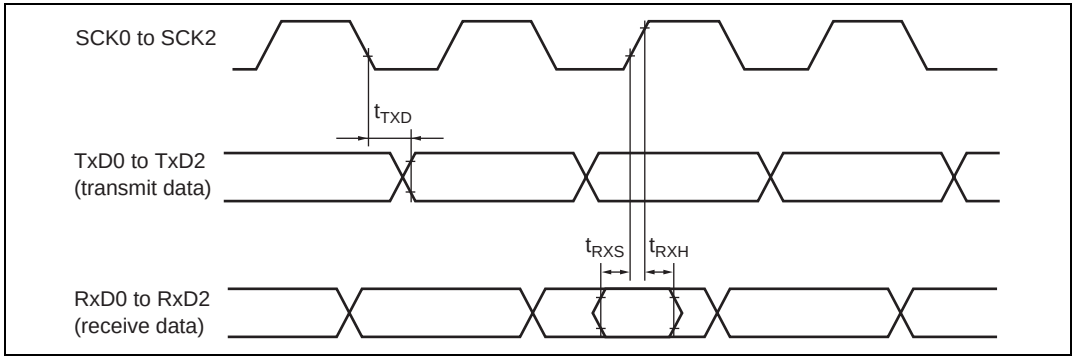
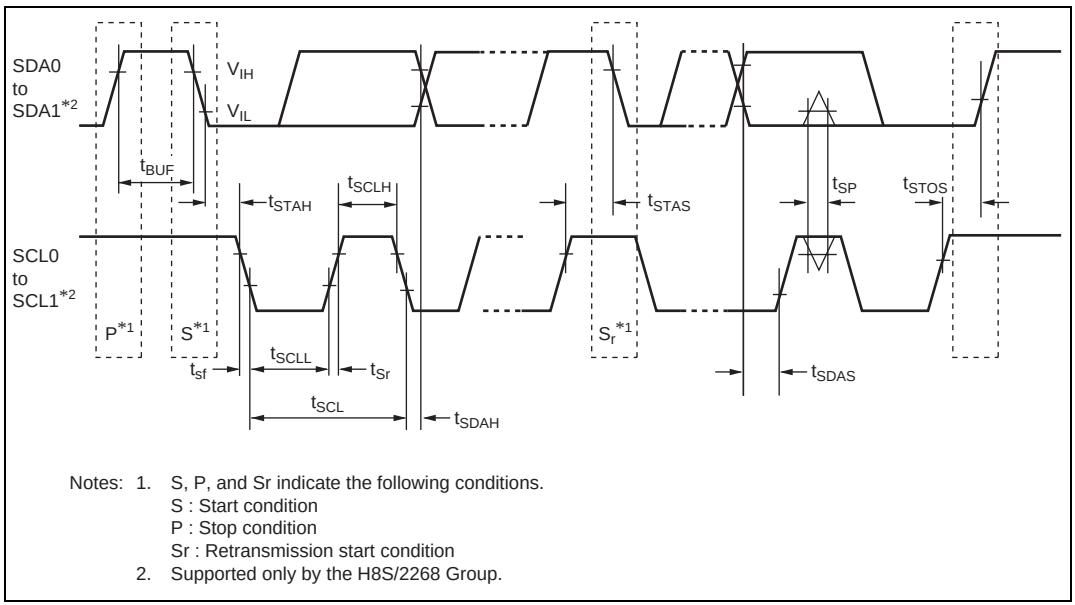


Figure 25.10 SCI Input/Output Timing (Clock Synchronous Mode)



Notes: 1. S, P, and Sr indicate the following conditions.
S : Start condition
P : Stop condition
Sr : Retransmission start condition
2. Supported only by the H8S/2268 Group.

Figure 25.11 I^2C Bus Interface Input/Output Timing (Option)

Appendix A I/O Port States in Each Pin State

A.1 I/O Port State in Each Pin State of H8S/2268 Group

Port Name	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Program Execution State Sleep Mode Subsleep Mode
Port 1	T	T	Keep	Keep	I/O port
Port 3	T	T	Keep	Keep	I/O port
Port 4	T	T	T	T	I/O port
Port 7	T	T	Keep	Keep	I/O port
P97/DA1 P96/DA0	T	T	[DAOEn = 1] Keep [DAOEn = 0] T	[DAOEn = 1] Keep [DAOEn = 0] T	Input port
Port F	T	T	Keep	Keep	I/O port
PH7	T	T	T	T	Input port
PH3 to PH0	T	T	[Common output] Port [Otherwise] Keep	[Common output] COM4 to COM1 [Otherwise] Keep	[Common output] COM4 to COM1 [Otherwise] I/O port
Port J	T	T	[Segment output] Port [Otherwise] Keep	[Segment output] SEG8 to SEG1 [Otherwise] Keep	[Segment output] SEG8 to SEG1 [Otherwise] I/O port
Port K	T	T	[Segment output] Port [Otherwise] Keep	[Segment output] SEG16 to SEG9 [Otherwise] Keep	[Segment output] SEG16 to SEG9 [Otherwise] I/O port
Port L	T	T	[Segment output] Port [Otherwise] Keep	[Segment output] SEG24 to SEG17 [Otherwise] Keep	[Segment output] SEG24 to SEG17 [Otherwise] I/O port

Port Name	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Program Execution State Sleep Mode Subsleep Mode
Port K	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG16 to SEG9	SEG16 to SEG9
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
Port L	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG24 to SEG17	SEG24 to SEG17
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
SEG40 to SEG25	T	T	T	[Segment output]	[Segment output]
				SEG40 to SEG25	SEG40 to SEG25
				[Otherwise]	[Otherwise]
				T	T

Legend:

H: High level

T: High-impedance

Keep: Input port becomes high-impedance, output port retains state

Port: Determined by port setting (input is high-impedance)

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