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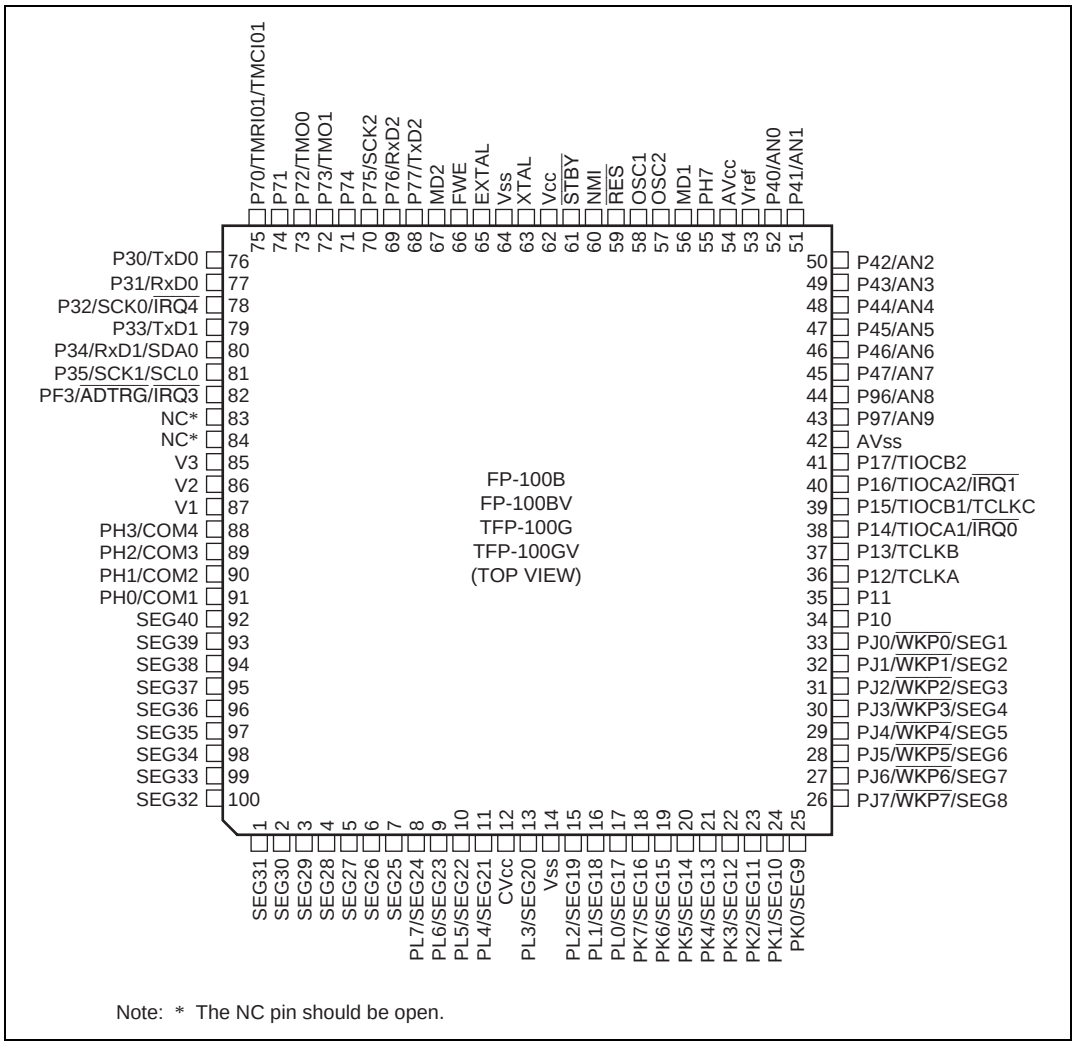
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2266fa13v



Note: * The NC pin should be open.

Figure 1.4 Pin Arrangement of H8S/2264 Group

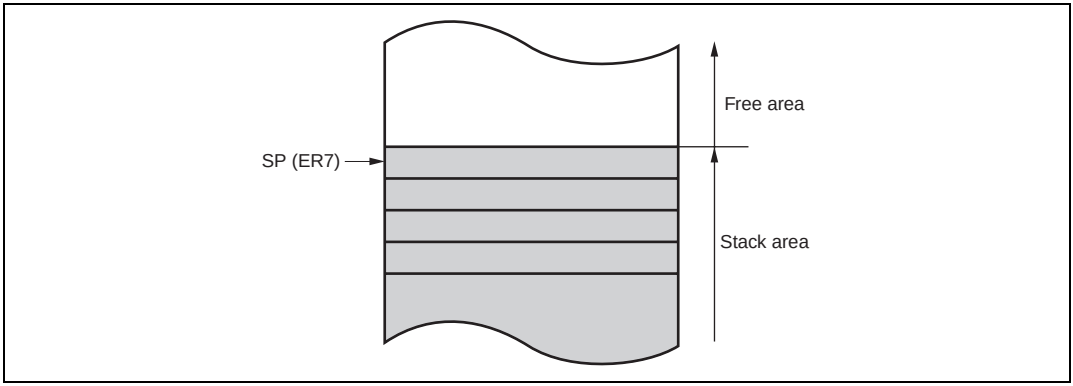


Figure 2.8 Stack Status

2.4.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0.)

2.4.3 Extended Control Register (EXR) (H8S/2268 Group Only)

EXR is an 8-bit register that manipulates the LDC, STC, ANDC, ORC, and XORC instructions. When these instructions except for the STC instruction is executed, all interrupts including NMI will be masked for three states after execution is completed.

Bit	Bit Name	Initial Value	R/W	Description
7	T	0	R/W	Trace Bit When this bit is set to 1, a trace exception is generated each time an instruction is executed. When this bit is cleared to 0, instructions are executed in sequence.
6 to 3	—	1	—	Reserved These bits are always read as 1.
2	I2	1	R/W	These bits designate the interrupt mask level (0 to 7). For details, refer to section 5, Interrupt Controller.
1	I1	1	R/W	
0	I0	1	R/W	

2.8 Processing States

The H8S/2000 CPU has five main processing states: the reset state, exception handling state, program execution state, bus-released state, and power-down state. Figure 2.13 indicates the state transitions.

- Reset State

  In this state, the CPU and all on-chip peripheral modules are initialized and not operating. When the $\overline{\text{RES}}$ input goes low, all current processing stops and the CPU enters the reset state. All interrupts are masked in the reset state. Reset exception handling starts when the $\overline{\text{RES}}$ signal changes from low to high. For details, refer to section 4, Exception Handling.

  The reset state can also be entered by a watchdog timer overflow.

- Exception-Handling State

  The exception-handling state is a transient state that occurs when the CPU alters the normal processing flow due to an exception source, such as a reset, trace, interrupt, or trap instruction. The CPU fetches a start address (vector) from the exception vector table and branches to that address. For further details, refer to section 4, Exception Handling.

- Program Execution State

  In this state, the CPU executes program instructions in sequence.

- Bus-Released State (H8S/2268 Group only)

  In a product which has a bus master other than the CPU, such as a data transfer controller (DTC), the bus-released state occurs when the bus has been released in response to a bus request from a bus master other than the CPU.

  While the bus is released, the CPU halts operations.

- Power-down State

  This is a power-down state in which the CPU stops operating. The program stop state occurs when a SLEEP instruction is executed or the CPU enters hardware standby mode. For further details, refer to section 22, Power-Down Modes.

6.2.2 Break Address Register B (BARB)

BARB is the channel B break address register. The bit configuration is the same as for BARA.

6.2.3 Break Control Register A (BCRA)

BCRA controls channel A PC breaks.

Bit	Bit Name	Initial Value	R/W	Description
7	CMFA	0	R/(W)*1	Condition Match Flag A [Setting condition] When a condition set for channel A is satisfied [Clearing condition] When 0 is written to CMFA after reading*2 CMFA = 1
6	CDA	0	R/W	CPU Cycle/DTC Cycle Select A Selects the channel A break condition bus master. 0: CPU 1: CPU or DTC
5	BAMRA2	0	R/W	Break Address Mask Register A2 to A0
4	BAMRA1	0	R/W	These bits specify which bits of the break address set in BARA are to be masked.
3	BAMRA0	0	R/W	000: BAA23 – 0 (All bits are unmasked) 001: BAA23 – 1 (Lowest bit is masked) 010: BAA23 – 2 (Lower 2 bits are masked) 011: BAA23 – 3 (Lower 3 bits are masked) 100: BAA23 – 4 (Lower 4 bits are masked) 101: BAA23 – 8 (Lower 8 bits are masked) 110: BAA23 – 12 (Lower 12 bits are masked) 111: BAA23 – 16 (Lower 16 bits are masked)
2	CSELA1	0	R/W	Break Condition Select
1	CSELA0	0	R/W	Selects break condition of channel A. 00: Instruction fetch is used as break condition 01: Data read cycle is used as break condition 10: Data write cycle is used as break condition 11: Data read/write cycle is used as break condition

Port	Description	Port and Other Functions Name	Input/Output and Output Type
Port L	General I/O port also functioning as LCD segment output pins	PL7/SEG24	
		PL6/SEG23	
		PL5/SEG22	
		PL4/SEG21	
		PL3/SEG20	
		PL2/SEG19	
		PL1/SEG18	
		PL0/SEG17	
Port M	General I/O port also functioning as LCD segment output pins	PM7/SEG32	
		PM6/SEG31	
		PM5/SEG30	
		PM4/SEG29	
		PM3/SEG28	
		PM2/SEG27	
		PM1/SEG26	
		PM0/SEG25	
Port N	General I/O port also functioning as LCD segment output pins	PN7/SEG40	
		PN6/SEG39	
		PN5/SEG38	
		PN4/SEG37	
		PN3/SEG36	
		PN2/SEG35	
		PN1/SEG34	
		PN0/SEG33	

Common Registers

- Timer start register (TSTR)
- Timer synchro register (TSYR)

Note: * Supported only by the H8S/2268 Group.

10.3.1 Timer Control Register (TCR)

The TCR registers control the TCNT operation for each channel. The H8S/2268 Group TPU has a total of three TCR registers and the H8S/2264 Group TPU has a total of two TCR registers, one for each channel (channels 0 to 2, or 1 and 2). TCR register settings should be conducted only when TCNT operation is stopped.

Bit	Bit Name	Initial value	R/W	Description
7	CCLR2	0	R/W	Counter Clear 0 to 2
6	CCLR1	0	R/W	These bits select the TCNT counter clearing source. See tables 10.3 and 10.4 for details.
5	CCLR0	0	R/W	
4	CKEG1	0	R/W	Clock Edge 0 and 1
3	CKEG0	0	R/W	These bits select the input clock edge. When the input clock is counted using both edges, the input clock period is halved (e.g. ϕ/4 both edges = ϕ/2 rising edge). Internal clock edge selection is valid when the input clock is ϕ/4 or slower. If the input clock is ϕ/1, this setting is ignored and count at falling edge of ϕ is selected. In the H8S/2268 Group, if phase counting mode is used on channels 1 and 2, this setting is ignored and the phase counting mode setting has priority. 00: Count at rising edge 01: Count at falling edge 1X: Count at both edges Legend: X: Don't care
2	TPSC2	0	R/W	Time Prescaler 0 to 2
1	TPSC1	0	R/W	These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See tables10.5 to10.7 for details.
0	TPSC0	0	R/W	

10.3.4 Timer Interrupt Enable Register (TIER)

The TIER registers control enabling or disabling of interrupt requests for each channel. The H8S/2268 Group TPU has three TIER registers and the H8S/2264 Group TPU has two TIER registers, one for each channel (channels 0 to 2, or 1 and 2).

Bit	Bit Name	Initial value	R/W	Description
7	TTGE	0	R/W	A/D Conversion Start Request Enable Enables or disables generation of A/D conversion start requests by TGRA input capture/compare match. 0: A/D conversion start request generation disabled 1: A/D conversion start request generation enabled
6	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
5	TCIEU	0	R/W	H8S/2268 Group: Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1 and 2. In channel 0, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled H8S/2264 Group: The write value should always be 0.
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled

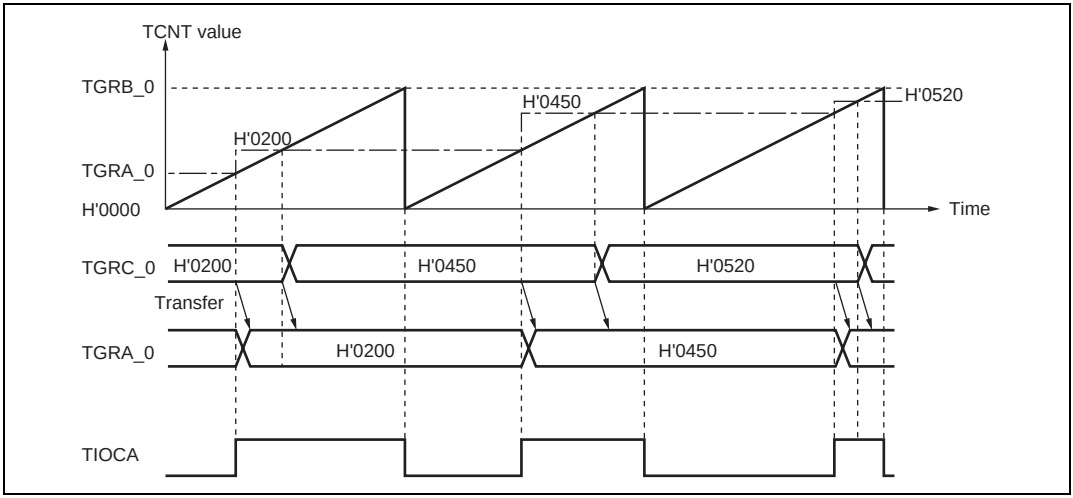


Figure 10.20 Example of Buffer Operation (1)

2. When TGR is an input capture register

   Figure 10.21 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

   Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge.

   As buffer operation has been set, when the TCNT value is stored in TGRA upon the occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

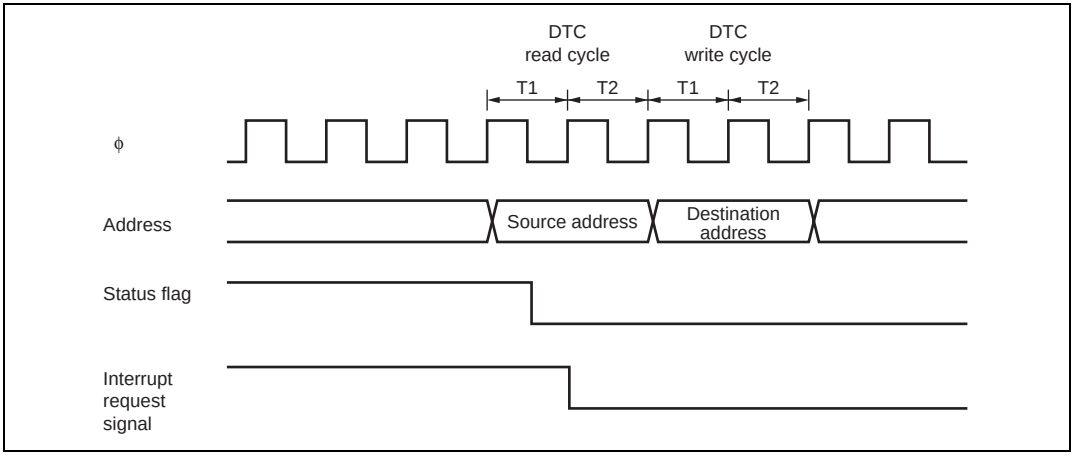


Figure 10.44 Timing for Status Flag Clearing by DTC Activation (H8S/2268 Group Only)

10.10 Usage Notes

10.10.1 Module Stop Mode Setting

TPU operation can be disabled or enabled using the module stop control register. The initial setting is for TPU operation to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 22, Power-Down Modes.

10.10.2 Input Clock Restrictions

The input clock pulse width must be at least 1.5 states in the case of single-edge detection, and at least 2.5 states in the case of both-edge detection. The TPU will not operate properly at narrower pulse widths.

In the H8S/2268 Group phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 states, and the pulse width must be at least 2.5 states. Figure 10.45 shows the input clock conditions in phase counting mode.

10.10.9 Contention between TGR Write and Input Capture

If an input capture signal is generated in the T2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed.

Figure 10.51 shows the timing in this case.

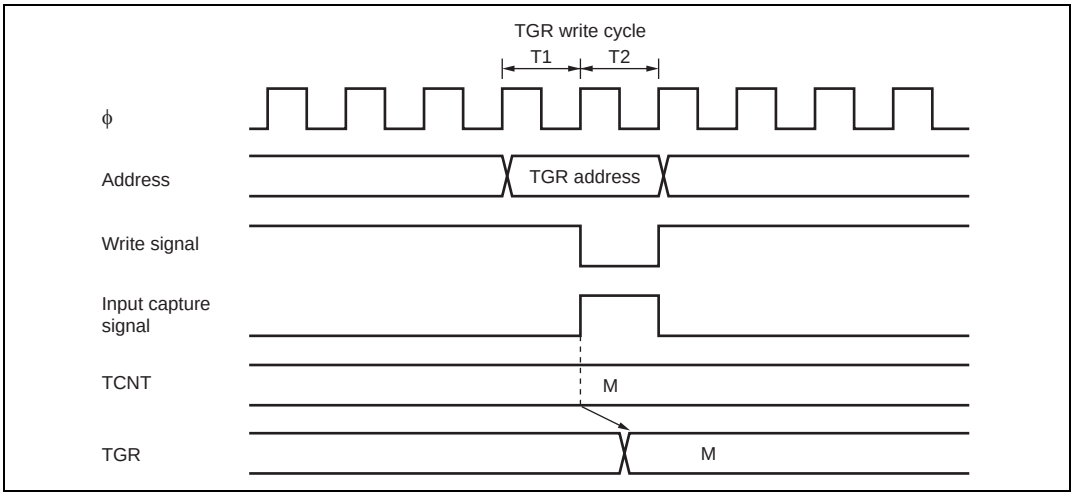


Figure 10.51 Contention between TGR Write and Input Capture

14.4 Operation

The I²C bus interface has clocked synchronous serial and I²C bus formats.

14.4.1 I²C Bus Data Format

The I²C bus formats are addressing formats and an acknowledge bit is inserted. The first frame following a start condition always consists of 8 bits. The I²C bus format is shown in figure 14.3. The clocked synchronous serial format is a non-addressing format with no acknowledge bit. This is shown in figure 14.4. Figure 14.5 shows the I²C bus timing.

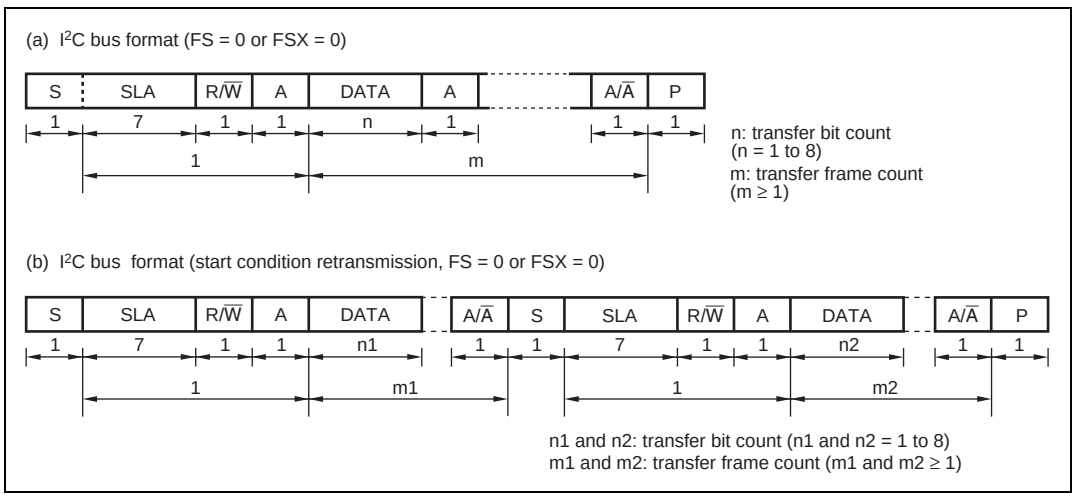


Figure 14.3 I²C Bus Data Formats (I²C Bus Formats)

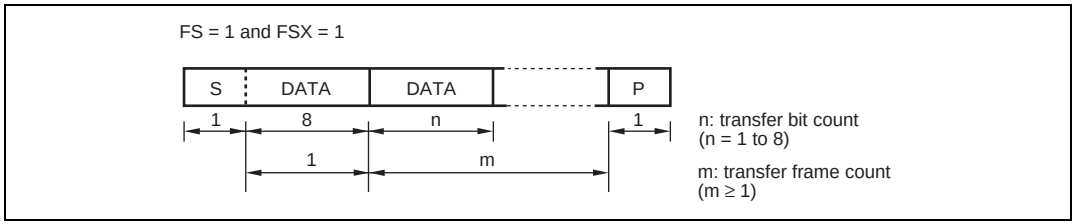


Figure 14.4 I²C Bus Data Format (Clocked Synchronous Serial Format)

14.4.7 IRIC Setting Timing and SCL Control

The interrupt request flag (IRIC) is set at different times depending on the WAIT bit in ICMR, the FS bit in SAR, and the FSX bit in SARX. If the TDRE or RDRF internal flag is set to 1, SCL is automatically held low after one frame has been transferred; this timing is synchronized with the internal clock. Figure 14.19 shows the IRIC set timing and SCL control.

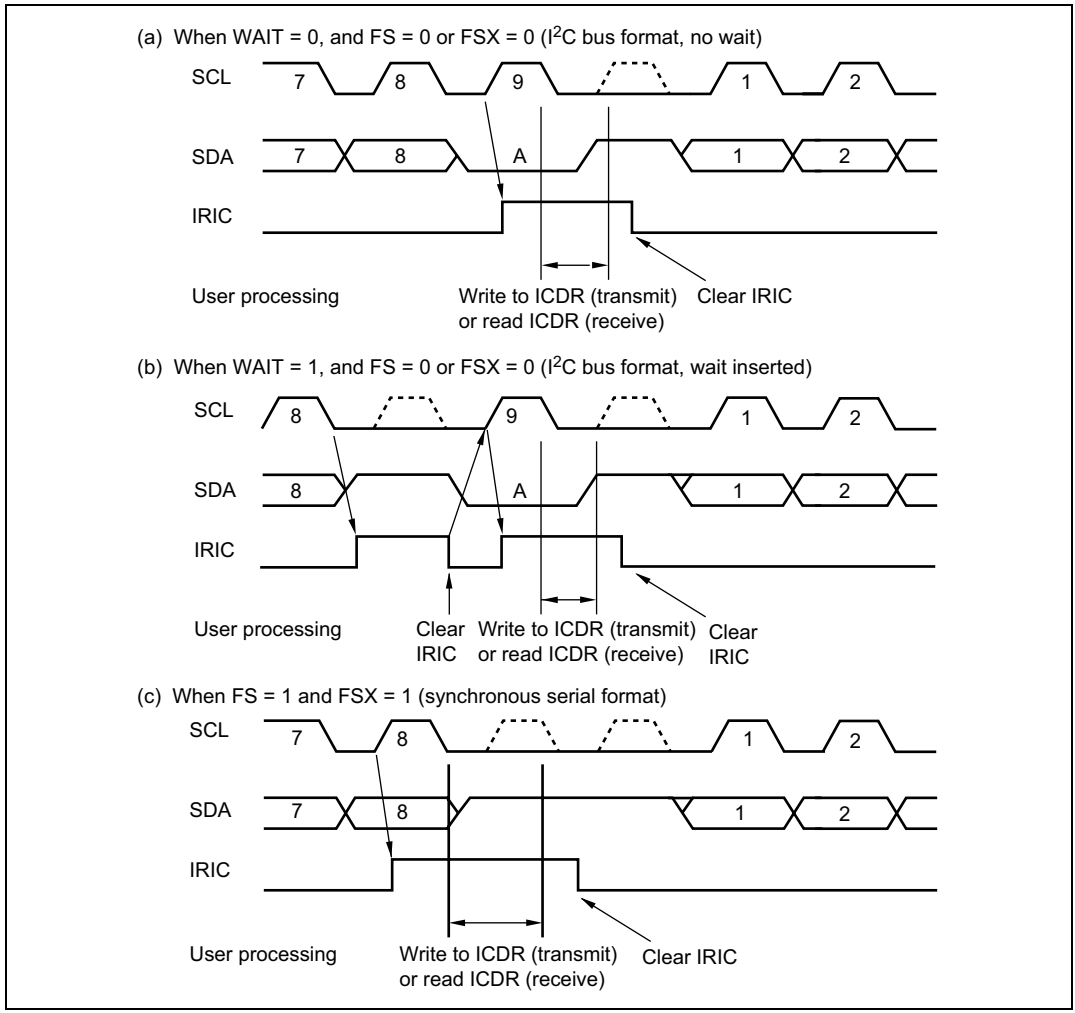


Figure 14.19 IRIC Setting Timing and SCL Control

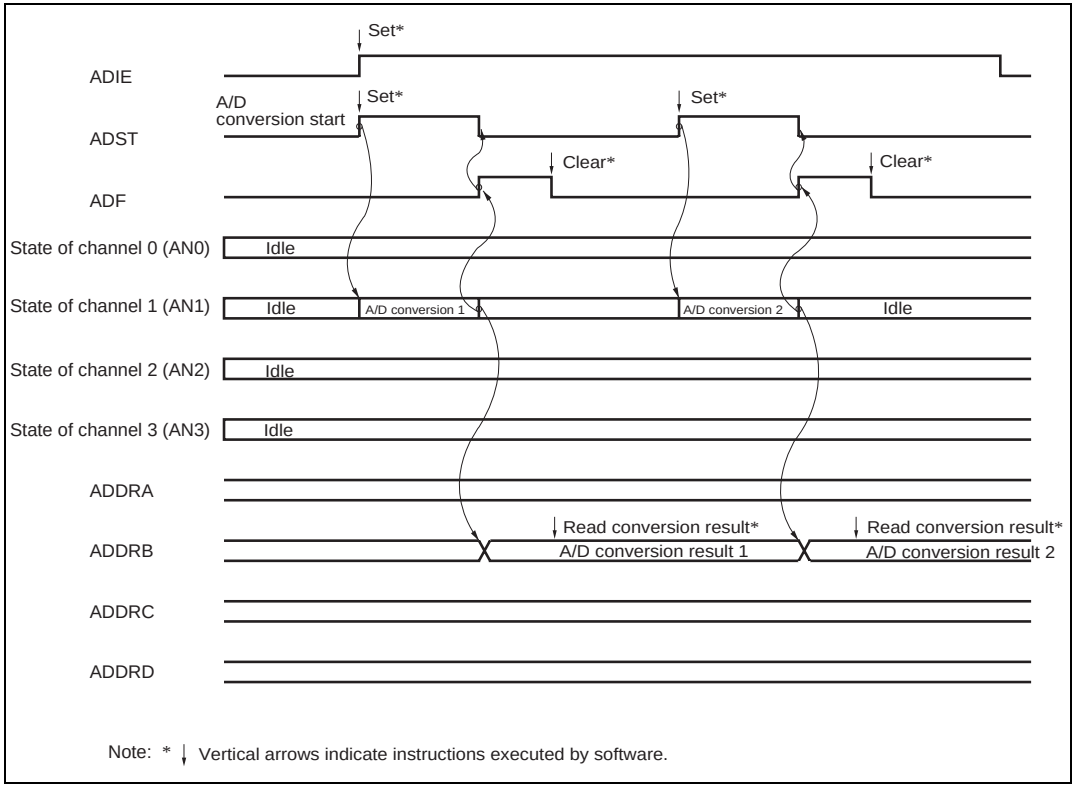


Figure 15.3 Example of A/D Converter Operation (Single Mode, Channel 1 Selected)

Bit	Bit Name	Initial Value	R/W	Description
3	CKS3	0	R/W	Frame Frequency Select 3 to 0
2	CKS2	0	R/W	Bits 3 to 0 select the operating clock and the frame frequency. In subactive mode, watch mode, and subsleep mode, the system clock (ϕ) is halted, and therefore display operations are not performed if one of the clocks from ϕ/16 to ϕ/2048 is selected. If LCD display is required in these modes, ϕ_{SUB}, ϕ_{SUB}/2, or ϕ_{SUB}/4 must be selected as the operating clock. For details, see table 17.5.
1	CKS1	0	R/W	
0	CKS0	0	R/W	

Note: 0 should be written to bit 7 after the other bits have been set.

Table 17.5 Frame Frequency Selection

Bit 3: CKS3	Bit 2: CKS2	Bit 1: CKS1	Bit 0: CKS0	Operating Clock	Frame Frequency*1	
					ϕ = 20 MHz	ϕ = 2 MHz
0	X	0	0	ϕ_{SUB}	128 Hz*2	128 Hz*2
			1	ϕ_{SUB}/2	64 Hz*2	64 Hz*2
		1	X	ϕ_{SUB}/4	32 Hz*2	32 Hz*2
1	0	0	0	ϕ/16	—	488 Hz
			1	ϕ/32	—	244 Hz
		1	0	ϕ/64	—	122 Hz
			1	ϕ/128	610 Hz	61 Hz
	1	0	0	ϕ/256	305 Hz	30.5 Hz
			1	ϕ/512	152.6 Hz	—
		1	0	ϕ/1024	76.3 Hz	—
			1	ϕ/2048	38.1 Hz	—

Legend:

X: Don't care

Notes: 1. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.

2. This is the frame frequency when ϕ_{SUB} = 32.768 kHz.

Section 21 Clock Pulse Generator

This LSI has an on-chip clock pulse generator that generates the system clock (ϕ), the bus master clock, and internal clocks. The clock pulse generator consists of an oscillator, duty adjustment circuit, clock selection circuit, medium-speed clock divider, bus master clock selection circuit, subclock oscillator, and wave formation circuit. A block diagram of the clock pulse generator is shown in figure 21.1.

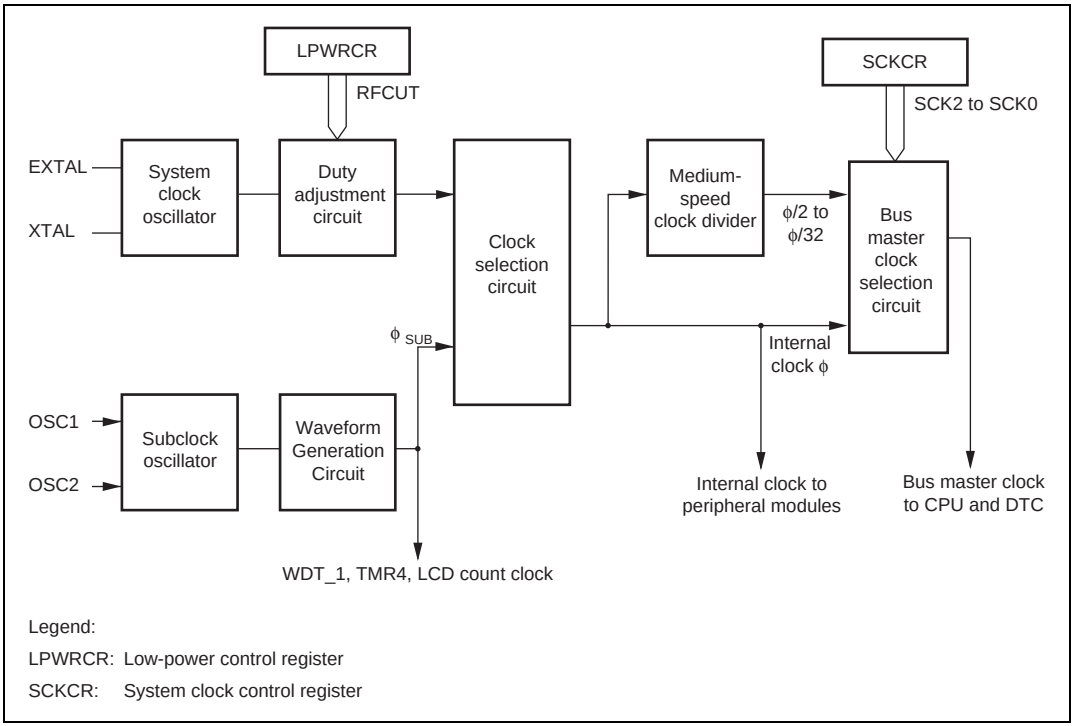


Figure 21.1 Block Diagram of Clock Pulse Generator

Frequency changes are performed by software by settings in the low-power control register (LPWRCR) and system clock control register (SCKCR).

22.7 Watch Mode

22.7.1 Transition to Watch Mode

CPU operation makes a transition to watch mode when the SLEEP instruction is executed in high-speed mode or sub-active mode with SBYCR SSBY=1, LPWRCR DTON = 0, and TCSR_1 (WDT_1) PSS = 1.

In watch mode, the CPU is stopped and peripheral modules other than WDT_1, TMR_4*, and LCD are also stopped. The contents of the CPU's internal registers, the data in internal RAM, and the statuses of the internal peripheral modules (excluding the A/D converter) and I/O ports are retained. To make a transition to watch mode, bits SCK2 to SCK0 in SCKCR must be set to 0.

Note: * Supported only by the H8S/2268 Group.

22.7.2 Exiting Watch Mode

Watch mode is exited by any interrupt (WOVI1 interrupt, OVI4 to OVI7 interrupts*, NMI pin, or $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ4}}$, $\overline{\text{IRQ5}}$*, or $\overline{\text{WKP0}}$ to $\overline{\text{WKP7}}$), or signals at the $\overline{\text{RES}}$, or $\overline{\text{STBY}}$ pins.

- Exiting Watch Mode by Interrupts

  When an interrupt occurs, watch mode is exited and a transition is made to high-speed mode or medium-speed mode when the LPWRCR LSON bit = 0 or to sub-active mode when the LSON bit = 1. When a transition is made to high-speed mode, a stable clock is supplied to all LSI circuits and interrupt exception processing starts after the time set in SBYCR STS2 to STS0 has elapsed. In the case of IRQ0, IRQ1, IRQ3, IRQ4, IRQ5*, and WKP0 to WKP7 interrupts, no transition is made from watch mode if the corresponding enable bit/pin function switching bit has been cleared to 0, and, in the case of interrupts from the internal peripheral modules, the interrupt enable register has been set to disable the reception of that interrupt, or is masked by the CPU.

  See section 22.4.3, Oscillation Settling Time after Clearing Software Standby Mode, for how to set the oscillation settling time when making a transition from watch mode to high-speed mode.
- Exiting Watch Mode by $\overline{\text{RES}}$ pins

  For exiting watch mode by the $\overline{\text{RES}}$ pins, see section 22.4.2, Clearing Software Standby Mode.
- Exiting Watch Mode by $\overline{\text{STBY}}$ pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

Note: * Supported only by the H8S/2268 Group.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ICCR_0	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_0
BRR_0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SCI_0
ICSR_0	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	IIC_0
SCR_0	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI_0
TDR_0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SSR_0	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SSR_0	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT	
RDR_0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SCMR_0	—	—	—	—	SDIR	SINV	—	SMIF	
ICDR_0/ SARX_0	ICDR7/ SVAX6	ICDR6/ SVAX5	ICDR5/ SVAX4	ICDR4/ SVAX3	ICDR3/ SVAX2	ICDR2/ SVAX1	ICDR1/ SVAX0	ICDR0/ FSX	IIC_0
ICMR_0/ SAR_0	MLS/ SVA6	WAIT/ SVA5	CKS2/ SVA4	CKS1/ SVA3	CKS0/ SVA2	BC2/ SVA1	BC1/ SVA0	BC0/ FS	
SMR_1	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_1
SMR_1	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0	
ICCR_1[*1]	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_1
BRR_1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SCI_1
ICSR_1[*1]	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	IIC_1
SCR_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI_1
TDR_1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SSR_1	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SSR_1	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT	
RDR_1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SCMR_1	—	—	—	—	SDIR	SINV	—	SMIF	
ICDR_1/ SARX_1[*1]	ICDR7/ SVAX6	ICDR6/ SVAX5	ICDR5/ SVAX4	ICDR4/ SVAX3	ICDR3/ SVAX2	ICDR2/ SVAX1	ICDR1/ SVAX0	ICDR0/FSX	IIC_1
ICMR_1/ SAR_1[*1]	MLS/ SVA6	WAIT/ SVA5	CKS2/ SVA4	CKS1/ SVA3	CKS0/ SVA2	BC2/ SVA1	BC1/ SVA0	BC0/FS	
ADDRAH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D
ADDRAL	AD1	AD0	—	—	—	—	—	—	
ADDRBH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
ADDRBL	AD1	AD0	—	—	—	—	—	—	