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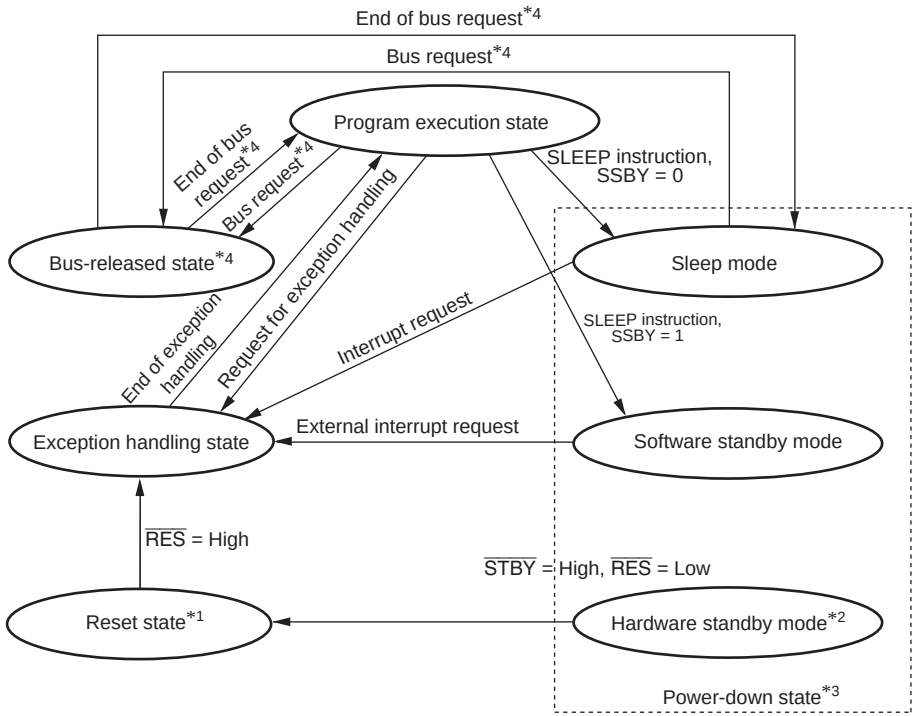
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	13MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2268fa13v

Item	Page	Revision (See Manual for Details)
9.7.1 Port H Data Direction Register (PHDDR)	165	Description added PHDDR specifies input or output the port H pins using the individual bits. PHDDR cannot be read; if it is, an undefined value will be read. The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.
9.8.1 Port J Data Direction Register (PJDDR)	170	Description added PJDDR specifies input or output the port J pins using the individual bits. PJDDR cannot be read; if it is, an undefined value will be read. The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.
9.9.1 Port K Data Direction Register (PKDDR)	174	Description added PKDDR specifies input or output the port K pins using the individual bits. PKDDR cannot be read; if it is, an undefined value will be read. The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.
9.10.1 Port L Data Direction Register (PLDDR)	176	Description added PLDDR specifies input or output of the port L pins using the individual bits. PLDDR cannot be read; if it is, an undefined value will be read. The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low. A transition can also be made to the reset state when the watchdog timer overflows.
2. From any state, a transition to hardware standby mode occurs when $\overline{STBY}$ goes low.
3. Apart from these states, there are also the watch mode, subactive mode, and the subsleep mode. See section 22, Power-Down Modes.
4. Supported only by the H8S/2268 Group.

Figure 2.13 State Transitions

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Output	Input	Input	Input	Input
P1DDR	1	1	1	1	0	0	0	0

RAM0	1	1	1	0	0	0	0	0

RAM locations are readable and writable, so there is no possibility of a problem if a bit-manipulation instruction is used to clear only bit 4 of RAM0. Read the value from RAM0 and then write it back to P1DDR.

```
MOV.B    @RAM0,     R0L
MOV.B    R0L,       @P1DDR
```

	P17	P16	P15	P14	P13	P12	P11	P10
I/O	Output	Output	Output	Input	Input	Input	Input	Input
P1DDR	1	1	1	0	0	0	0	0

RAM0	1	1	1	0	0	0	0	0

Following this procedure in access to registers that include write-only bits makes the behavior of the program independent of the type of instruction.

Table 10.14 TIORL_0 (Channel 0) (H8S/2268 Group Only)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_0 Function**	**TIOCC0 Pin Function**
0	0	0	0	Output compare register*	Output disabled
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*	Capture input source is TIOCC0 pin Input capture at rising edge
			1		Capture input source is TIOCC0 pin Input capture at falling edge
		1	X		Capture input source is TIOCC0 pin Input capture at both edges
	1	X	X		Setting disabled

Legend:

X: Don't care

Note: * When the BFA bit in TMDR_0 is set to 1 and TGRC_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Figure 10.25 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

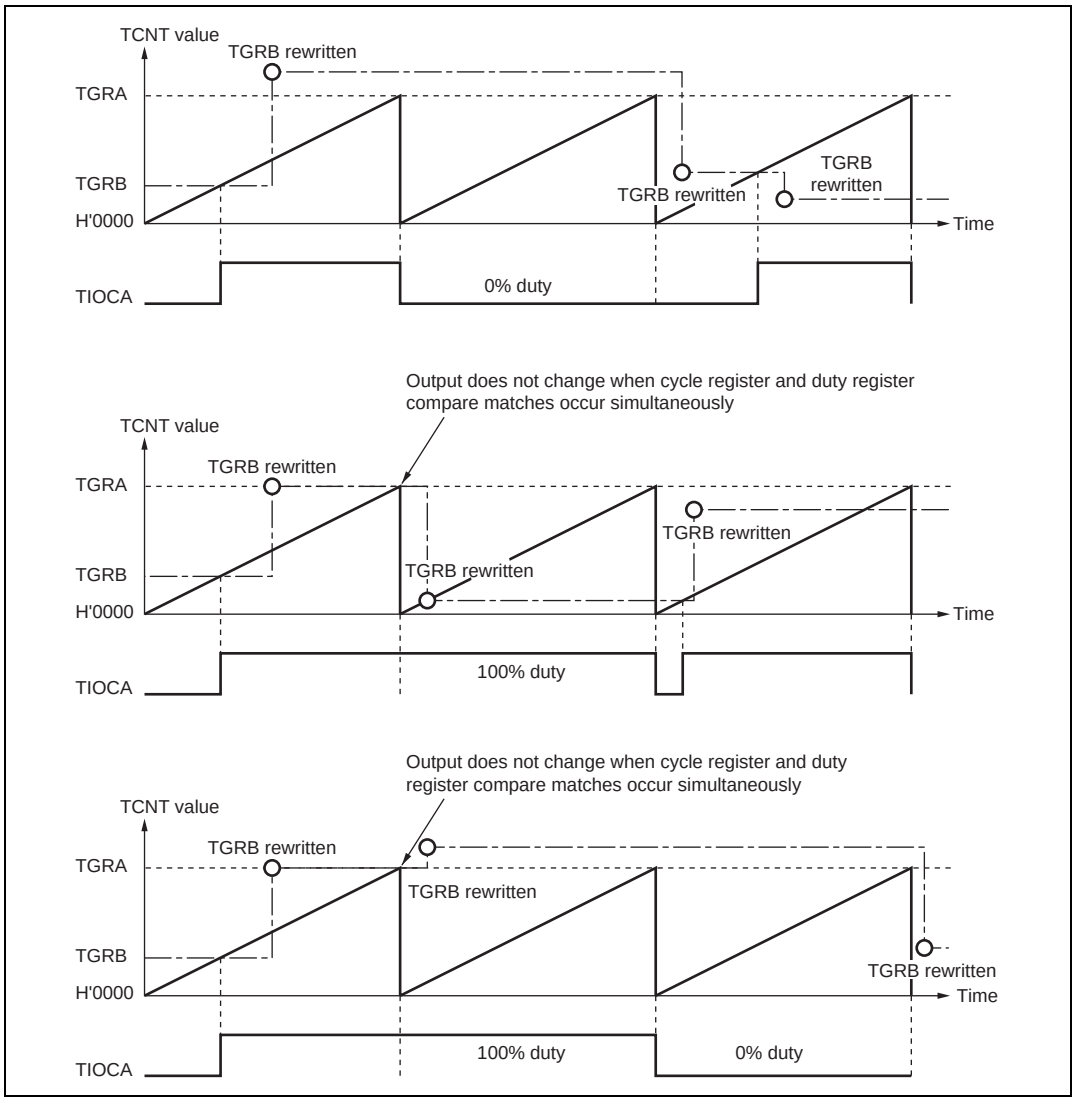


Figure 10.25 Example of PWM Mode Operation (3)

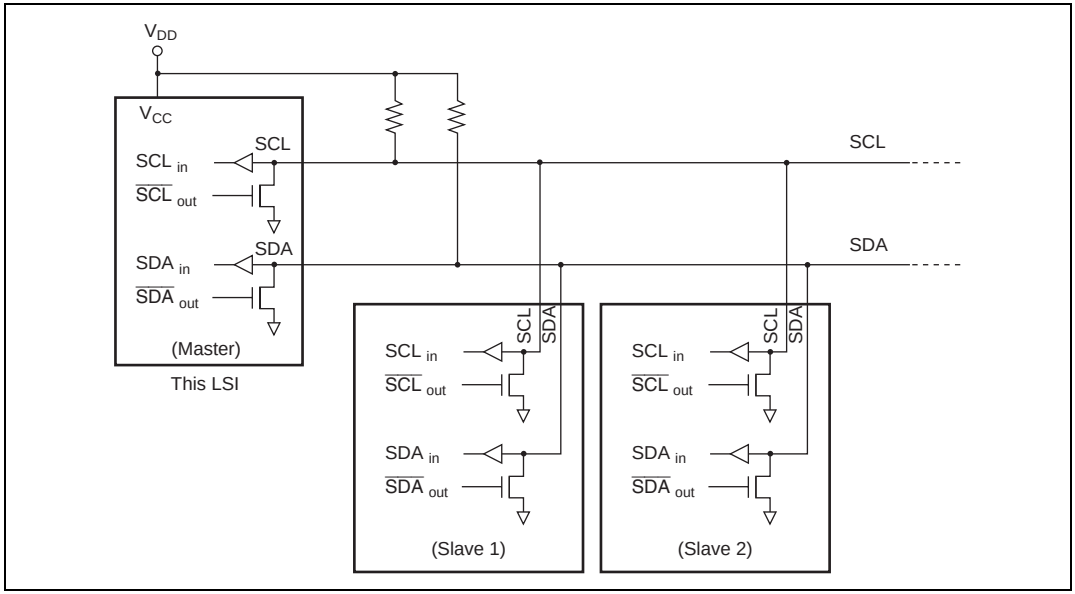


Figure 14.2 I²C Bus Interface Connections (Example: This LSI as Master)

14.2 Input/Output Pins

Table 14.1 shows the pin configuration for the I²C bus interface.

Table 14.1 Pin Configuration

Name	Abbreviation*1	I/O	Function
Serial clock	SCL0	I/O	IIC_0 serial clock input/output
Serial data	SDA0	I/O	IIC_0 serial data input/output
Serial clock*2	SCL1	I/O	IIC_1 serial clock input/output
Serial data*2	SDA1	I/O	IIC_1 serial data input/output

Notes: 1. In the text, the channel subscript is omitted, and only SCL and SDA are used.
2. Supported only by the H8S/2268 Group.

14.3.5 Serial Control Register X (SCRX)

SCRX controls the IIC operating modes.

Bit	Bit Name	Initial Value	R/W	Description
7	½	0	R/W	Reserved The initial value should not be changed.
6	IICX1*	0	R/W	I²C Transfer Rate Select 1 and 0
5	IICX0	0	R/W	Selects the transfer rate in master mode, together with bits CKS2 to CKS0 in ICMR. Refer to table 14.3. IICX1 controls IIC_1 and IICX0 controls IIC_0. Note: * In the H8S/2264 Group, this bit is reserved. The initial value should not be changed.
4	IICE	0	R/W	I²C Master Enable Controls CPU access to the IIC data register and control registers (ICCR, ICSR, ICDR/SARX, and ICMR/SAR). 0: CPU access to the IIC data register and control registers is disabled. 1: CPU access to the IIC data register and control registers is enabled.
3	FLSHE	0	R/W	For details on this bit, refer to section 20.5.7, Serial Control Register X (SCRX).
2 to 0	½	All 0	R/W	Reserved The initial value should not be changed.

Section 23 Power Supply Circuit

Section 25 Electrical Characteristics

Appendix C Package Dimensions 650