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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | H8S/2000 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, SCI, SmartCard |
| Peripherals | LCD, POR, PWM, WDT |
| Number of I/O | 67 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4V ~ 5.5V |
| Data Converters | A/D 10x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BFQFP |
| Supplier Device Package | 100-QFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/df2268fa20v |

## 2.6 Instruction Set

The H8S/2000 CPU has 65 types of instructions. The instructions are classified by function in table 2.1.

**Table 2.1 Instruction Classification**

| Function | Instructions | Size | Types |
|---|---|---|---|
| Data transfer | MOV | B/W/L | 5 |
| | POP*1, PUSH*1 | W/L | |
| | LDM*5, STM*5 | L | |
| | MOVFPE*3, MOVTPE*3 | B | |
| Arithmetic operations | ADD, SUB, CMP, NEG | B/W/L | 19 |
| | ADDX, SUBX, DAA, DAS | B | |
| | INC, DEC | B/W/L | |
| | ADDS, SUBS | L | |
| | MULXU, DIVXU, MULXS, DIVXS | B/W | |
| | EXTU, EXTS | W/L | |
| | TAS*4 | B | |
| Logic operations | AND, OR, XOR, NOT | B/W/L | 4 |
| Shift | SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR | B/W/L | 8 |
| Bit manipulation | BSET, BCLR, BNOT, BTST, BLD, BILD, BST, BIST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR | B | 14 |
| Branch | Bcc*2, JMP, BSR, JSR, RTS | — | 5 |
| System control | TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP | — | 9 |
| Block data transfer | EEPMOV | — | 1 |
| | | | Total: 65 |

Legend:

B: Byte

W: Word

L: Longword

Notes: 1. POP.W Rn and PUSH.W Rn are identical to MOV.W @SP+, Rn and MOV.W Rn, @-SP. POP.L ERn and PUSH.L ERn are identical to MOV.L @SP+, ERn and MOV.L ERn, @-SP.

2. Bcc is the general name for conditional branch instructions.
3. Cannot be used in this LSI.
4. Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction.
5. Only register ER0 to ER6 should be used when using the STM/LDM instruction.

**Table 2.11 Addressing Modes**

| No. | Addressing Mode | Symbol |
|---|---|---|
| 1 | Register direct | Rn |
| 2 | Register indirect | @ERn |
| 3 | Register indirect with displacement | @(d:16,ERn)/@(d:32,ERn) |
| 4 | Register indirect with post-increment<br>Register indirect with pre-decrement | @ERn+<br>@–ERn |
| 5 | Absolute address | @aa:8/@aa:16/@aa:24/@aa:32 |
| 6 | Immediate | #xx:8/#xx:16/#xx:32 |
| 7 | Program-counter relative | @(d:8,PC)/@(d:16,PC) |
| 8 | Memory indirect | @@aa:8 |

### 2.7.1 Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

### 2.7.2 Register Indirect—@ERn

The register field of the instruction code specifies an address register (ERn) which contains the address of the operand on memory. If the address is a program instruction address, the lower 24 bits are valid and the upper 8 bits are all assumed to be 0 (H'00).

### 2.7.3 Register Indirect with Displacement—@(d:16, ERn) or @(d:32, ERn)

A 16-bit or 32-bit displacement contained in the instruction is added to an address register (ERn) specified by the register field of the instruction, and the sum gives the address of a memory operand. A 16-bit displacement is sign-extended when added.

## 5.4 Interrupt Sources

### 5.4.1 External Interrupts

There are 14 external interrupts for the H8S/2268 Group: NMI, IRQ5 to IRQ3, IRQ1, IRQ0, and WKP7 to WKP0, and 13 external interrupts for the H8S/2264 Group: NMI, IRQ4, IRQ3, IRQ1, IRQ0, and WKP7 to WKP0. These interrupts can be used to restore this LSI from software standby mode.

**NMI Interrupt:** NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of the interrupt control mode or the status of the CPU interrupt mask bits. The NMIEG bit in SYSCR can be used to select whether an interrupt is requested at a rising edge or a falling edge on the NMI pin.

**IRQn Interrupts (H8S/2268 Group: n = 5 to 3, 1, and 0; H8S/2264 Group: n = 4, 3, 1, and 0):** IRQn interrupts are requested by an input signal at $\overline{\text{IRQn}}$ pins. IRQn interrupts have the following features:

- Using ISCR, it is possible to select whether an interrupt is generated by a low level, falling edge, rising edge, or both edges, at $\overline{\text{IRQn}}$ pins.
- Enabling or disabling of IRQn interrupt requests can be selected with IER.
- The interrupt priority level can be set with IPR. (H8S/2268 Group only)
- The status of IRQn interrupt requests is indicated in ISR. ISR flags can be cleared to 0 by software.

A block diagram of IRQn interrupts is shown in figure 5.3.

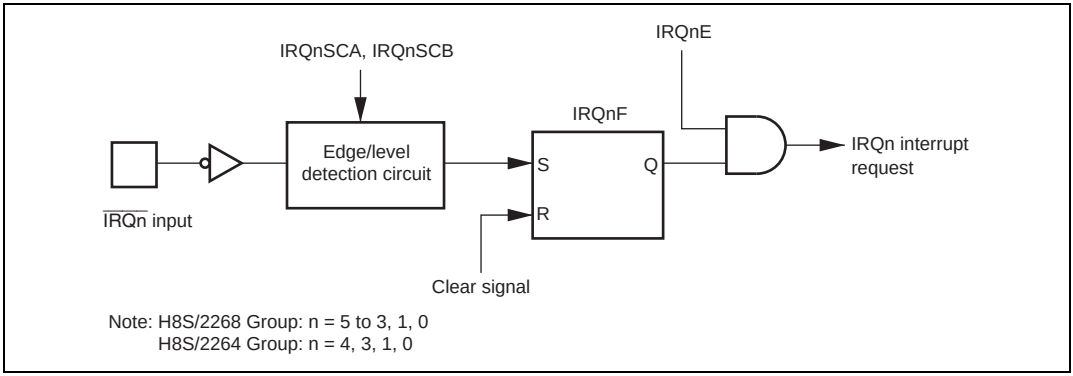


**Figure 5.3 Block Diagram of IRQn Interrupts**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 0 | BIEA | 0 | R/W | Break Interrupt Enable<br>When this bit is 1, the PC break interrupt request of channel A is enabled. |

Notes: 1. Only a 0 can be written to this bit to clear the flag.
2. Read the state wherein CMFA = 1 twice or more, when the CMFA is polled after inhibiting the PC break interruption.

### 6.2.4 Break Control Register B (BCRB)

BCRB is the channel B break control register. The bit configuration is the same as for BCRA.

## 6.3 Operation

The operation flow from break condition setting to PC break interrupt exception handling is shown in section 6.3.1, PC Break Interrupt Due to Instruction Fetch, and 6.3.2, PC Break Interrupt Due to Data Access, taking the example of channel A.

### 6.3.1 PC Break Interrupt Due to Instruction Fetch

1. Set the break address in BARA.
   For a PC break caused by an instruction fetch, set the address of the first instruction byte as the break address.
2. Set the break conditions in BCR.
   Set bit 6 (CDA) to 0 to select the CPU because the bus master must be the CPU for a PC break caused by an instruction fetch. Set the address bits to be masked to bits 3 to 5 (BAMA2 to 0). Set bits 1 and 2 (CSELA1 to 0) to 00 to specify an instruction fetch as the break condition. Set bit 0 (BIEA) to 1 to enable break interrupts.
3. When the instruction at the set address is fetched, a PC break request is generated immediately before execution of the fetched instruction, and the condition match flag (CMFA) is set.
4. After priority determination by the interrupt controller, PC break interrupt exception handling is started.

### 7.1.2 On-Chip Peripheral Module Access Timing (H'FFFDAC to H'FFFFBF)

Addresses H'FFFDAC to H'FFFFBF in the on-chip peripheral modules are accessed in two states. The data bus is either 8 bits or 16 bits wide, depending on the particular internal I/O register being accessed. For details, refer to section 24, List of Registers. Figure 7.2 shows access timing for the on-chip peripheral modules (H'FFFDAC to H'FFFFBF).

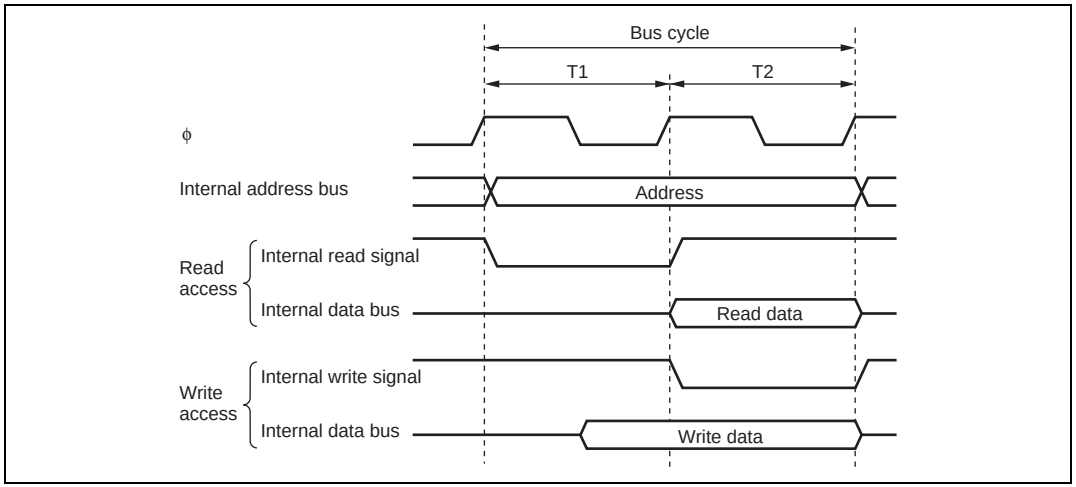


**Figure 7.2 On-Chip Peripheral Module Access Cycle (H'FFFDAC to H'FFFFBF)**

### 7.1.3 On-Chip Peripheral Module Access Timing (H'FFFC30 to H'FFFCA3)

Addresses H'FFFC30 to H'FFFCA3 on the on-chip peripheral modules and registers are accessed in four states. The data bus is either 8 bits or 16 bits wide, depending on the particular internal I/O register being accessed. For details, refer to section 24, List of Registers. Figure 7.3 shows access timing for the on-chip peripheral modules (H'FFFC30 to H'FFFCA3).

The on-chip module of which address is between H'FFFC30 to H'FFFCA3 includes LCD, DTMF*, TMR4*, ports H to L and ports M* and N*. The registers are WKP register and module stop control register D.

Note: * Supported only by the H8S/2268 Group.

### 8.2.7 DTC Enable Register (DTCER)

DTCER is comprised of seven registers; DTCERA to DTCERF and DTCERI, and is a register that specifies DTC activation interrupt sources. The correspondence between interrupt sources and DTCE bits is shown in table 8.1. For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR for reading and writing. If all interrupts are masked, multiple activation sources can be set at one time (only at the initial setting) by writing data after executing a dummy read on the relevant register.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | DTCE7 | 0 | R/W | DTC Activation Enable |
| 6 | DTCE6 | 0 | R/W | Setting this bit to 1 specifies a relevant interrupt source as a DTC activation source.<br>[Clearing conditions]<br>• When the DISEL bit is 1 and the data transfer has ended<br>• When the specified number of transfers have ended<br>• These bits are not cleared when the DISEL bit is 0 and the specified number of transfers have not been completed |
| 5 | DTCE5 | 0 | R/W | |
| 4 | DTCE4 | 0 | R/W | |
| 3 | DTCE3 | 0 | R/W | |
| 2 | DTCE2 | 0 | R/W | |
| 1 | DTCE1 | 0 | R/W | |
| 0 | DTCE0 | 0 | R/W | |

- PH0/COM1

  The pin function is switched as shown below according to the combination of the SGS3 to SGS0 bits in LPCR of the LCD controller/driver and the PH0DDR bit.

| SGS3 to SGS0 | B'0000 | | H8S/2268 Group: B'0001, B'001X or B'010X<br>H8S/2264 Group: B'001X or B'010X |
|---|---|---|---|
| PH0DDR | 0 | 1 | — |
| Pin functions | PH0 input pin | PH0 output pin | COM1 output pin |

Legend:
X: Don't care

## 9.8 Port J

Port J is an 8-bit I/O port and has the following registers.

- Port J data direction register (PJDDR)
- Port J data register (PJDR)
- Port J register (PORTJ)
- Port J pull-up MOS control register (PJPCR)
- Wakeup control register (WPCR)

### 9.8.3 Port J Register (PORTJ)

PORTJ shows port J pin states. This register cannot be modified.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | PJ7 | —* | R | If a port J read is performed while PJDDR bits are set to 1, the PJDR values are read. If a port J read is performed while PADDR bits are cleared to 0, the pin states are read. |
| 6 | PJ6 | —* | R | |
| 5 | PJ5 | —* | R | |
| 4 | PJ4 | —* | R | |
| 3 | PJ3 | —* | R | |
| 2 | PJ2 | —* | R | |
| 1 | PJ1 | —* | R | |
| 0 | PJ0 | —* | R | |

Note: * Determined by the states of pins PJ7 to PJ0.

### 9.8.4 Port J Pull-Up MOS Control Register (PJPCR)

PJPCR controls the input pull-up MOS function for each bit.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | PJ7PCR | 0 | R/W | When a pin is specified as an input port, setting the corresponding bit to 1 turns on the input pull-up MOS for that pin. |
| 6 | PJ6PCR | 0 | R/W | |
| 5 | PJ5PCR | 0 | R/W | |
| 4 | PJ4PCR | 0 | R/W | |
| 3 | PJ3PCR | 0 | R/W | |
| 2 | PJ2PCR | 0 | R/W | |
| 1 | PJ1PCR | 0 | R/W | |
| 0 | PJ0PCR | 0 | R/W | |

### 9.8.7 Input Pull-Up MOS Function

Port J has a built-in input pull-up MOS function that can be controlled by software. Input pull-up MOS can be specified as on or off on an individual bit basis.

When port J is set to port input and wakeup input, PJDDR is cleared to 0, and then PJPCR is set to 1, the input pull-up MOS is turned on.

The input pull-up MOS function is in the off state after a reset, and in hardware standby mode. The prior state is retained in software standby mode.

Table 9.2 summarizes the input pull-up MOS states in port J.

**Table 9.2 Input Pull-Up MOS States (Port J)**

| Pin States | Reset | Hardware Standby Mode | Software Standby Mode | In Other Operations |
|---|---|---|---|---|
| Segment output and port output | OFF | OFF | OFF | OFF |
| Port input and wakeup input | | | ON/OFF | ON/OFF |

Legend:
OFF : Input pull-up MOS is always off.
ON/OFF : On when PJDDR = 0 and PJPCR = 1; otherwise off.

## 9.9 Port K

Port K is an 8-bit I/O port and has the following registers.

- Port K data direction register (PKDDR)
- Port K data register (PKDR)
- Port K register (PORTK)

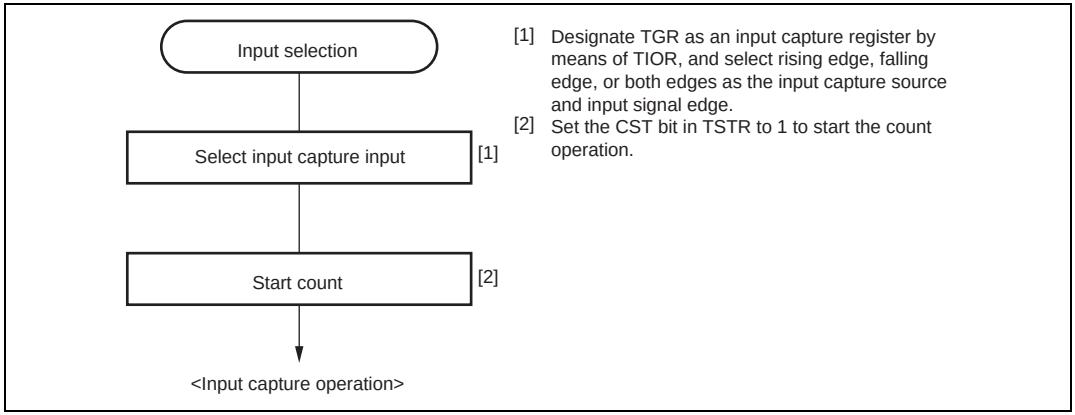


**Figure 10.13 Example of Input Capture Operation Setting Procedure**

2. Example of input capture operation

   Figure 10.14 shows an example of input capture operation.

   In this example both rising and falling edges have been selected as the TIOCA pin input capture input edge, the falling edge has been selected as the TIOCB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT.

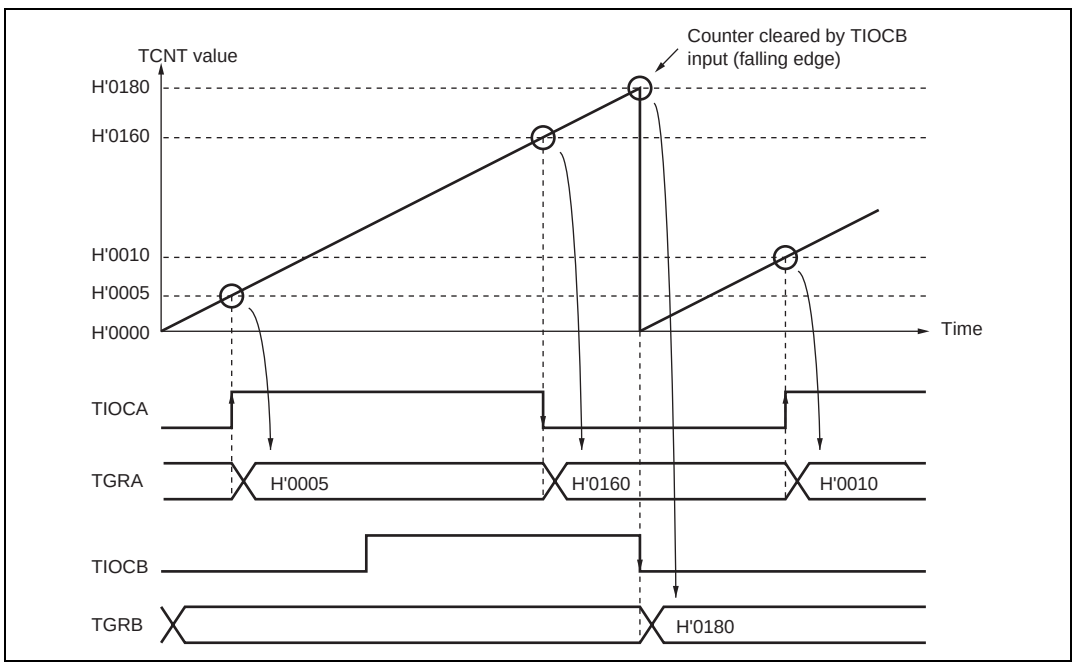


**Figure 10.14 Example of Input Capture Operation**

### 10.10.6 Contention between TGR Write and Compare Match

If a compare match occurs in the T2 state of a TGR write cycle, the TGR write takes precedence and the compare match signal is inhibited. A compare match does not occur even if the previous value is written.

Figure 10.48 shows the timing in this case.

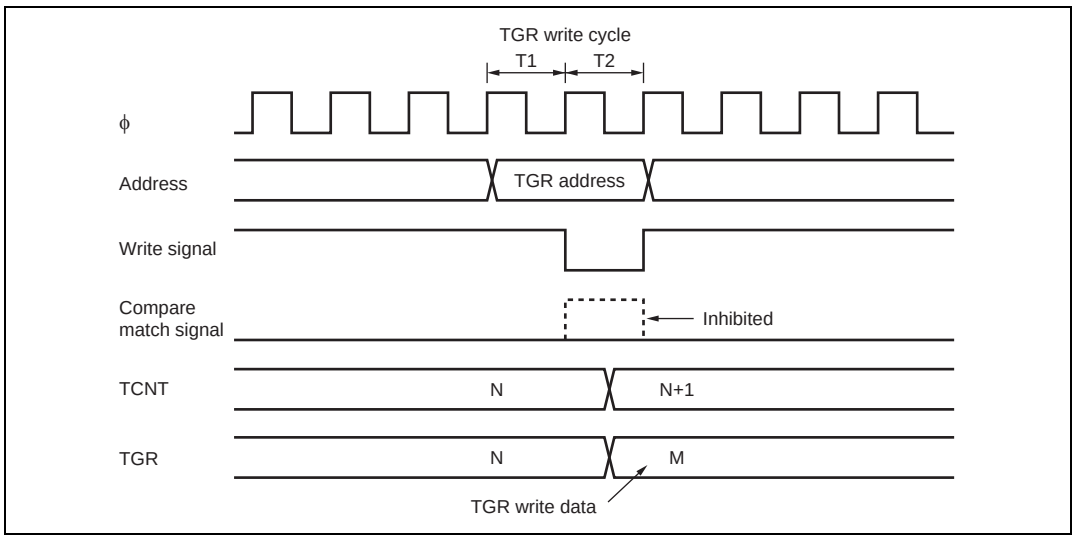


**Figure 10.48 Contention between TGR Write and Compare Match**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 5 | ORER | 0 | R/(W)*1 | Overrun Error<br>Indicates that an overrun error occurred during reception, causing abnormal termination.<br>[Setting condition]<br>When the next serial reception is completed while RDRF = 1<br>The receive data prior to the overrun error is retained in RDR, and the data received subsequently is lost. Also, subsequent serial reception cannot be continued while the ORER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued either.<br>[Clearing condition]<br>When 0 is written to ORER after reading ORER = 1<br>The ORER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0. |
| 4 | FER | 0 | R/(W)*1 | Framing Error<br>Indicates that a framing error occurred during reception in asynchronous mode, causing abnormal termination.<br>[Setting condition]<br>When the stop bit is 0<br>In 2 stop bit mode, only the first stop bit is checked for a value to 1; the second stop bit is not checked. If a framing error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the FER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either.<br>[Clearing condition]<br>When 0 is written to FER after reading FER = 1<br>In 2-stop-bit mode, only the first stop bit is checked.<br>The FER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 3 | PER | 0 | R/(W)*1 | Parity Error<br>Indicates that a parity error occurred during reception using parity addition in asynchronous mode, causing abnormal termination.<br>[Setting condition]<br>When a parity error is detected during reception<br>If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either.<br>[Clearing condition]<br>When 0 is written to PER after reading PER = 1<br>The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0. |
| 2 | TEND | 1 | R | Transmit End<br>Indicates that transmission has been ended.<br>[Setting conditions]<br>• When the TE bit in SCR is 0<br>• When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character<br>[Clearing conditions]<br>• When 0 is written to TDRE after reading TDRE = 1<br>• When the DTC*2 is activated by a TXI interrupt request and transfer transmission data to TDR (H8S/2268 Group only) |
| 1 | MPB | 0 | R | Multiprocessor Bit<br>MPB stores the multiprocessor bit in the receive data. When the RE bit in SCR is cleared to 0 its previous state is retained. |
| 0 | MPBT | 0 | R/W | Multiprocessor Bit Transfer<br>MPBT stores the multiprocessor bit to be added to the transmit data. |

Notes: 1. Only a 0 can be written to this bit, to clear the flag.
2. This bit is cleared by DTC only when DISEL = 0 with the transfer counter other than 0.

## 20.6 On-Board Programming Modes

When pins are set to on-board programming mode, program/erase/verify operations can be performed on the on-chip flash memory. There are two on-board programming modes: boot mode and user program mode. The pin settings for transition to each of these modes are shown in table 20.3. For a diagram of the transitions to the various flash memory modes, see figure 20.2.

**Table 20.3 Setting On-Board Programming Modes**

| FWE | MD2 | MD1 | Mode Setting |
|---|---|---|---|
| 1 | 1 | 0 | Boot Mode |
| 1 | 1 | 1 | User program mode |
| 0 | 1 | 1 | User mode |

### 20.6.1 Boot Mode

Table 20.4 shows the boot mode operations between reset end and branching to the programming control program.

1. When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. Prepare a programming control program in accordance with the description in section 20.8, Flash Memory Programming/Erasing.

   In boot mode, if any data has been programmed into the flash memory (if all data is not 1), all flash memory blocks are erased. Boot mode is for use when user program mode is unavailable, such as the first time on-board programming is performed, or if the program activated in user program mode is accidentally erased.
2. SCI_0 should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity.
3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI_0 bit rate to match that of the host. The reset should end with the RxD pin high. The RxD and TxD pins should be pulled up on the board if necessary. After the reset is complete, it takes approximately 100 states before the chip is ready to measure the low-level period.
4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the completion of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between

# Section 21 Clock Pulse Generator

This LSI has an on-chip clock pulse generator that generates the system clock (ϕ), the bus master clock, and internal clocks. The clock pulse generator consists of an oscillator, duty adjustment circuit, clock selection circuit, medium-speed clock divider, bus master clock selection circuit, subclock oscillator, and wave formation circuit. A block diagram of the clock pulse generator is shown in figure 21.1.

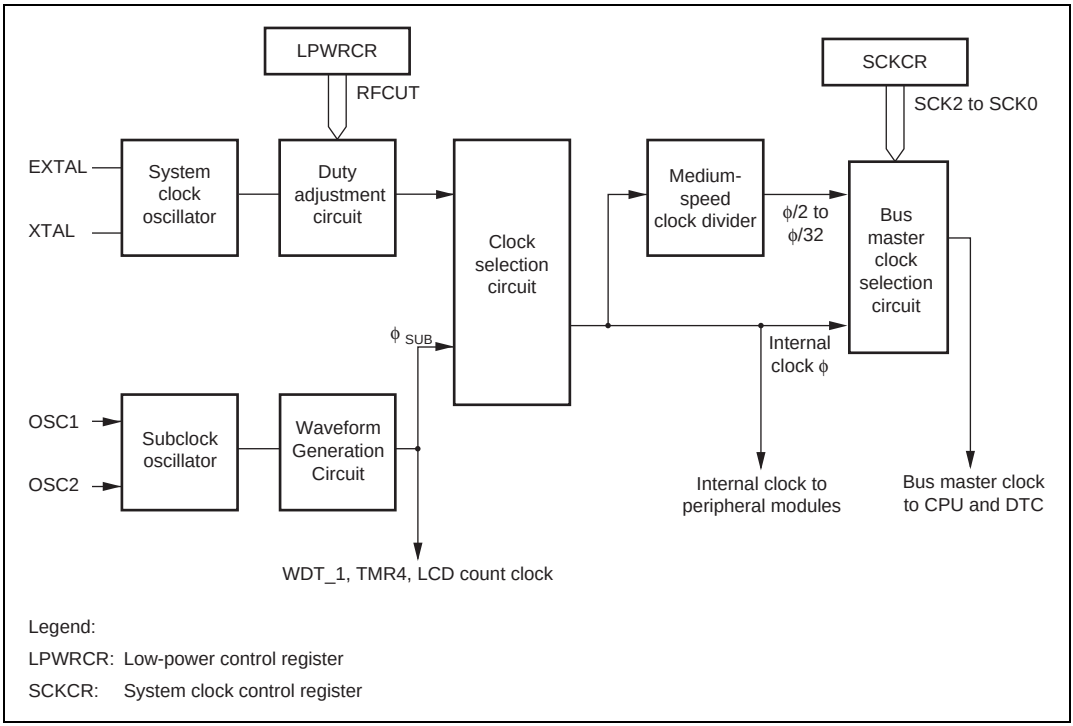


**Figure 21.1 Block Diagram of Clock Pulse Generator**

Frequency changes are performed by software by settings in the low-power control register (LPWRCR) and system clock control register (SCKCR).

**Table 21.1 Damping Resistance Value**

| Frequency (MHz) | 2 | 4 | 6 | 8 | 10 | 12 | 16 | 20 |
|---|---|---|---|---|---|---|---|---|
| $R_d$ (Ω) | 1 k | 500 | 300 | 200 | 100 | 0 | 0 | 0 |

Figure 21.3 shows the equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in table 21.2.

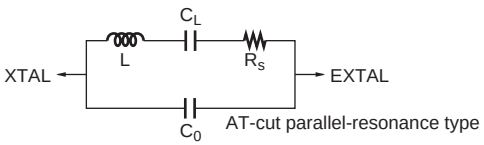


**Figure 21.3 Crystal Resonator Equivalent Circuit**

**Table 21.2 Crystal Resonator Characteristics**

| Frequency (MHz) | 2 | 4 | 6 | 8 | 10 | 12 | 16 | 20 |
|---|---|---|---|---|---|---|---|---|
| $R_S$ max. (Ω) | 500 | 120 | 100 | 80 | 60 | 60 | 50 | 40 |
| $C_0$ max. (pF) | 7 | 7 | 7 | 7 | 7 | 7 | 7 | 7 |

### 21.2.2 External Clock Input

An external clock signal can be input as shown in the examples in figure 21.4. If the XTAL pin is left open, ensure that stray capacitance does not exceed 10 pF. When complementary clock is input to the XTAL pin, the external clock input should be fixed high in standby mode, subactive mode, subsleep mode, or watch mode.

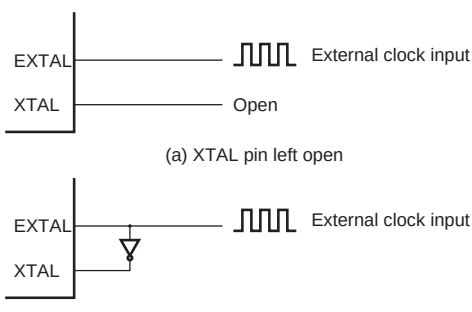


**Figure 21.4 External Clock Input (Examples)**

## 22.7 Watch Mode

### 22.7.1 Transition to Watch Mode

CPU operation makes a transition to watch mode when the SLEEP instruction is executed in high-speed mode or sub-active mode with SBYCR SSBY=1, LPWRCR DTON = 0, and TCSR_1 (WDT_1) PSS = 1.

In watch mode, the CPU is stopped and peripheral modules other than WDT_1, TMR_4*, and LCD are also stopped. The contents of the CPU's internal registers, the data in internal RAM, and the statuses of the internal peripheral modules (excluding the A/D converter) and I/O ports are retained. To make a transition to watch mode, bits SCK2 to SCK0 in SCKCR must be set to 0.

Note: * Supported only by the H8S/2268 Group.

### 22.7.2 Exiting Watch Mode

Watch mode is exited by any interrupt (WOVI1 interrupt, OVI4 to OVI7 interrupts*, NMI pin, or $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ4}}$, $\overline{\text{IRQ5}}$*, or $\overline{\text{WKP0}}$ to $\overline{\text{WKP7}}$), or signals at the $\overline{\text{RES}}$, or $\overline{\text{STBY}}$ pins.

- Exiting Watch Mode by Interrupts

  When an interrupt occurs, watch mode is exited and a transition is made to high-speed mode or medium-speed mode when the LPWRCR LSON bit = 0 or to sub-active mode when the LSON bit = 1. When a transition is made to high-speed mode, a stable clock is supplied to all LSI circuits and interrupt exception processing starts after the time set in SBYCR STS2 to STS0 has elapsed. In the case of IRQ0, IRQ1, IRQ3, IRQ4, IRQ5*, and WKP0 to WKP7 interrupts, no transition is made from watch mode if the corresponding enable bit/pin function switching bit has been cleared to 0, and, in the case of interrupts from the internal peripheral modules, the interrupt enable register has been set to disable the reception of that interrupt, or is masked by the CPU.

  See section 22.4.3, Oscillation Settling Time after Clearing Software Standby Mode, for how to set the oscillation settling time when making a transition from watch mode to high-speed mode.
- Exiting Watch Mode by $\overline{\text{RES}}$ pins

  For exiting watch mode by the $\overline{\text{RES}}$ pins, see section 22.4.2, Clearing Software Standby Mode.
- Exiting Watch Mode by $\overline{\text{STBY}}$ pin

  When the $\overline{\text{STBY}}$ pin level is driven low, a transition is made to hardware standby mode.

Note: * Supported only by the H8S/2268 Group.

## 24.2 Register Bits

| Register Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| MRA[*1] | SM1 | SM0 | DM1 | DM0 | MD1 | MD0 | DTS | Sz | DTC |
| SAR[*1] | | | | | | | | | |
| MRB[*1] | CHNE | DISEL | — | — | — | — | — | — | |
| DAR[*1] | | | | | | | | | |
| CRA[*1] | | | | | | | | | |
| CRB[*1] | | | | | | | | | |
| LPCR | DTS1 | DTS0 | CMX | — | SGS3 | SGS2 | SGS1 | SGS0 | LCD |
| LCR | — | PSW | ACT | DISP | CKS3 | CKS2 | CKS1 | CKS0 | |
| LCR2 | LCDAB | — | HCKS[*2] | SUPS[*2] | CDS3 | CDS2 | CDS1 | CDS0 | |
| LCD RAM | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| MSTPCRD | MSTPD7 | MSTPD6 | MSTPD5 | MSTPD4 | MSTPD3 | MSTPD2 | MSTPD1 | MSTPD0 | SYSTEM |
| DTCR[*1] | DTEN | — | CLOE | RWOE | CLF1 | CLF0 | RWF1 | RWF0 | DTMF |
| DTLR[*1] | — | — | DTL5 | DTL4 | DTL3 | DTL2 | DTL1 | DTL0 | |
| TCR_4[*1] | ARSL | OVF | OVIE | — | — | CKS2 | CKS1 | CKS0 | TMR_4 |
| TCR_5[*1] | ARSL | OVF | OVIE | — | — | CKS2 | CKS1 | CKS0 | |
| TCR_6[*1] | ARSL | OVF | OVIE | — | — | CKS2 | CKS1 | CKS0 | |
| TCR_7[*1] | ARSL | OVF | OVIE | — | — | CKS2 | CKS1 | CKS0 | |
| TCNT_4(R)/ TLR_4(W)[*1] | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TCNT_5(R)/ TLR_5(W)[*1] | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TCNT_6(R)/ TLR_6(W)[*1] | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |
| TCNT_7(R)/ TLR_7(W)[*1] | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | |

### 25.2.7 DTMF Characteristics

Table 25.12 lists the DTMF characteristics.

**Table 25.12 DTMF Characteristics**

Condition A (F-ZTAT version): $V_{CC}$ = 3.0 V to 5.5 V, $AV_{CC}$ = 2.7 V to 5.5 V, $V_{ref}$ = 2.7 V to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 2 to 13.2 MHz, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications)

Condition C (F-ZTAT version): $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 2.7 V*1 to 5.5 V, $V_{ref}$ = 2.7 V*1 to $AV_{CC}$, $V_{SS}$ = $AV_{SS}$ = 0 V, $\phi$ = 10 to 20.4 MHz, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications)

| Item | Symbol | Applicable Pins | Test Conditions | Standard Value | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| DTMF output voltage (Row side) | $V_{OR}$ | TONED | $AV_{cc}$-GND = 2.7 V<br>$R_L$ = 100 kΩ | 750 | 924 | — | mVrms | Figure 25.12*2 |
| DTMF output voltage (Column side) | $V_{OC}$ | TONED | $AV_{cc}$ - GND = 2.7 V<br>$R_L$ = 100 kΩ | 770 | 945 | — | mVrms | Figure 25.12*2 |
| DTMF output distortion | % DISDT | TONED | $AV_{cc}$ – GND = 2.7 V<br>$R_L$ = 100 kΩ | — | 3 | 7 | % | Figure 25.12 |
| DTMF output ratio | $dB_{CR}$ | TONED | $AV_{cc}$ – GND = 2.7 V<br>$R_L$ = 100 kΩ | — | 2.5 | — | dB | Figure 25.12 |

Notes: 1. When $AV_{cc}$ = 2.7 to 4.0 V, and $V_{ref}$ = 2.7 to 4.0 V, DTMF is only available.
2. $V_{OR}$ and $V_{cc}$ are output voltages when a single waveform is output.

**Table 25.21 I²C Bus Timing**

Conditions: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, $\phi$ = 5 MHz to maximum operating frequency, $T_a$ = –20°C to +75°C (regular specifications), $T_a$ = –40°C to +85°C (wide-range specifications)

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | Remarks |
|---|---|---|---|---|---|---|---|
| SCL input cycle time | $t_{SCL}$ | 12 $t_{cyc}$ | — | — | ns | | Figure 25.11 |
| SCL input high pulse width | $t_{SCLH}$ | 3 $t_{cyc}$ | — | — | ns | | |
| SCL input low pulse width | $t_{SCLL}$ | 5 $t_{cyc}$ | — | — | ns | | |
| SCL, SDA input rise time | $t_{Sr}$ | — | — | 7.5 $t_{cyc}$ * | ns | | |
| SCL, SDA input fall time | $t_{Sf}$ | — | — | 300 | ns | | |
| SCL, SDA input spike pulse elimination time | $t_{SP}$ | — | — | 1 $t_{cyc}$ | ns | | |
| SDA input bus free time | $t_{BUF}$ | 5 $t_{cyc}$ | — | — | ns | | |
| Start condition input hold time | $t_{STAH}$ | 3 $t_{cyc}$ | — | — | ns | | |
| Retransmission start condition input setup time | $t_{STAS}$ | 3 $t_{cyc}$ | — | — | ns | | |
| Stop condition input setup time | $t_{STOS}$ | 3 $t_{cyc}$ | — | — | ns | | |
| Data input setup time | $t_{SDAS}$ | 0.5 $t_{cyc}$ | — | — | ns | | |
| Data input hold time | $t_{SDAH}$ | 0 | — | — | ns | | |
| SCL, SDA load capacitance | $C_b$ | — | — | 400 | pF | | |

Note: * $t_{Sr}$ can be set to 7.5 $t_{cyc}$ or 17.5 $t_{cyc}$ according to the clock used for the I²C module. For details, see section 14.5, Usage Notes.