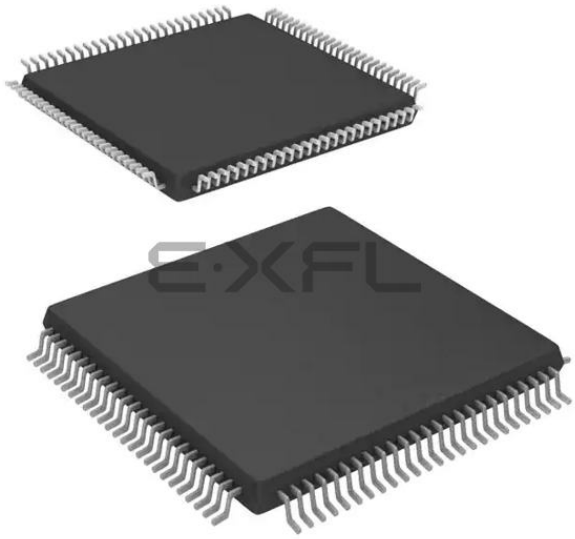

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2268te20v

Tables

Section 8 Data Transfer Controller (DTC)

Section 9 I/O Ports

Section 10 16-Bit Timer Pulse Unit (TPU)

5.3.4 IRQ Sense Control Registers H and L (ISCRH and ISCRL)

The ISCR registers select the source that generates an interrupt request at pins $\overline{\text{IRQn}}$ (H8S/2268 Group: n = 5 to 3, 1, 0; H8S/2264 Group: n = 4, 3, 1, 0). Specifiable sources are the falling edge, rising edge, or both edge detection, and level sensing.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R/W	Reserved The write value should always be 0.
11	IRQ5SCB	0	R/W	H8S/2268 Group:
10	IRQ5SCA	0	R/W	IRQ5 Sense Control B IRQ5 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ5}}$ input level low 01: Interrupt request generated at falling edge of $\overline{\text{IRQ5}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ5}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ5}}$ input H8S/2264 Group: Reserved The write value should always be 0.
9	IRQ4SCB	0	R/W	IRQ4 Sense Control B
8	IRQ4SCA	0	R/W	IRQ4 Sense Control A 00: Interrupt request generated at $\overline{\text{IRQ4}}$ input level low 01: Interrupt request generated at falling edge of $\overline{\text{IRQ4}}$ input 10: Interrupt request generated at rising edge of $\overline{\text{IRQ4}}$ input 11: Interrupt request generated at both falling and rising edges of $\overline{\text{IRQ4}}$ input

6.4 Usage Notes

6.4.1 Module Stop Mode Setting

PBC operation can be disabled or enabled using the module stop control register. The initial setting is for PBC operation to be halted. Register access is enabled by clearing module stop mode. For details, refer to section 22, Power-Down Modes.

6.4.2 PC Break Interrupts

The PC break interrupt is shared by channels A and B. The channel from which the request was issued must be determined by the interrupt handler.

6.4.3 CMFA and CMFB

The CMFA and CMFB flags are not automatically cleared to 0, so 0 must be written to CMFA or CMFB after first reading the flag while it is set to 1. If the flag is left set to 1, another interrupt will be requested after interrupt handling ends.

6.4.4 PC Break Interrupt when DTC Is Bus Master

A PC break interrupt generated when the DTC is the bus master is accepted after the bus has been transferred to the CPU by the bus controller.

6.4.5 PC Break Set for Instruction Fetch at Address Following BSR, JSR, JMP, TRAPA, RTE, or RTS Instruction

When a PC break is set for an instruction fetch at an address following a BSR, JSR, JMP, TRAPA, RTE, or RTS instruction:

Even if the instruction at the address following a BSR, JSR, JMP, TRAPA, RTE, or RTS instruction is fetched, it is not executed, and so a PC break interrupt is not generated by the instruction fetch at the next address.

8.5.5 Interrupts

An interrupt request is issued to the CPU when the DTC has completed the specified number of data transfers, or a data transfer for which the DISEL bit was set to 1. In the case of interrupt activation, the interrupt set as the activation source is generated. These interrupts to the CPU are subject to CPU mask level and interrupt controller priority level control.

In the case of software activation, a software-activated data transfer end interrupt (SWDTEND) is generated.

When the DISEL bit is 1 and one data transfer has been completed, or the specified number of transfers have been completed, after data transfer ends the SWDTE bit is held at 1 and an SWDTEND interrupt is generated. The interrupt handling routine will then clear the SWDTE bit to 0.

When the DTC is activated by software, an SWDTEND interrupt is not generated during a data transfer wait or during data transfer even if the SWDTE bit is set to 1.

8.5.6 Operation Timing

Figures 8.10 to 8.12 show the DTC operation timings.

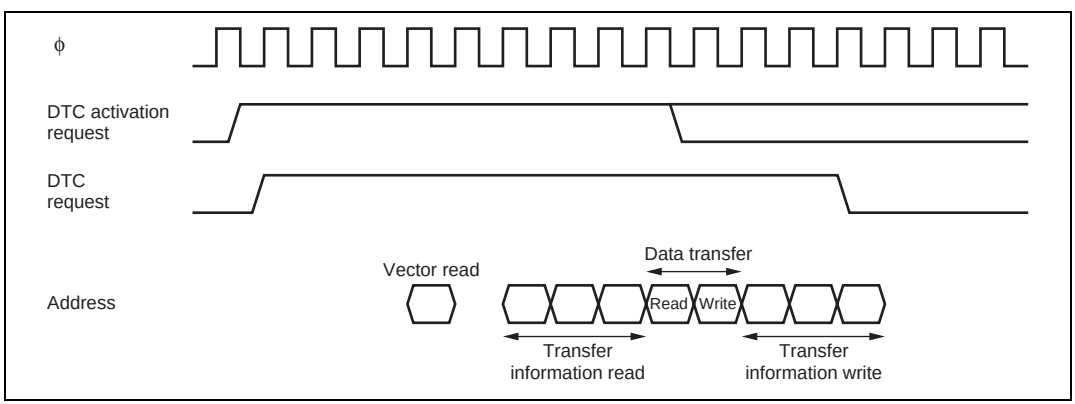

Figure 8.10 DTC Operation Timing (Example in Normal Mode or Repeat Mode)

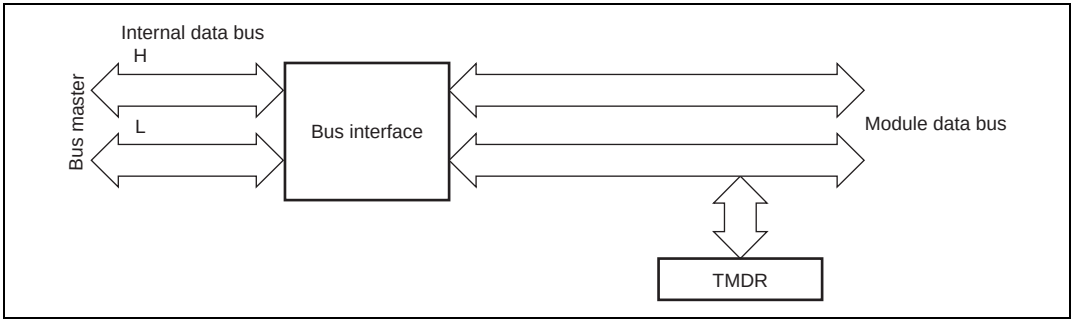

Figure 10.5 8-Bit Register Access Operation [Bus Master ↔ TMDR (Lower 8 Bits)]

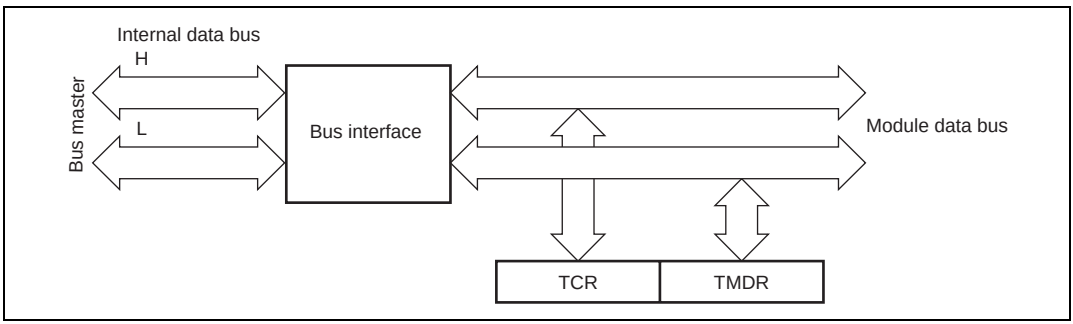

Figure 10.6 8-Bit Register Access Operation [Bus Master ↔ TCR and TMDR (16 Bits)]

10.10.7 Contention between Buffer Register Write and Compare Match (H8S/2268 Group Only)

If a compare match occurs in the T2 state of a TGR write cycle, the data that is transferred to TGR by the buffer operation will be that in the buffer prior to the write.

Figure 10.49 shows the timing in this case.

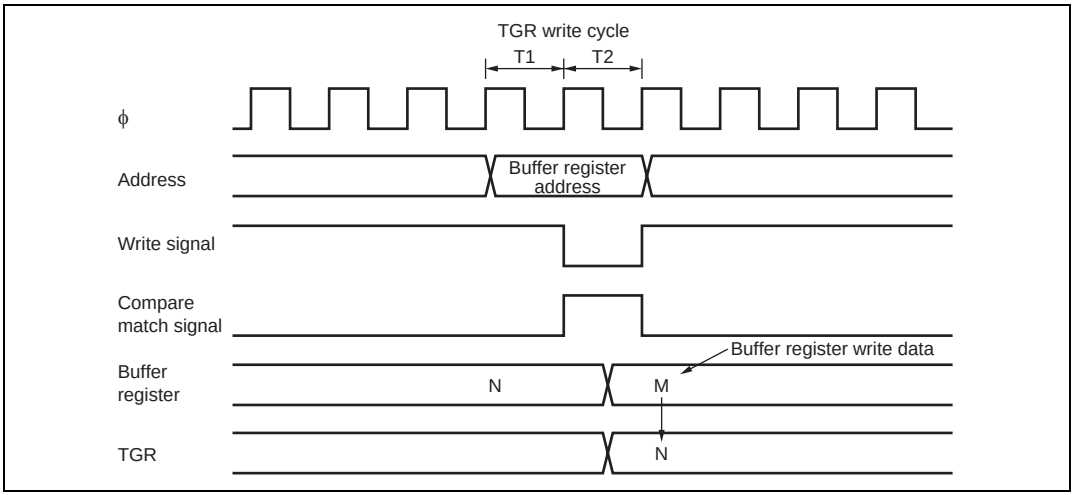

Figure 10.49 Contention between Buffer Register Write and Compare Match

11.10 Register Descriptions

The 8-bit reload timer has the following registers. For details on the module stop control register, refer to section 22.1.2, Module Stop Control Registers A to D (MSTPCRA to MSTPCRD).

- Timer control register (TCR)
- Timer Counter (TCNT)
- Timer reload register (TLR)

TCNT or TLR can operate as a 16-bit timer using TCNT_4 or TLR_4 (TCNT_6 or TLR_6) as the upper half and TCNT_5 or TLR_5 (TCNT_7 or TLR_7) as the lower half.

11.10.1 Timer Control Registers 4 to 7 (TCR_4 to TCR_7)

TCR selects the automatic reload function and TCNT clock source, and controls interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	ARSL	0	R/W	Automatic Reload Function Select Selects the automatic reload function 0: The interval function is selected 1: The automatic reload function is selected
6	OVF	0	R/(W)*	Timer Overflow Flag Indicates that TCNT overflows from H'FF to H'00. 0: [Clearing condition] Read OVF when OVF = 1, then write 0 in OVF 1: [Setting condition] When TCNT overflows from H'FF to H'00
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether the OVF interrupt request (OVI) is enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt request (OVI) is disabled 1: OVF interrupt request (OVI) is enabled
4, 3	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.

11.11.2 Automatic Reload Timer Operation

When the ARSL bit in TCR is set to 1, the timer operates as an automatic reload timer.

When a reload value is set to TLR, the value is also loaded to TCNT simultaneously, and TCNT starts incrementation from the value.

If a clock is input after the TCNT count value reaches H'FF, the timer overflows, the TLR value is written to TCNT, and incrementation is continued from the value. Therefore, the overflow cycle can be set within the range from 1 to 256, using a TLR value.

Clock sources and interrupts in automatic reload operation are the same as those in interval operation. If TLR is re-set during automatic reload operation, the value is also set to TCNT.

This operation timing is shown in figure 11.15.

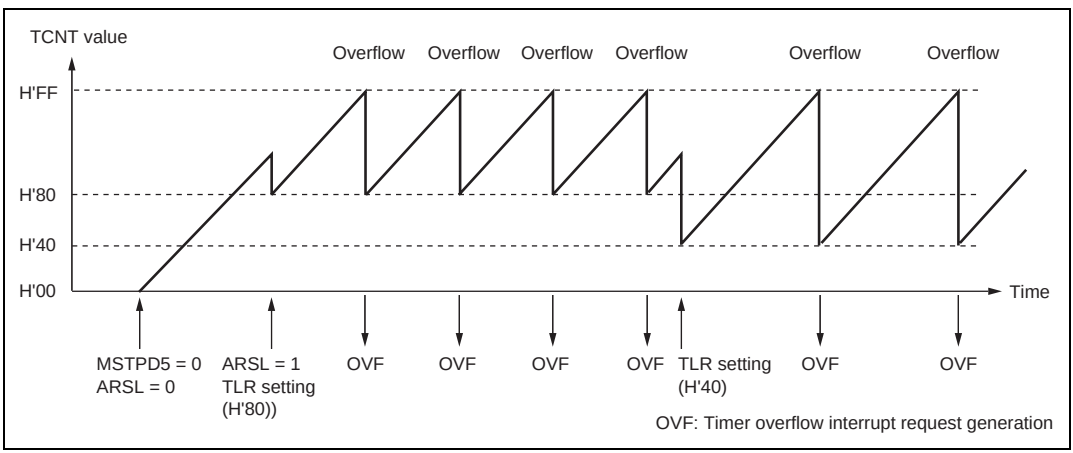

Figure 11.15 Operation in Automatic Reload Timer Mode

11.11.3 Cascaded Connection

- Read of TCNT

  The channel relationship for cascaded connection is shown in figure 11.16.
  When accessing beyond the word area, for example, when a cascaded connection including channels 5 and 6 is created as shown in (3), and (6) to (8) in the figure, the counter value of the lower channel is read when TCNT5 is read, and the data is stored in the TCNT register.

  For case (7) where channels 5 to 7 are cascaded, the counter values of channels 6 and 7 are read when TCNT5 is read, and the data is stored in TCNT6/7 registers. Accordingly, when reading cascaded TCNT, read from the upper channel.

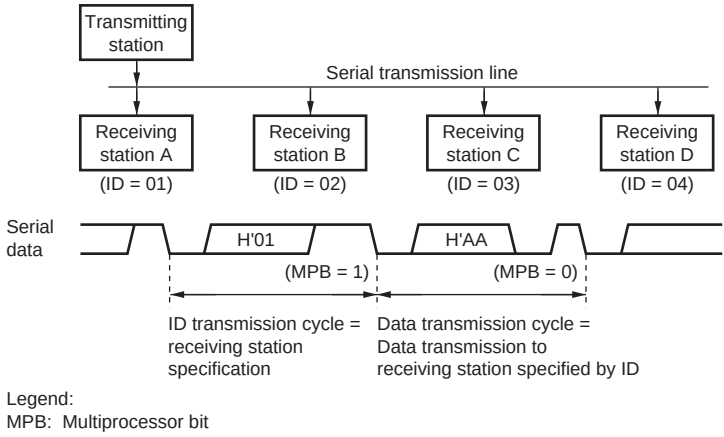

Figure 13.13 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

3. 8-bit data is sent from the TxD pin synchronized with the output clock when output clock mode has been specified, and synchronized with the input clock when use of an external clock has been specified.
4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial transmission of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag maintains the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI interrupt request is generated. The SCK pin is fixed high.

Figure 13.20 shows a sample flow chart for serial data transmission. Even if the TDRE flag is cleared to 0, transmission will not start while a receive error flag (ORER, FER, or PER) is set to 1. Make sure that the receive error flags are cleared to 0 before starting transmission. Note that clearing the RE bit to 0 does not clear the receive error flags.

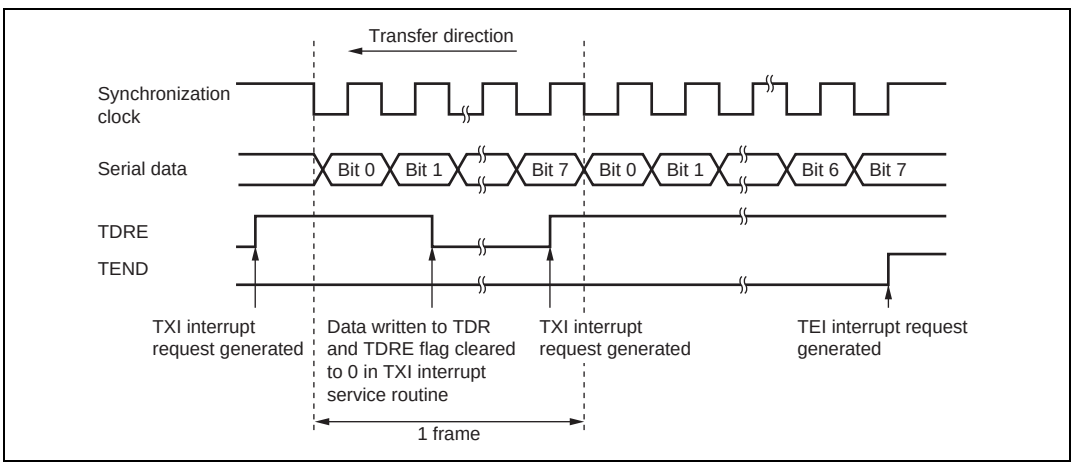

Figure 13.19 Sample SCI Transmission Operation in Clocked Synchronous Mode

13.6.4 Serial Data Reception (Clocked Synchronous Mode)

Figure 13.21 shows an example of SCI operation for reception in clocked synchronous mode. In serial reception, the SCI operates as described below.

1. The SCI performs internal initialization synchronous with a synchronous clock input or output, starts receiving data, and stores the received data in RSR.
2. If an overrun error occurs (when reception of the next data is completed while the RDRF flag in SSR is still set to 1), the ORER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this time, an ERI interrupt request is generated, receive data is not transferred to RDR, and the RDRF flag remains to be set to 1.
3. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI interrupt request is generated. Continuous reception is possible because the RXI interrupt routine reads the receive data transferred to RDR before reception of the next receive data has finished.

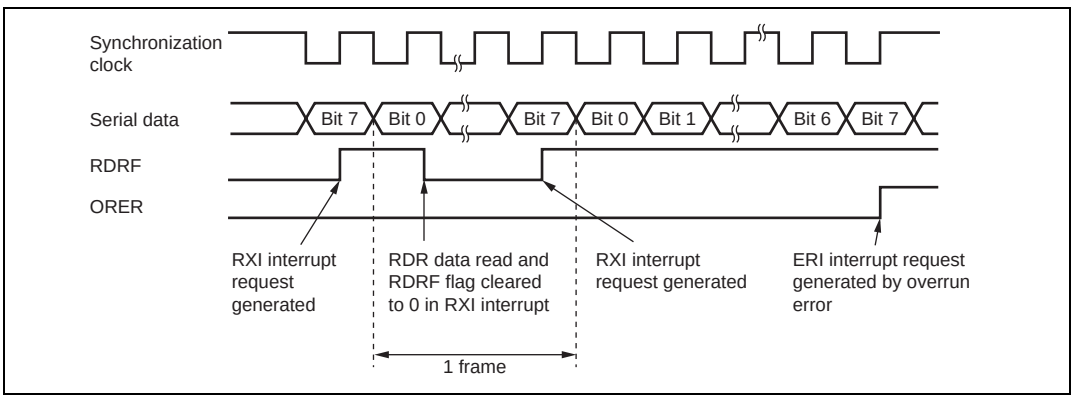

Figure 13.21 Example of SCI Operation in Reception

Reception cannot be resumed while a receive error flag is set to 1. Accordingly, clear the ORER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 13.22 shows a sample flow chart for serial data reception.

An overrun error occurs or synchronous clocks are output until the RE bit is cleared to 0 when an internal clock is selected and only receive operation is possible. When a transmission and reception will be carried out in a unit of one frame, be sure to carry out a dummy transmission with only one frame by the simultaneous transmit and receive operations at the same time.

20.8.1 Program/Program-Verify

When writing data or programs to the flash memory, the program/program-verify flowchart shown in figure 20.10 should be followed. Performing programming operations according to this flowchart will enable data or programs to be written to the flash memory without subjecting the chip to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to which programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer must be performed even if writing fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data area, a 128-byte reprogramming data area, and a 128-byte additional-programming data area. Perform reprogramming data computation and additional programming data computation according to figure 20.10.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data area or additional-programming data area to the flash memory. The program address and 128-byte data are latched in the flash memory. The lower 8 bits of the start address in the flash memory destination area must be H'00 or H'80.
5. The time during which the P1 bit is set to 1 is the programming time. Figure 20.10 shows the allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. Set a value greater than (tspsu + tsp200 + tcp + tcpsu) µs as the WDT overflow period.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 1 bit is B'0. Verify data can be read in words from the address to which a dummy write was performed.
8. The maximum number of repetitions of the program/program-verify sequence of the same bit is (N).

20.9 Program/Erase Protection

There are three kinds of flash memory program/erase protection; hardware protection, software protection, and error protection.

20.9.1 Hardware Protection

Hardware protection refers to a state in which programming/erasing of flash memory is forcibly disabled or aborted because of a transition to reset or standby mode. Flash memory control register 1 (FLMCR1), flash memory control register 2 (FLMCR2), erase block register 1 (EBR1), and erase block register 2 (EBR2) are initialized. In a reset via the $\overline{\text{RES}}$ pin, the reset state is not entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the AC Characteristics section.

20.9.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memory blocks by clearing the SWE1 bit in FLMCR1. When software protection is in effect, setting the P1 or E1 bit in FLMCR1 does not cause a transition to program mode or erase mode. By setting the erase block register 1 and 2 (EBR1 and EBR2), erase protection can be set for individual blocks. When EBR1 and EBR2 are set to H'00, erase protection is set for all blocks. By setting bit RAMS in RAMER, programming/erase protection is set for all blocks.

20.9.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory programming/erasing, or operation is not performed in accordance with the program/erase algorithm, and the program/erase operation is aborted. Aborting the program/erase operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the FLER bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/erasing (including vector read and instruction fetch)
- Immediately after exception handling (excluding a reset) during programming/erasing
- When a SLEEP instruction is executed during programming/erasing
- When the CPU loses the bus during programming/erasing

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TCSR_3*1	CMFB	CMFA	OVF	—	OS3	OS2	OS1	OS0	TMR_3
TCORA_2*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_2
TCORA_3*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_3
TCORB_2*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_2
TCORB_3*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_3
TCNT_2*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_2
TCNT_3*1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	TMR_3
SMR_2	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI_2
SMR_2	GM	BLK	PE	O/$\overline{E}$	BCP1	BCP0	CKS1	CKS0	
BRR_2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SCR_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SSR_2	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT	
SSR_2	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT	
RDR_2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
SCMR_2	—	—	—	—	SDIR	SINV	—	SMIF	
SBYCR	SSBY	STS2	STS1	STS0	—	—	—	—	SYSTEM
SYSCR	—	—	INTM1	INTM0	NMIEG	—	—	—	
SCKCR	—	—	—	—	—	SCK2	SCK1	SCK0	
MDCR	—	—	—	—	—	MDS2	MDS1	—	
MSTPCRA	MSTPA7	MSTPA6	MSTPA5	MSTPA4	MSTPA3	MSTPA2	MSTPA1	MSTPA0	
MSTPCRB	MSTPB7	MSTPB6	MSTPB5	MSTPB4	MSTPB3	MSTPB2	MSTPB1	MSTPB0	
MSTPCRC	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0	
LPWRCR	DTON	LSON	NESEL	SUBSTP	RFCUT	—	STC1	STC0	
SEMR0	—	—	—	—	ABCS	ACS2	ACS1	ACS0	SCI_0
BARA*1	—	—	—	—	—	—	—	—	PBC
	BAA23	BAA22	BAA21	BAA20	BAA19	BAA18	BAA17	BAA16	
	BAA15	BAA14	BAA13	BAA12	BAA11	BAA10	BAA9	BAA8	
	BAA7	BAA6	BAA5	BAA4	BAA3	BAA2	BAA1	BAA0	

Table 25.15 DC Characteristics (4)

Condition D (Masked-ROM version): V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	30	pF	
	P34 and P35		—	—	20	pF	
	All input pins except $\overline{RES}$, NMI, P34, and P35		—	—	15	pF	
Current consumption*2	Normal operation	I_{CC}*4	—	18 V_{CC} = 5.0 V	25 V_{CC} = 5.5 V	mA	f = 20.5 MHz
	Sleep mode		—	12 V_{CC} = 5.0 V	17 V_{CC} = 5.5 V	mA	f = 20.5 MHz
	All modules stopped		—	11	—	mA	f = 20.5 MHz, V_{CC} = 5.0 V (reference values)
	Medium-speed mode (ϕ/32)		—	10	—	mA	f = 20.5 MHz, V_{CC} = 5.0 V (reference values)
	Subactive mode		—	20	40	μA	Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD lighting)
	Subsleep mode		—	8	25	μA	Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD lighting)
	Watch mode		—	3	10	μA	$T_a \leq$ 50°C, Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD not used, WDT_1 operates)

Port Name	Reset	Hardware Standby Mode	Software Standby Mode	Watch Mode	Program Execution State Sleep Mode Subsleep Mode
Port K	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG16 to SEG9	SEG16 to SEG9
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
Port L	T	T	[Segment output]	[Segment output]	[Segment output]
			Port	SEG24 to SEG17	SEG24 to SEG17
			[Otherwise]	[Otherwise]	[Otherwise]
			Keep	Keep	I/O port
SEG40 to SEG25	T	T	T	[Segment output]	[Segment output]
				SEG40 to SEG25	SEG40 to SEG25
				[Otherwise]	[Otherwise]
				T	T

Legend:

H: High level

T: High-impedance

Keep: Input port becomes high-impedance, output port retains state

Port: Determined by port setting (input is high-impedance)