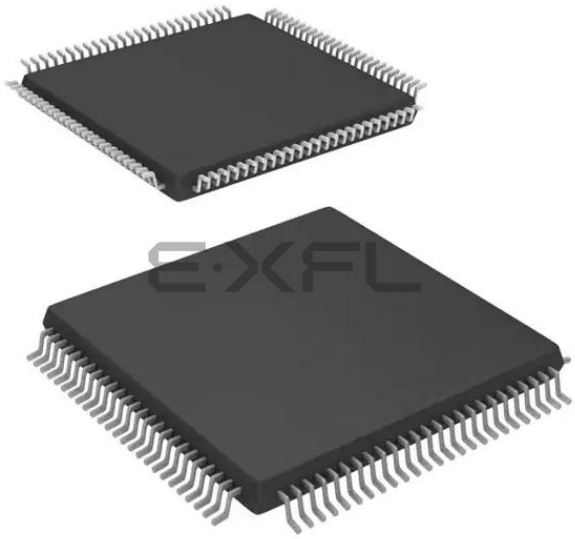

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, SCI, SmartCard
Peripherals	LCD, POR, PWM, WDT
Number of I/O	67
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2268tf20v

Item	Page	Revision (See Manual for Details)
25.2.2 DC Characteristics Table 25.2 DC Characteristics (2)	602	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	$\overline{RES}$, $\overline{STBY}$,NMI, FWE, MD2, MD1	V_{IH}	V_{CC} × 0.9		V_{CC} + 0.3	V	
	EXTAL, Ports 1, 3, 7, F, J to N, PH0 to PH3		V_{CC} × 0.8		V_{CC} + 0.3	V	
	Ports 4*4, 9, PH7		V_{CC} × 0.8		V_{CC} + 0.3*4	V	

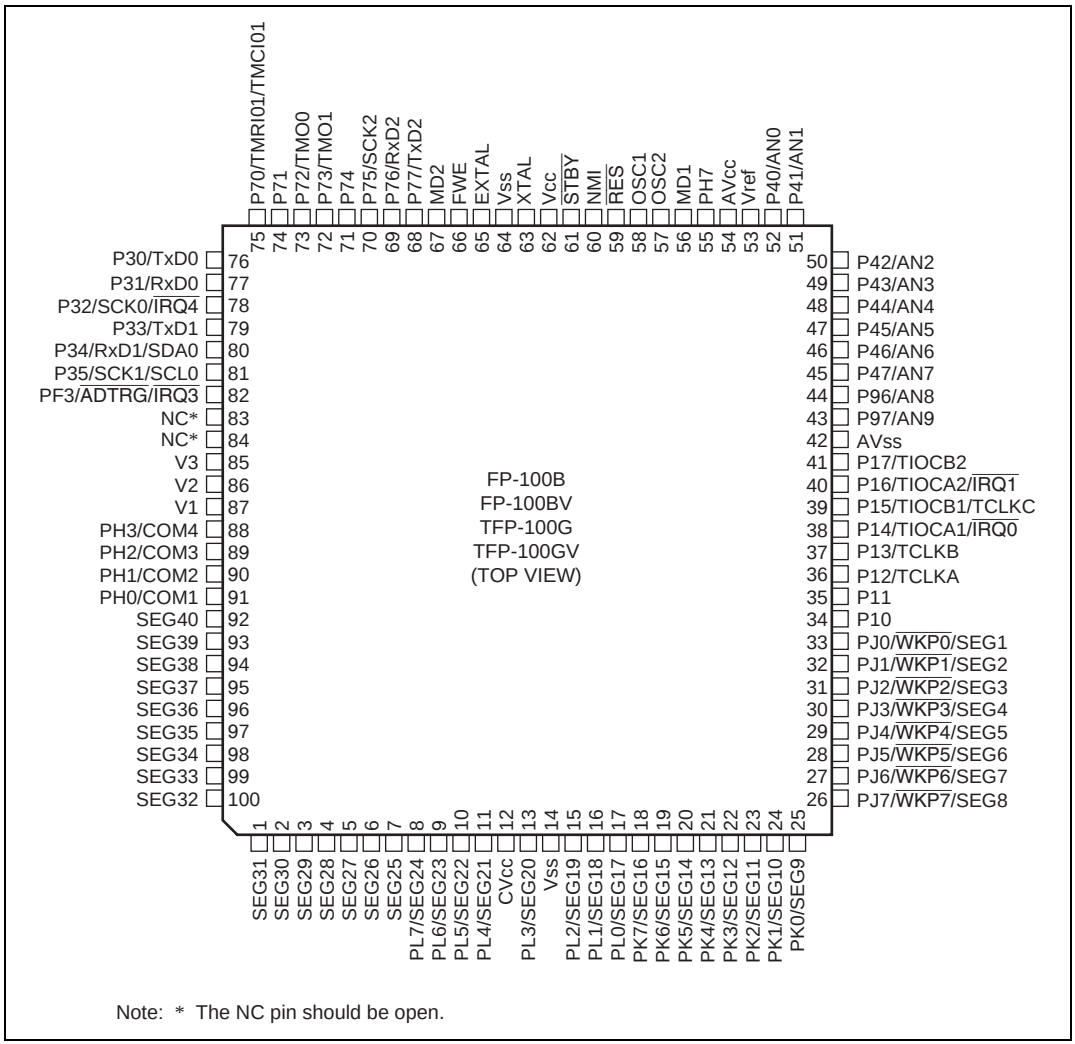
	603	Note added Notes: 4. When Vcc < AVcc, the maximum value for P40 and P41 is Vcc + 0.3 V.
25.2.4 A/D Conversion Characteristics Table 25.9 A/D Conversion Characteristics	615	Table condition amended Condition A (F-ZTAT version): V_{CC} = 3.0 V to 5.5 V*, AV_{CC} = 2.7 V to 5.5 V*, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 2 to 13.5 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications) Condition C (F-ZTAT version): V_{CC} = 4.0 V to 5.5 V*, AV_{CC} = 4.0 V to 5.5 V*, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 10 to 20.5 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications) Note added Note: * AN0 and AN1 can be used only when Vcc = AVcc.
25.3.2 DC Characteristics Table 25.15 DC Characteristics (1)	622	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, FWE, MD2, MD1	V_{IH}	V_{CC} 0.9		V_{CC} + 0.3	V	
	EXTAL, Ports 1, 3, 7, F, H, J to L		V_{CC} 0.8		V_{CC} + 0.3	V	
	Ports 4*4, 9		V_{CC} 0.8		AV_{CC} + 0.3*4	V	

	623	Note added Notes: 4. When Vcc < AVcc, the maximum value for P40 and P41 is Vcc + 0.3 V.
25.3.2 DC Characteristics Table 25.15 DC Characteristics (2)	624	Table amended

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	$\overline{RES}$, $\overline{STBY}$, NMI, FWE, MD2, MD1	V_{IH}	V_{CC} 0.9		V_{CC} + 0.3	V	
	EXTAL, Ports 1, 3, 7, F, H, J to L		V_{CC} 0.8		V_{CC} + 0.3	V	
	Ports 4*4, 9		V_{CC} 0.8		AV_{CC} + 0.3*4	V	

	625	Note added Notes: 4. When Vcc < AVcc, the maximum value for P40 and P41 is Vcc + 0.3 V.



Note: * The NC pin should be open.

Figure 1.4 Pin Arrangement of H8S/2264 Group

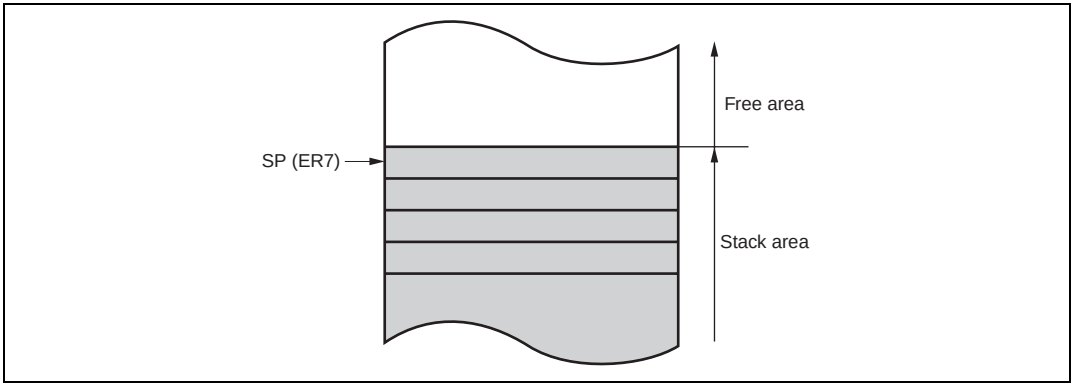


Figure 2.8 Stack Status

2.4.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. The length of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (When an instruction is fetched, the least significant PC bit is regarded as 0.)

2.4.3 Extended Control Register (EXR) (H8S/2268 Group Only)

EXR is an 8-bit register that manipulates the LDC, STC, ANDC, ORC, and XORC instructions. When these instructions except for the STC instruction is executed, all interrupts including NMI will be masked for three states after execution is completed.

Bit	Bit Name	Initial Value	R/W	Description
7	T	0	R/W	Trace Bit When this bit is set to 1, a trace exception is generated each time an instruction is executed. When this bit is cleared to 0, instructions are executed in sequence.
6 to 3	—	1	—	Reserved These bits are always read as 1.
2	I2	1	R/W	These bits designate the interrupt mask level (0 to 7). For details, refer to section 5, Interrupt Controller.
1	I1	1	R/W	
0	I0	1	R/W	

2.5 Data Formats

The H8S/2000 CPU can process 1-bit, 4-bit (BCD), 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

2.5.1 General Register Data Formats

Figure 2.9 shows the data formats in general registers.

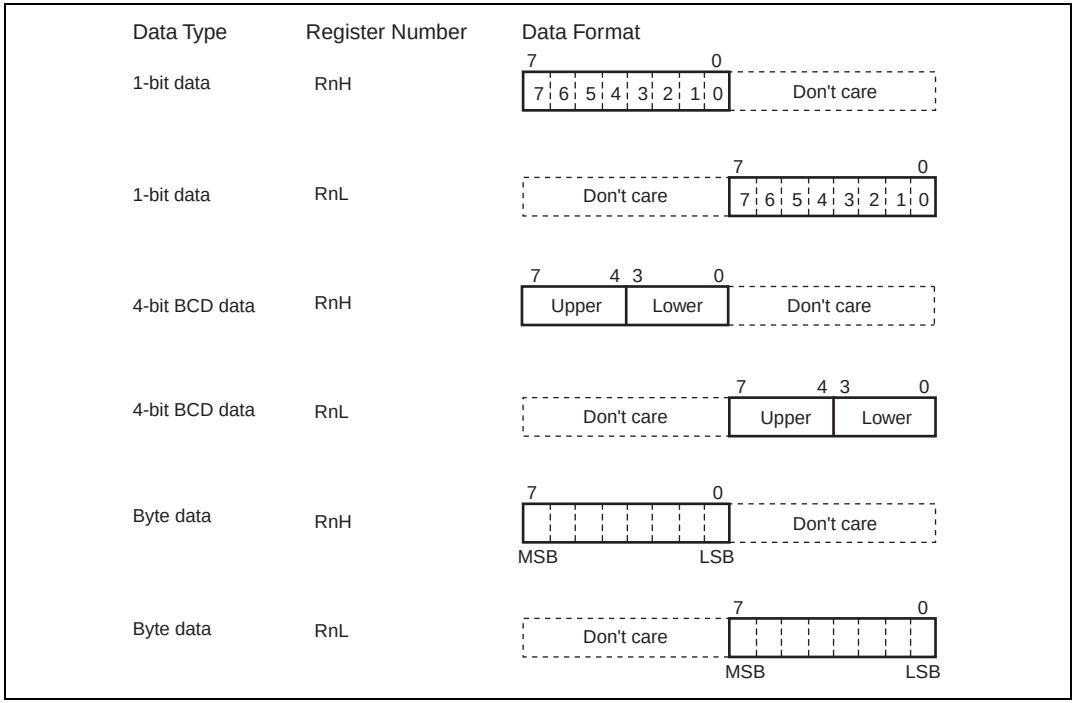


Figure 2.9 General Register Data Formats (1)

Exception Source	Vector Number	Vector Address Advanced Mode*1
Internal interrupt*2	24	H'0060 to H'0063
	⎮	⎮
	107	H'01AC to H'01AF
External interrupt WKP0 to WKP7	108	H'01B0 to H'01B3
Internal interrupt	120	H'01E0 to H'01E3
	⎮	⎮
	123	H'01EC to H'01EF

Notes: 1. Lower 16 bits of the address.
2. For details of internal interrupt vectors, see section 5.4.3, Interrupt Exception Handling Vector Table.
3. For details on direct transitions, see section 22.10, Direct Transitions.
4. Supported only by the H8S/2268 Group.

4.3 Reset

A reset has the highest exception priority.

When the $\overline{\text{RES}}$ pin goes low, all processing halts and this LSI enters the reset. A reset initializes the internal state of the CPU and the registers of on-chip peripheral modules. The interrupt control mode is 0 immediately after reset.

When the $\overline{\text{RES}}$ pin goes high from the low state, this LSI starts reset exception handling.

The chip can also be reset by overflow of the watchdog timer. For details see section 12, Watchdog Timer (WDT).

4.3.1 Reset Exception Handling

When the $\overline{\text{RES}}$ pin goes low, this LSI enters the reset. To ensure that this LSI is reset, hold the $\overline{\text{RES}}$ pin low for at least 20 ms at power-up. To reset the chip during operation, hold the $\overline{\text{RES}}$ pin low for at least 20 states. When the $\overline{\text{RES}}$ pin goes high after being held low for the necessary time, this LSI starts reset exception handling as follows.

1. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized, the T bit in EXR* is cleared to 0, and the I bits in EXR* and CCR is set to 1.
2. The reset exception handling vector address is read and transferred to the PC, and program execution starts from the address indicated by the PC.

Note: * Supported only by the H8S/2268 Group.

the corresponding DDR to 0; and use the pin as an I/O pin for another function. IRQnF interrupt request flag is set to 1 when the setting condition is satisfied, regardless of IER settings. Accordingly, refer to only necessary flags.

5.4.2 Internal Interrupts

For each on-chip peripheral module, there are flags that indicate the interrupt request status, and enable bits that select enabling or disabling of these interrupts. If both of these are set to 1 for a particular interrupt source, an interrupt request is issued to the interrupt controller.

5.4.3 Interrupt Exception Handling Vector Table

Table 5.2 shows interrupt exception handling sources, vector addresses, and interrupt priorities. For default priorities, the lower the vector number, the higher the priority.

Priorities among modules can be set by means of the IPR. (H8S/2268 Group only)

Modules set at the same priority will conform to their default priorities. Priorities within a module are fixed.

Port	Description	Port and Other Functions Name	Input/Output and Output Type
Port L	General I/O port also functioning as LCD segment output pins	PL7/SEG24	
		PL6/SEG23	
		PL5/SEG22	
		PL4/SEG21	
		PL3/SEG20	
		PL2/SEG19	
		PL1/SEG18	
		PL0/SEG17	

9.1 Port 1

Port 1 is an 8-bit I/O port and has the following registers.

- Port 1 data direction register (P1DDR)
- Port 1 data register (P1DR)
- Port 1 register (PORT1)

9.1.1 Port 1 Data Direction Register (P1DDR)

P1DDR specifies input or output of the port 1 pins using the individual bits. P1DDR cannot be read; if it is, an undefined value will be read.

The value of this register when read is undefined after a bit manipulation instruction is executed. To prevent undefined read values, do not use bit manipulation instructions to write to this register. For details, see section 2.9.4, Access Methods for Registers with Write-Only Bits.

Table 9.3 Examples of Ways to Handle Unused Input Pins

Port Name	Pin Handling Example
Port 1	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port 3	
Port 4	Connect each pin to AVcc (pull-up) or to AVss (pull-down) via a resistor.
Port 7	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port 9	Connect each pin to AVcc (pull-up) or to AVss (pull-down) via a resistor.
Port F	Connect each pin to Vcc (pull-up) or to Vss (pull-down) via a resistor.
Port H	* Ports M and N apply to the H8S/2268 Group only.
Port J	
Port K	
Port L	
Port M*	
Port N*	

For pins set as LCD SEG pins (see 17.3.1, LED Port Control Register (LPCR)), add extra capacitance as appropriate to accommodate the LCD drive power supply capacity and the LCD used.

10.10.12 Contention between TCNT Write and Overflow/Underflow

In the H8S/2268 Group, if there is an up-count or down-count in the T2 state of a TCNT write cycle and overflow/underflow occurs, the TCNT write takes precedence and the TCFV/TCFU flag in TSR is not set.

In the H8S/2264 Group, if there is an up-count in the T2 state of a TCNT write cycle and overflow occurs, the TCNT write takes precedence and the TCFV flag in TSR is not set.

Figure 10.54 shows the operation timing when there is contention between TCNT write and overflow.

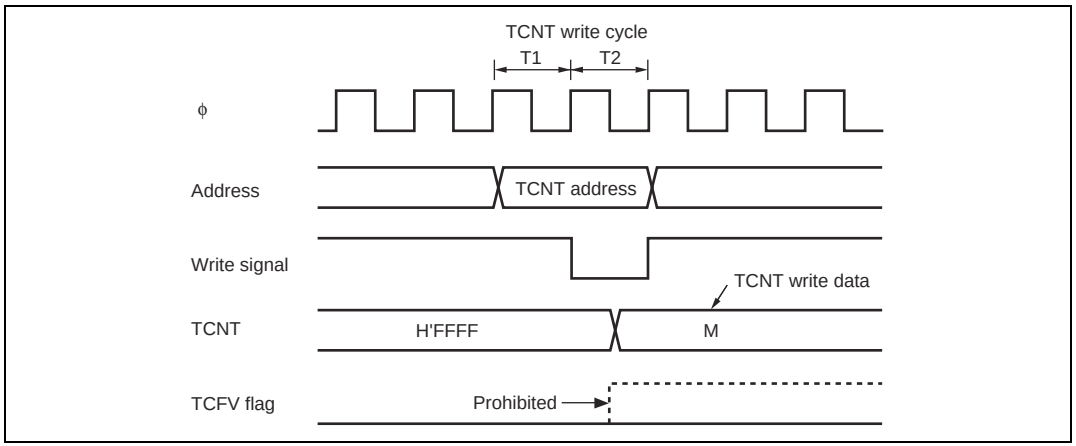


Figure 10.54 Contention between TCNT Write and Overflow

10.10.13 Multiplexing of I/O Pins

In the H8S/2268 Group, the TCLKA input pin is multiplexed with the TIOCC0 I/O pin, the TCLKB input pin with the TIOCD0 I/O pin, the TCLKC input pin with the TIOCB1 I/O pin, and the TCLKD input pin with the TIOCB2 I/O pin. In the H8S/2264 Group, the TCLKC input pin is multiplexed with the TIOCB1 I/O pin. When an external clock is input, compare match output should not be performed from a multiplexed pin.

10.10.14 Interrupts in Module Stop Mode

If module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source, or the DTC activation source (the H8S/2268 Group only). Interrupts should therefore be disabled before entering module stop mode.

TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding compare-match flag B (CMFB) in TCSR is set. Note, however, that comparison is disabled during the T2 state of a TCORB write cycle.

The timer output from the TMO pin can be freely controlled by the compare-match signal B and the settings of output select bits OS1 and OS0 in TCSR.

The initial value of TCORB is H'FF.

11.3.4 Timer Control Register (TCR)

TCR selects the TCNT clock source and the time at which TCNT is cleared, and controls interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	CMIEB	0	R/W	Compare-Match Interrupt Enable B Selects whether the CMFB interrupt request (CMIB) is enabled or disabled when the CMFB flag in TCSR is set to 1. 0: CMFB interrupt request (CMIB) is disabled 1: CMFB interrupt request (CMIB) is enabled
6	CMIEA	0	R/W	Compare-Match Interrupt Enable A Selects whether the CMFA interrupt request (CMIA) is enabled or disabled when the CMFA flag in TCSR is set to 1. 0: CMFA interrupt request (CMIA) is disabled 1: CMFA interrupt request (CMIA) is enabled
5	OVIE	0	R/W	Timer Overflow Interrupt Enable Selects whether the OVF interrupt request (OVI) is enabled or disabled when the OVF flag in TCSR is set to 1. 0: OVF interrupt request (OVI) is disabled 1: OVF interrupt request (OVI) is enabled
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	0	R/W	These bits select the method by which TCNT is cleared 00: Clearing is disabled 01: Cleared on compare-match A 10: Cleared on compare-match B 11: Cleared on rising edge of external reset input

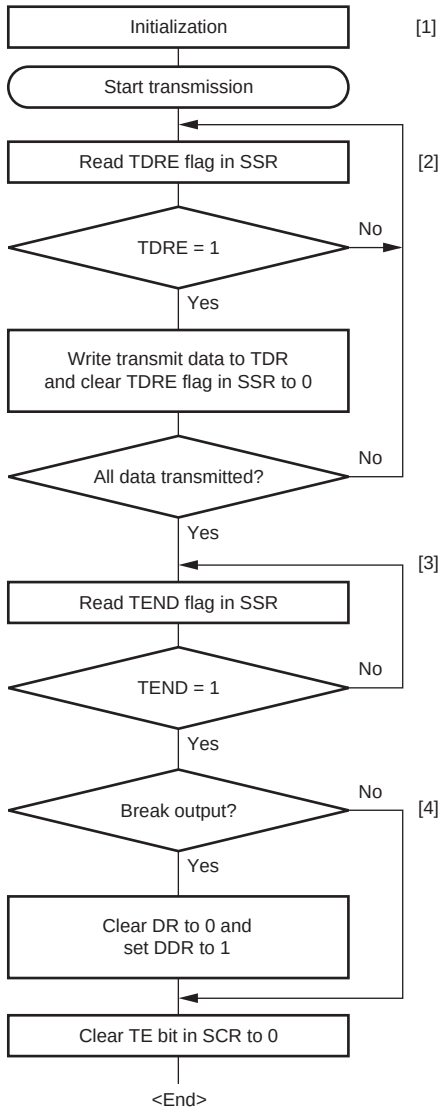
Table 13.3 BRR Settings for Various Bit Rates (Asynchronous Mode) (4)

Bit Rate (bps)	Operating Frequency ϕ (MHz)								
	18			19.6608			20		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	79	–0.12	3	86	0.31	3	88	–0.25
150	2	233	0.16	2	255	0.00	2	64	0.16
300	2	116	0.16	2	127	0.00	2	129	0.16
600	1	233	0.16	1	255	0.00	1	64	0.16
1200	1	116	0.16	1	127	0.00	1	129	0.16
2400	0	233	0.16	0	255	0.00	0	64	0.16
4800	0	116	0.16	0	127	0.00	0	129	0.16
9600	0	58	–0.69	0	63	0.00	0	64	0.16
19200	0	28	1.02	0	31	0.00	0	32	–1.36
31250	0	17	0.00	0	19	–1.70	0	19	0.00
38400	0	14	–2.34	0	15	0.00	0	15	1.73

Table 13.4 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (kbps)	n	N	ϕ (MHz)	Maximum Bit Rate (kbps)	n	N
2	62.5	0	0	9.8304	307.2	0	0
2.097152	65.536	0	0	10	312.5	0	0
2.4576	76.8	0	0	12	375.0	0	0
3	93.75	0	0	12.288	384.0	0	0
3.6864	115.2	0	0	14	437.5	0	0
4	125.0	0	0	14.7456	460.8	0	0
4.9152	153.6	0	0	16	500.0	0	0
5	156.25	0	0	17.2032	537.6	0	0
6	187.5	0	0	18	562.5	0	0
6.144	192.0	0	0	19.6608	614.4	0	0
7.3728	230.4	0	0	20	625.0	0	0
8	250.0	0	0				

Figure 13.10 shows a sample flowchart for data transmission.



[1] SCI initialization:
The TxD pin is automatically designated as the transmit data output pin.
After the TE bit is set to 1, a frame of 1s is output, and transmission is enabled.

[2] SCI status check and transmit data write:
Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR and clear the TDRE flag to 0.

[3] Serial transmission continuation procedure:
To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR, and then clear the TDRE flag to 0. Checking and clearing of the TDRE flag is automatic when the DTC* is activated by a transmit data empty interrupt (TXI) request, and data is written to TDR. (H8S/2268 Group only)

[4] Break output at the end of serial transmission:
To output a break in serial transmission, set DR for the port corresponding to the TxD pin to 0, clear DDR to 1, then clear the TE bit in SCR to 0.

Note: * The case, in which the DTC automatically checks and clears the TDRE flag, occurs only when DISEL in DTC is 0 with the transfer counter not being 0.
Therefore, the TDRE flag should be cleared by CPU when DISEL is 1, or when DISEL is 0 with the transfer counter being 0.

Figure 13.10 Sample Serial Transmission Flowchart

14.4.7 IRIC Setting Timing and SCL Control

The interrupt request flag (IRIC) is set at different times depending on the WAIT bit in ICMR, the FS bit in SAR, and the FSX bit in SARX. If the TDRE or RDRF internal flag is set to 1, SCL is automatically held low after one frame has been transferred; this timing is synchronized with the internal clock. Figure 14.19 shows the IRIC set timing and SCL control.

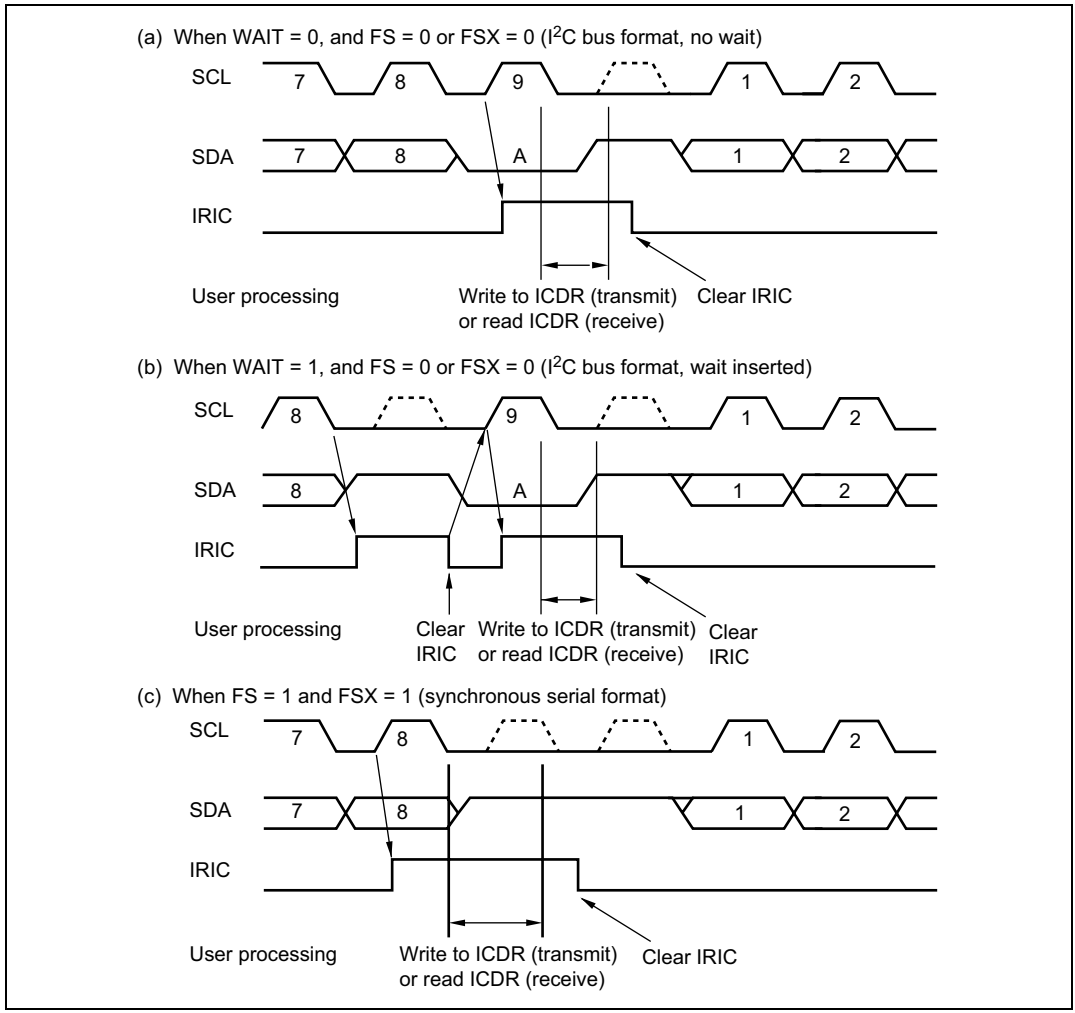


Figure 14.19 IRIC Setting Timing and SCL Control

Bit	Bit Name	Initial Value	R/W	Description
4	SUPS	0	R/W	(H8S/2268 Group) Drive Power Select Triple Step-up Voltage Circuit Control The triple step-up voltage circuit stops operation when Vcc is selected as drive power. The triple step-up voltage circuit starts operation when LCD input reference voltage (V_{LCD3}) is selected as drive power. 0: Drive power is Vcc, triple step-up voltage circuit halts 1: Drive power is triple step-up voltage of the LCD input reference voltage (V_{LCD3}), triple step-up voltage circuit operates (H8S/2264 Group) Reserved 0 should be written to this bit.
3	CDS3	0	R/W	Selection of Duty Ratio for Charge/Discharge Pulse
2	CDS2	0	R/W	Duty ratio is selected during the power supply divider resistance is connected to power supply circuit. When the duty ratio of 0 is selected, the power supply divider resistance is fixed to the state that the resistance is separated from the power supply circuit. Therefore, supply the power to pins V_1, V_2, and V_3 from the external circuit. The charge/discharge pulses have the waveform shown in figure 17.2. The duty ratio is represented by T_C/T_W. 0000: duty ratio = 1 (stack at high) 0001: duty ratio = 1/8 0010: duty ratio = 2/8 0011: duty ratio = 3/8 0100: duty ratio = 4/8 0101: duty ratio = 5/8 0110: duty ratio = 6/8 0111: duty ratio = 0 (stack at low) 10XX: duty ratio = 1/16 11XX: duty ratio = 1/32
1	CDS1	0	R/W	
0	CDS0	0	R/W	

Legend:
X: Don’t care

The differences between boot mode and user program mode are shown in table 20.1.

Figure 20.3 shows the operation flow for boot mode and figure 20.4 shows that for user program mode.

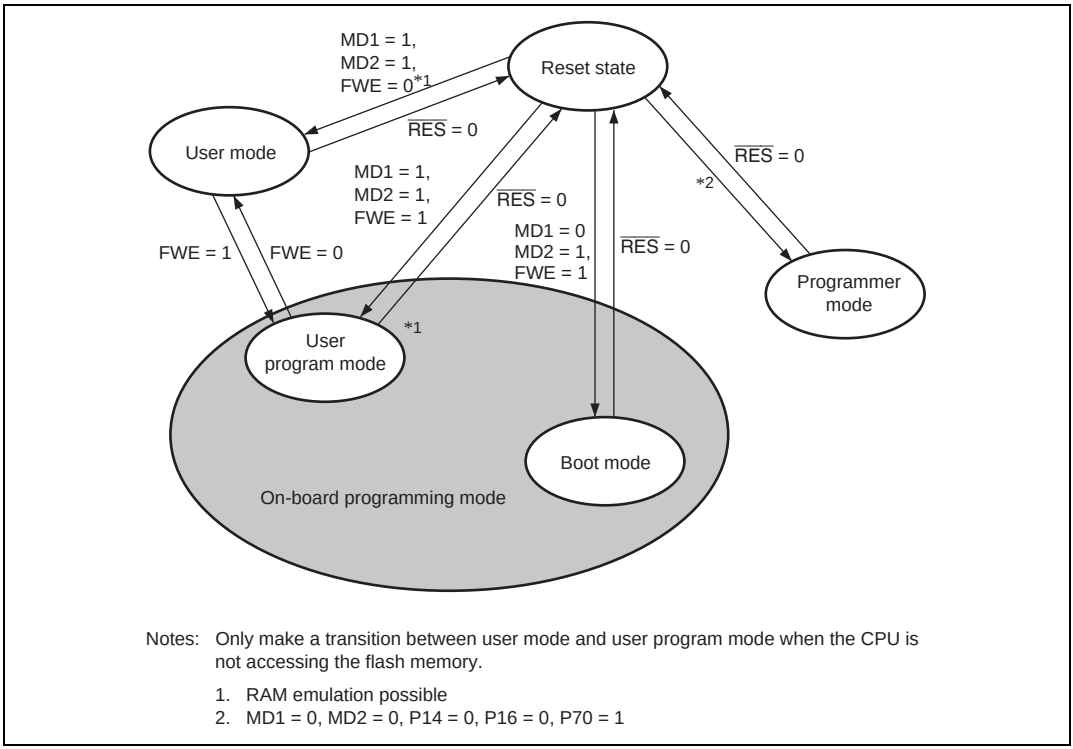


Figure 20.2 Flash Memory State Transitions

Table 20.1 Differences between Boot Mode and User Program Mode

	Boot Mode	User Program Mode
Total erase	Yes	Yes
Block erase	No	Yes
Programming control program*	Program/program-verify	Program/program-verify/erase/ erase-verify/emulation

Note: * To be provided by the user, in accordance with the recommended algorithm.

Section 24 List of Registers

This section gives information on the on-chip I/O registers and is configured as described below.

1. Register Addresses (by functional module, in address order)
   - Descriptions by functional module, in ascending order of addresses
   - When registers consist of 16 bits, the addresses of the MSBs are given.
   - Data bus width is given.
   - The number of access states are given.
2. Register Bits
   - Bit configurations of the registers are described in the same order as the Register Addresses (by functional module, in ascending order of addresses).
   - Reserved bits are indicated by — in the bit name.
   - When registers consist of 16 or 32 bits, bits are described from the MSB side.
3. Register States in Each Operating Mode
   - Register states are described in the same order as the Register Addresses (by functional module, in ascending order of addresses).
   - The register states described are for the basic operating modes. If there is a specific reset for an on-chip module, refer to the section on that on-chip module.

Table 25.2 DC Characteristics (4)

Condition C (F-ZTAT version): V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)*1

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	$\overline{RES}$	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz, Ta = 25°C
	NMI		—	—	30	pF	
	P32 to P35		—	—	20	pF	
	All input pins except $\overline{RES}$, NMI, P32 to P35		—	—	15	pF	
Current consumption*2	Normal operation	I_{CC}*4	—	30 V_{CC} = 5.0 V	40 V_{CC} = 5.5 V	mA	f = 20.5 MHz
	Sleep mode		—	22 V_{CC} = 5.0 V	30 V_{CC} = 5.5 V	mA	f = 20.5 MHz
	All modules stopped		—	15	—	mA	f = 20.5 MHz, V_{CC} = 5.0 V (reference values)
	Medium-speed mode (ϕ/32)		—	19	—	mA	f = 20.5 MHz, V_{CC} = 5.0 V (reference values)
	Subactive mode		—	70	120	μA	Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD lighting)
	Subsleep mode		—	60	100	μA	Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD lighting)
	Watch mode		—	5	30	μA	Using 32.768 kHz crystal resonator, Vcc = 5.0 V (LCD and TMR4 not used, WDT_1 operates)
	Standby mode*3		—	1.0 Vcc = 5.0 V	10 Vcc = 5.5 V	μA	$T_a \leq$ 50°C, 32.768 kHz not used
			—	—	50 Vcc = 5.5 V		50°C < T_a, 32.768 kHz not used

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current consumption*2	Watch mode	I_{CC}*4	—	2.5	8	μA	$T_a \leq 50°C$, Using 32.768 kHz crystal resonator, Vcc = 3.0 V (LCD not used, WDT_1 operates)
			—	—	10		50°C < Ta, using 32.768 kHz crystal resonator, Vcc = 3.0 V (LCD not used, WDT_1 operates)
	Standby mode*3		—	0.5 Vcc = 3.0 V	5 Vcc = 5.5 V	μA	$T_a \leq 50°C$, 32.768 kHz not used
			—	—	20 Vcc = 5.5 V		50°C < T_a, 32.768 kHz not used
Analog power supply current	During A/D conversion	AI_{CC}	—	0.3	1.5	mA	
	Waiting for A/D conversion		—	0.01	5.0	μA	
Reference current	During A/D conversion	AI_{CC}	—	0.4	1.0	mA	
	Waiting for A/D conversion		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. If the A/D converter is not used, do not leave the AVCC, Vref, and AVSS pins open. Apply a voltage 2.0 to 5.5 V to the AVCC and Vref pins by connecting them to V_{CC}, for instance. Set $V_{ref} \leq AV_{CC}$.

2. Current consumption values are for V_{IH} min. = V_{CC} – 0.2 V, V_{IL} max. = 0.2 V with all output pins unloaded and the on-chip pull-up resistors in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, V_{IH} min. = V_{CC} – 0.2, and V_{IL} max. = 0.2 V.

4. I_{CC} depends on V_{CC} and f as follows (reference):

   I_{CC} max. = 3.0 (mA) + 1.24 (mA/V) × (Vcc – 2.7 (V)) + 1.00 (mA/MHz) × (f – 2.0 (MHz)) (normal operation)

   I_{CC} max. = 2.0 (mA) + 1.12 (mA/V) × (Vcc – 2.7 (V)) + 0.64 (mA/MHz) × (f – 2.0 (MHz)) (sleep mode)