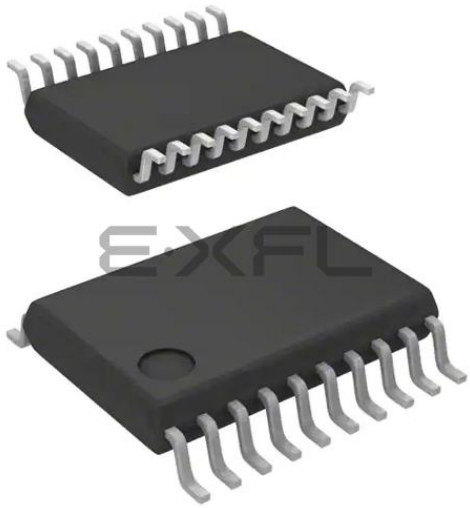

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10369asp-x0

Table 2.9 System Control Instructions

Instruction	Size*1	Function
TRAPA	—	Starts trap-instruction exception handling.
RTE	—	Returns from an exception-handling routine.
SLEEP	—	Causes a transition to a power-down state.
LDC	B/W	(EAs) → CCR, (EAs) → EXR*2 Moves the source operand contents or immediate data to CCR or EXR*2. Although CCR and EXR*2 are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
STC	B/W	CCR → (EAd), EXR*2 → (EAd) Transfers CCR or EXR*2 contents to a general register or memory. Although CCR and EXR*2 are 8-bit registers, word-size transfers are performed between them and memory. The upper 8 bits are valid.
ANDC	B	CCR ∧ #IMM → CCR, EXR ∧ #IMM → EXR*2 Logically ANDs the CCR or EXR*2 contents with immediate data.
ORC	B	CCR ∨ #IMM → CCR, EXR ∨ #IMM → EXR*2 Logically ORs the CCR or EXR*2 contents with immediate data.
XORC	B	CCR ⊕ #IMM → CCR, EXR ⊕ #IMM → EXR*2 Logically XORs the CCR or EXR*2 contents with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Notes: 1. Refers to the operand size.
B: Byte
W: Word
2. Supported only by the H8S/2268 Group.

5.5.2 Interrupt Control Mode 0

Enabling and disabling of IRQ interrupts, WKP interrupts and on-chip peripheral module interrupts can be set by means of the I bit in the CPU's CCR. Interrupts are enabled when the I bit is cleared to 0, and disabled when set to 1.

Figure 5.9 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. If the I bit is set to 1, only an NMI interrupt is accepted, and other interrupt requests are held pending. If the I bit is cleared, an interrupt request is accepted.
3. Interrupt requests are sent to the interrupt controller, the highest-ranked interrupt according to the priority system is accepted, and other interrupt requests are held pending.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. The PC and CCR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.
6. Next, the I bit in CCR is set to 1. This masks all interrupts except NMI.
7. The CPU generates a vector address for the accepted interrupt and starts execution of the interrupt handling routine at the address indicated by the contents of the vector address in the vector table.

6.2.2 Break Address Register B (BARB)

BARB is the channel B break address register. The bit configuration is the same as for BARA.

6.2.3 Break Control Register A (BCRA)

BCRA controls channel A PC breaks.

Bit	Bit Name	Initial Value	R/W	Description
7	CMFA	0	R/(W)*1	Condition Match Flag A [Setting condition] When a condition set for channel A is satisfied [Clearing condition] When 0 is written to CMFA after reading*2 CMFA = 1
6	CDA	0	R/W	CPU Cycle/DTC Cycle Select A Selects the channel A break condition bus master. 0: CPU 1: CPU or DTC
5	BAMRA2	0	R/W	Break Address Mask Register A2 to A0
4	BAMRA1	0	R/W	These bits specify which bits of the break address set in BARA are to be masked.
3	BAMRA0	0	R/W	000: BAA23 – 0 (All bits are unmasked) 001: BAA23 – 1 (Lowest bit is masked) 010: BAA23 – 2 (Lower 2 bits are masked) 011: BAA23 – 3 (Lower 3 bits are masked) 100: BAA23 – 4 (Lower 4 bits are masked) 101: BAA23 – 8 (Lower 8 bits are masked) 110: BAA23 – 12 (Lower 12 bits are masked) 111: BAA23 – 16 (Lower 16 bits are masked)
2	CSELA1	0	R/W	Break Condition Select
1	CSELA0	0	R/W	Selects break condition of channel A. 00: Instruction fetch is used as break condition 01: Data read cycle is used as break condition 10: Data write cycle is used as break condition 11: Data read/write cycle is used as break condition

- P14/TIOCA1/$\overline{\text{IRQ0}}$

  The pin function is switched as shown below according to the combination of the TPU channel 1 setting and the P14DDR bit.

TPU Channel 1 Setting	Output	Input or Initial Value	
P14DDR	—	0	1
Pin function	TIOCA1 output	P14 input	P14 output
		TIOCA1 input*1	
	$\overline{\text{IRQ0}}$ input*2		

Notes: 1. This pin functions as TIOCA1 input when TPU channel 1 timer operating mode is set to normal operation or phase counting mode*3 and IOA3 to IOA0 in TIOR_1 are set to 10xx.
2. When this pin is used as an external interrupt pin, do not specify other functions.
3. Supported only by the H8S/2268 Group.

- P13/TIOCD0*3/TCLKB

  The pin function is switched as shown below according to the combination of the TPU channel 0*3 setting, TPSC2 to TPSC0 bits in TCR0*3, TCR1 and TCR2, and the P13DDR bit.

TPU Channel 0 Setting*3	Output	Input or Initial Value	
P13DDR	—	0	1
Pin function	TIOCD0 output*3	P13 input	P13 output
		TIOCD0 input*1*3	
	TCLKB input*2		

Notes: 1. In the H8S/2268 Group, this pin functions as TIOCD0 input when TPU channel 0 timer operating mode is set to normal operation and IOD3 to IOD0 in TIORL_0 are set to 10xx.
2. This pin functions as TCLKB input when TPSC2 to TPSC0 are set to 101 in any of TCR0*3, TCR1 and TCR2. TCLKB input, or when channel 1 is set to phase counting mode*3.
3. Supported only by the H8S/2268 Group.

9.3 Port 4

Port 4 is an 8-bit input-only port and has the following register.

- Port 4 register (PORT4)

9.3.1 Port 4 Register (PORT4)

PORT4 shows port 4 pin states. This register cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P47	—*	R	The pin states are always read when a port 4 read is performed.
6	P46	—*	R	
5	P45	—*	R	
4	P44	—*	R	
3	P43	—*	R	
2	P42	—*	R	
1	P41	—*	R	
0	P40	—*	R	

Note: * Determined by the states of pins P47 to P40.

9.3.2 Pin Functions

Port 4 pins also function as A/D converter analog input pins (AN0 to AN7).

9.4 Port 7

Port 7 is an 8-bit I/O port and has the following registers.

- Port 7 data direction register (P7DDR)
- Port 7 data register (P7DR)
- Port 7 register (PORT7)

9.7.2 Port H Data Register (PHDR)

PHDR stores output data for port H.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	Undefined	—	Reserved These bits are always read as undefined value and cannot be modified.
3	PH3DR	0	R/W	Output data for a pin is stored when the pin is specified as a general purpose output port.
2	PH2DR	0	R/W	
1	PH1DR	0	R/W	
0	PH0DR	0	R/W	

9.7.3 Port H Register (PORTH)

PORTH shows the pin states and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PH7	—*	R	When this bit is read, PH7 pin status is always read.
6 to 4	—	Undefined	—	Reserved These bits are always read as undefined value and cannot be modified.
3	PH3	—*	R	If these bits are read while the corresponding PHDDR bits are set to 1, the PHDR value is read. If these bits are read while PHDDR bits are cleared to 0, the pin states are read.
2	PH2	—*	R	
1	PH1	—*	R	
0	PH0	—*	R	

Note: * Determined by the states of pins PH7 and PH3 to PH0.

9.7.4 Pin Functions

Port H pins also function as a DTMF generation circuit analog output pin (TONED)*, 8-bit reload timer input pin (TMCI4)*, and LCD driver common output pins (COM4 to COM1). Port H pin functions are shown below.

Note: * Supported only by the H8S/2268 Group.

2. Free-running count operation and periodic count operation

   Immediately after a reset, the TPU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, the TPU requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

   Figure 10.8 illustrates free-running counter operation.

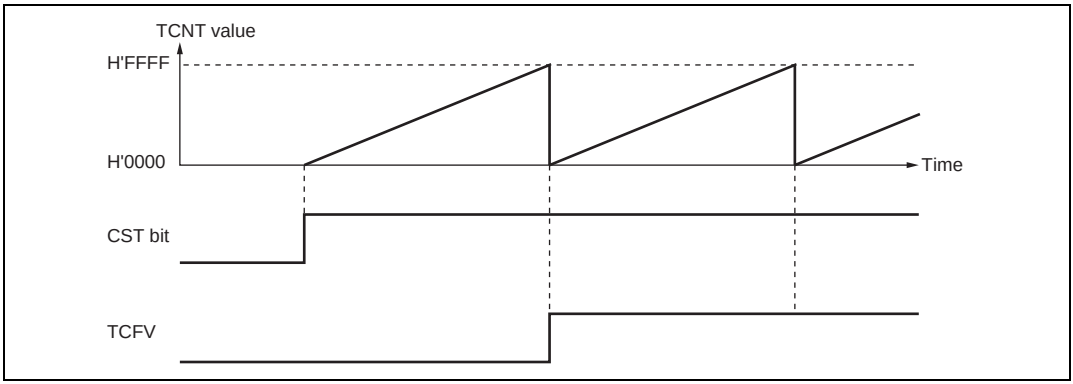


Figure 10.8 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR0 to CCLR2 in the H8S/2268 Group TCR or bits CCLR0 and CCLR1 in the H8S/2264 Group TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the TPU requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

Figure 10.9 illustrates periodic counter operation.

10.9 Operation Timing

10.9.1 Input/Output Timing

TCNT Count Timing: Figure 10.31 shows TCNT count timing in internal clock operation, and figure 10.32 shows TCNT count timing in external clock operation.

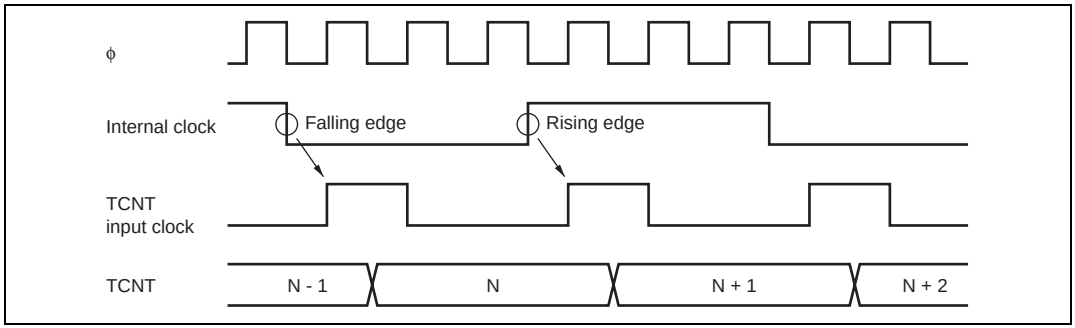


Figure 10.31 Count Timing in Internal Clock Operation

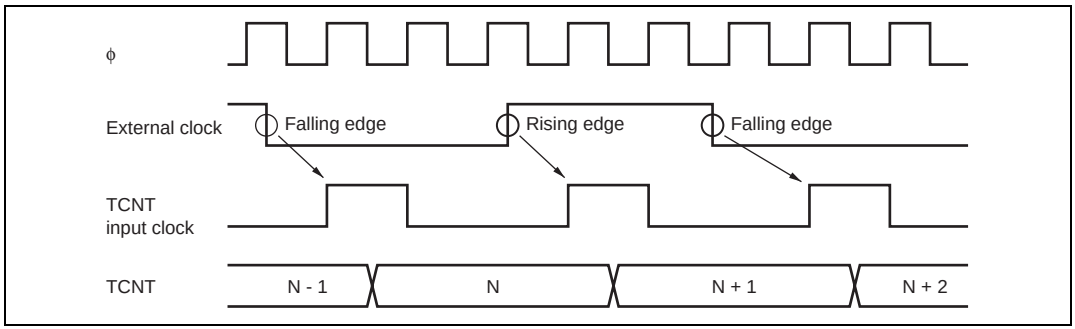
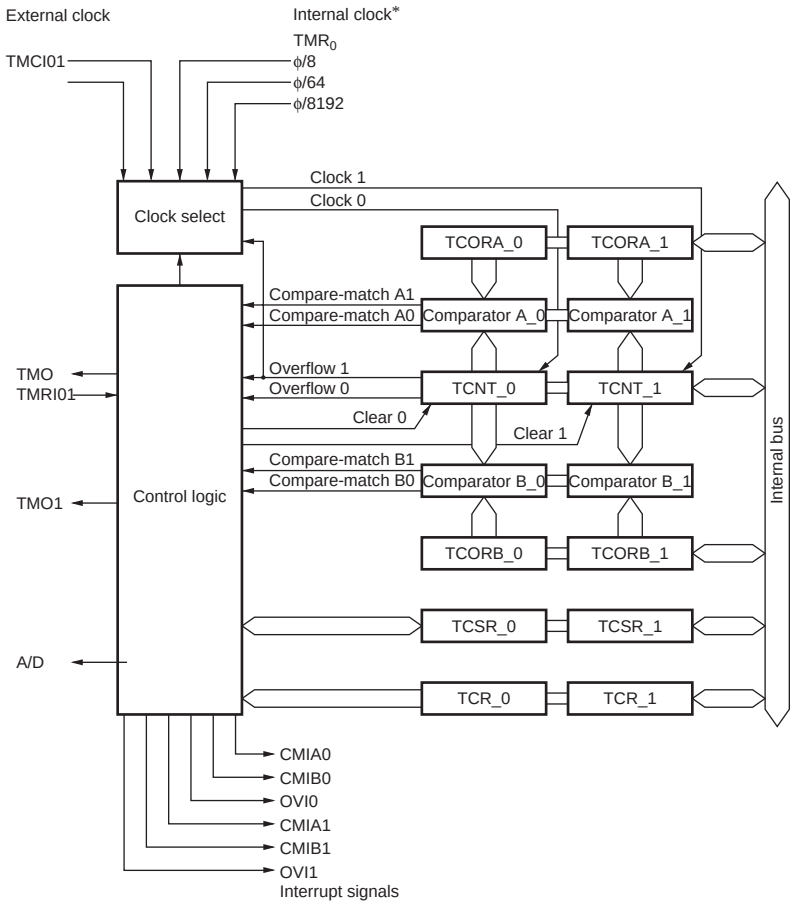


Figure 10.32 Count Timing in External Clock Operation

Output Compare Output Timing: A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TIOR is output at the output compare output pin. After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 10.33 shows output compare output timing.

Figure 11.1 shows a block diagram of the 8-bit timer module (TMR_0 and TMR_1).



Legend:
TCORA_0: Time constant register A_0
TCORB_0: Time constant register B_0
TCNT_0: Timer counter_0
TCSR_0: Timer control/status register_0
TCR_0: Timer control register_0
TCORA_1: Time constant register A_1
TCORB_1: Time constant register B_1
TCNT_1: Timer counter_1
TCSR_1: Timer control/status register_1
TCR_1: Timer control register_1

Note: * When a sub-clock is operating, ϕ will be ϕ_{SUB}.

Figure 11.1 Block Diagram of 8-Bit Timer Module

13.6.5 Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)

Figure 13.23 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (ORER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.

13.9.7 Switching from SCK Pin Function to Port Pin Function:

- Problem in Operation: When switching the SCK pin function to the output port function (high-level output) by making the following settings while DDR = 1, DR = 1, C/$\overline{A}$ = 1, CKE1 = 0, CKE0 = 0, and TE = 1 (synchronous mode), low-level output occurs for one half-cycle.
  1. End of serial data transmission
  2. TE bit = 0
  3. C/$\overline{A}$ bit = 0 ... switchover to port output
  4. Occurrence of low-level output (see figure 13.41)

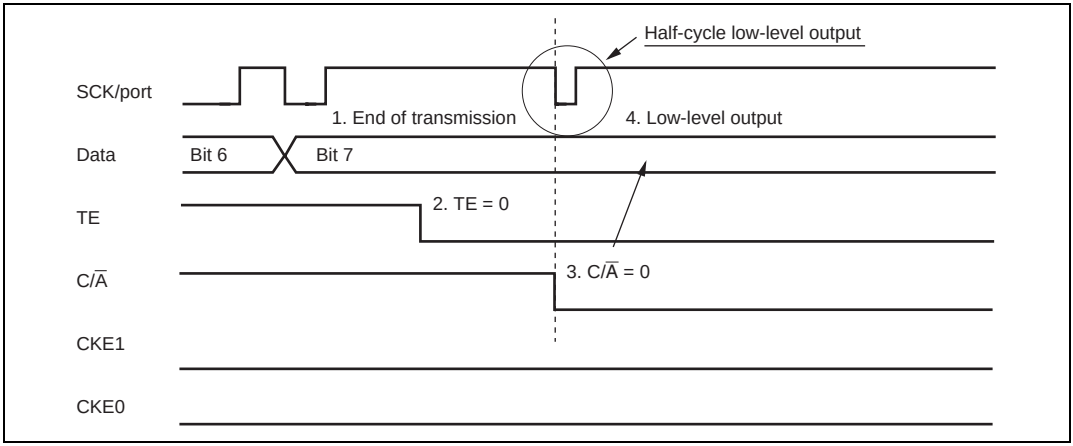


Figure 13.41 Operation when Switching from SCK Pin Function to Port Pin Function

Bit	Bit Name	Initial Value	R/W	Description
4	AASX	0	R/(W)*	Second Slave Address Recognition Flag [Setting condition] When the second slave address is detected in slave receive mode and FSX = 0 [Clearing conditions] • When 0 is written in AASX after reading AASX = 1 • When a start condition is detected • In master mode
3	AL	0	R/(W)*	Arbitration Lost Flag Indicates that bus arbitration was lost in master mode. [Setting condition] • When the internal SDA and SDA pin do not match at the rise of SCL. • When the internal SCL is high at the fall of SCL. [Clearing conditions] • When 0 is written in AL after reading AL = 1 • When ICDR data is written (transmit mode) or read (receive mode)
2	AAS	0	R/(W)*	Slave Address Recognition Flag [Setting condition] When the slave address or general call address (one frame including a R/$\overline{W}$ bit is H'00) is detected in slave receive mode and FS = 0. [Clearing conditions] • When ICDR data is written (transmit mode) or read (receive mode) • When 0 is written in AAS after reading AAS = 1 • In master mode

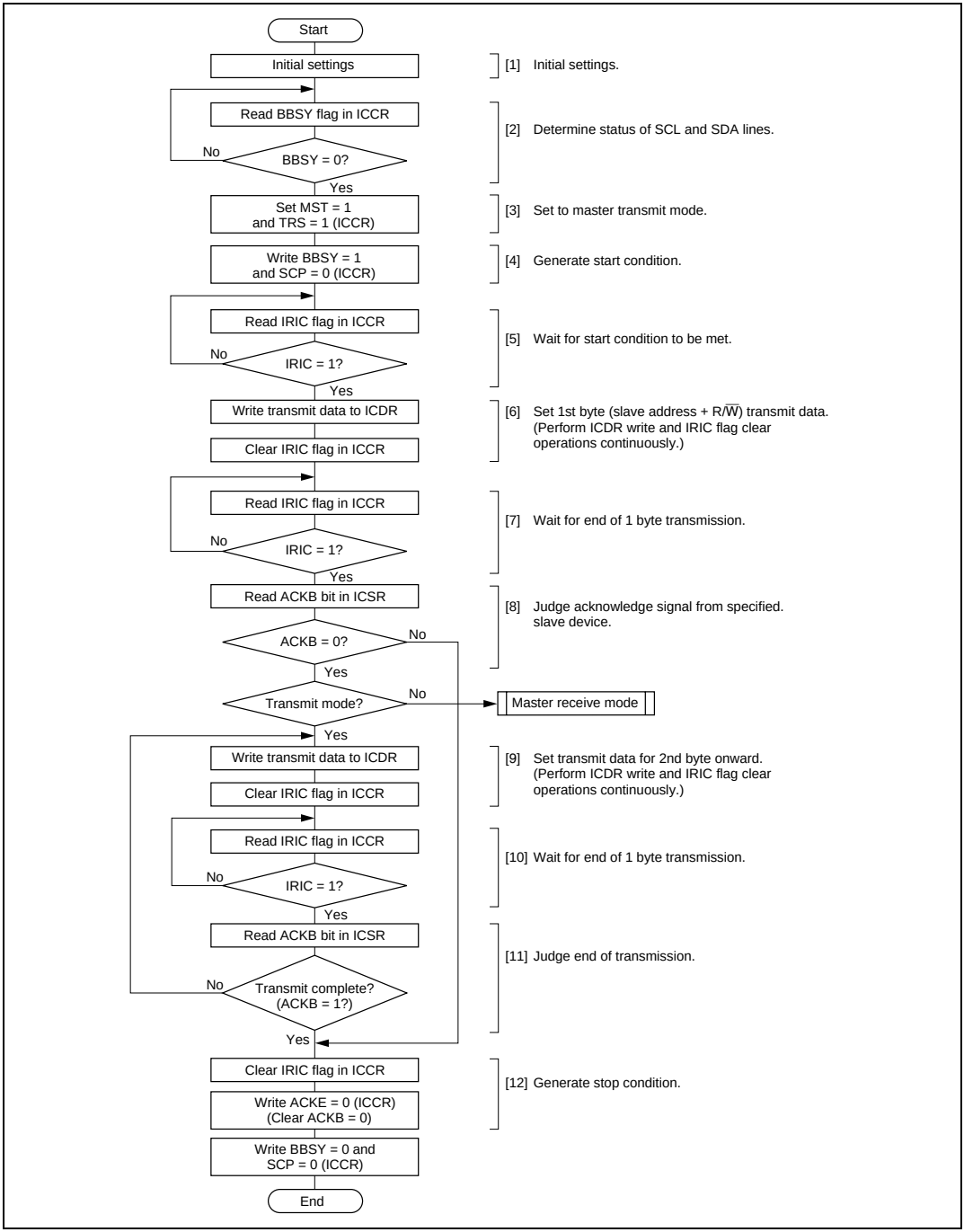


Figure 14.7 Flowchart for Master Transmit Mode (Example)

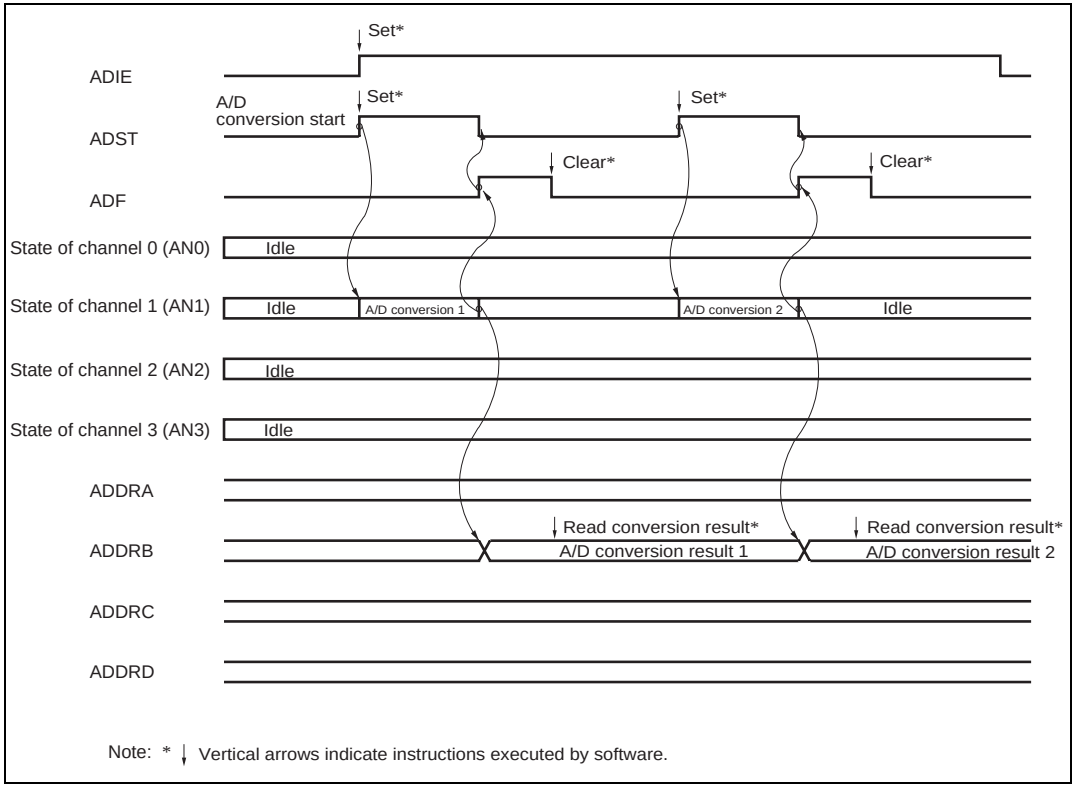


Figure 15.3 Example of A/D Converter Operation (Single Mode, Channel 1 Selected)

Section 17 LCD Controller/Driver

The H8S/2268 has an on-chip segment type LCD control circuit, LCD driver, and power supply circuit, enabling it to directly drive an LCD panel.

17.1 Features

Features of the LCD controller/driver are given below.

- Display capacity

Duty Cycle	Internal Driver
Static	40 SEG
1/2	40 SEG
1/3	40 SEG
1/4	40 SEG

- LCD RAM capacity
  8 bits × 20 bytes (160 bits)
  Byte or word access to LCD RAM
- The segment output pins can be used as ports.
  H8S/2268 Group: SEG40 to SEG1 pins can be used as ports in groups of eight.
  H8S/2264 Group: SEG24 to SEG1 pins can be used as ports in groups of eight.
- Common output pins not used because of the duty cycle can be used for common double-buffering (parallel connection).
  With 1/2 duty, parallel connection of COM1 to COM2, and of COM3 to COM4, can be used
  In static mode, parallel connection of COM1 to COM2, COM3, and COM4 can be used
- Choice of 11 frame frequencies
- A or B waveform selectable by software
- Built-in power supply split-resistance
- Display possible in operating modes other than standby mode and module stop mode
- Display possible during low-voltage operation by built-in triple step-up voltage circuit (supposrted only by the H8S/2268 Group)
- Module stop mode
  As the initial setting, LCD operation is halted. Access to registers and LCD RAM is enabled by clearing module stop mode.

Section 21 Clock Pulse Generator

This LSI has an on-chip clock pulse generator that generates the system clock (ϕ), the bus master clock, and internal clocks. The clock pulse generator consists of an oscillator, duty adjustment circuit, clock selection circuit, medium-speed clock divider, bus master clock selection circuit, subclock oscillator, and wave formation circuit. A block diagram of the clock pulse generator is shown in figure 21.1.

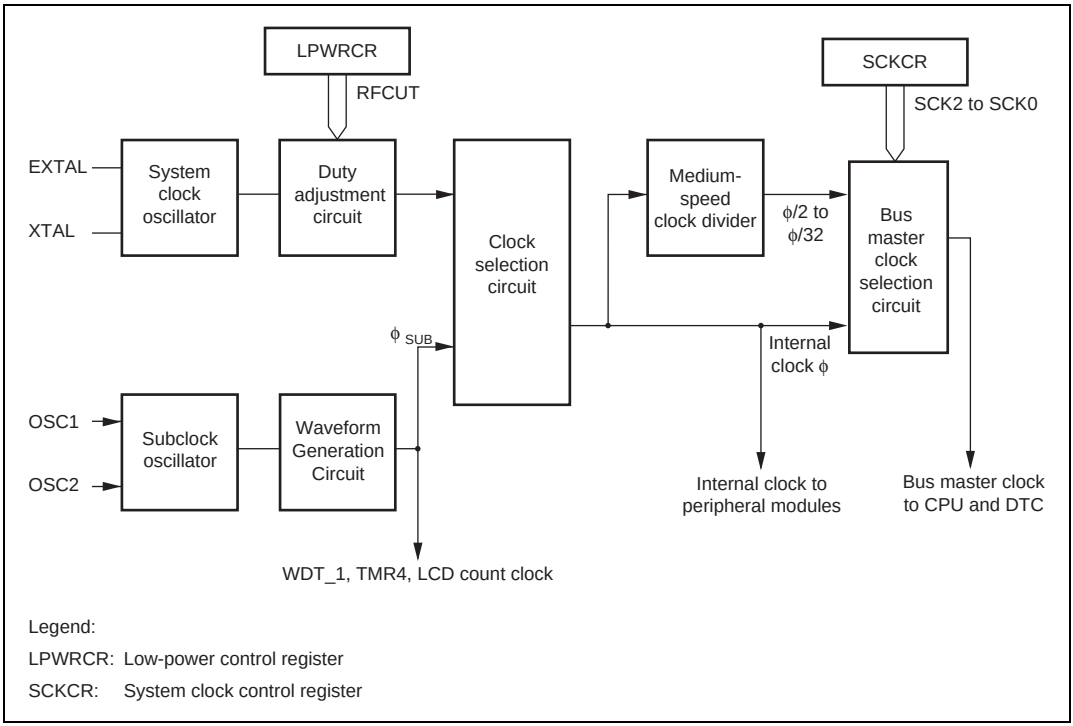


Figure 21.1 Block Diagram of Clock Pulse Generator

Frequency changes are performed by software by settings in the low-power control register (LPWRCR) and system clock control register (SCKCR).

22.11.4 On-Chip Peripheral Module Interrupt

- Module stop mode

  Relevant interrupt operations cannot be performed in module stop mode. Consequently, if module stop mode is entered when an interrupt has been requested, it will not be possible to clear the CPU interrupt source or the DTC* activation source. Interrupts should therefore be disabled before entering module stop mode.

  Note: Supported only by the H8S/2268 Group.

- Subactive mode / Watch mode

  On-chip peripheral modules (DTC*, TPU, IIC) that stop operation in subactive mode cannot clear interrupts in subactive mode. Therefore, if subactive mode is entered when an interrupt is requested, CPU interrupt factors cannot be cleared.

  Interrupts should therefore before executing the SLEEP instruction and entering subactive or watch mode.

  Note: * Supported only by the H8S/2268 Group.

22.11.5 Writing to MSTPCR

MSTPCR should only be written to by the CPU.

22.11.6 Entering Subactive/Watch Mode and DTC Module Stop (Supported Only by H8S/2268 Group)

To enter subactive or watch mode, set DTC to module stop (write 1 to the MSTPA6 bit) and reading the MSTPA6 bit as 1 before transiting mode. After transiting from subactive mode to active mode, clear module stop.

When DTC activation factor occurs in subactive mode, DTC is activated when module stop is cleared after active mode is entered.

Register Name	Abbreviation	Bit No.	Address*1	Module	Data Width	Access State
Port H data direction register	PHDDR	8	H'FC80	PORT	8	4
Port J data direction register	PJDDR	8	H'FC81	PORT	8	4
Port K data direction register	PKDDR	8	H'FC82	PORT	8	4
Port L data direction register	PLDDR	8	H'FC83	PORT	8	4
Port M data direction register*4	PMDDR	8	H'FC84	PORT	8	4
Port N data direction register*4	PNDDR	8	H'FC85	PORT	8	4
Port H data register	PHDR	8	H'FC88	PORT	8	4
Port J data register	PJDR	8	H'FC89	PORT	8	4
Port K data register	PKDR	8	H'FC8A	PORT	8	4
Port L data register	PLDR	8	H'FC8B	PORT	8	4
Port M data register*4	PMDR	8	H'FC8C	PORT	8	4
Port N data register*4	PNDR	8	H'FC8D	PORT	8	4
Port H register	PORTH	8	H'FC90	PORT	8	4
Port J register	PORTJ	8	H'FC91	PORT	8	4
Port K register	PORTK	8	H'FC92	PORT	8	4
Port L register	PORTL	8	H'FC93	PORT	8	4
Port M register*4	PORTM	8	H'FC94	PORT	8	4
Port N register*4	PORTN	8	H'FC95	PORT	8	4
Port J pull-up MOS control register	PJPCR	8	H'FC99	PORT	8	4
Wakeup control register	WPCR	8	H'FC9F	PORT	8	4
Wakeup interrupt request register	IWPR	8	H'FCA0	INT	8	4
Interrupt enable register	IENR1	8	H'FCA1	INT	8	4
D/A data register_0*4	DADR_0	8	H'FDAC	D/A	8	2
D/A data register_1*4	DADR_1	8	H'FDAD	D/A	8	2
D/A control register*4	DACR	8	H'FDAE	D/A	8	2
Serial control register X	SCRX	8	H'FDB4	IIC, FLASH	8	2
DDC switch register	DDCSWR	8	H'FDB5	IIC	8	2
Timer control register_2*4	TCR_2	8	H'FDC0	TMR_2	8	2

25.2.8 Flash Memory Characteristics

Table 25.13 shows the flash memory characteristics.

Table 25.13 Flash Memory Characteristics

Condition: V_{CC} = 3.0 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = –25°C to +75°C (Programming/erasing operating temperature range: regular specification)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Programming time*1*2*4		t_p	—	30	200	ms/ 128 bytes	
Erase time*1*3*5		t_E	—	100	1200	ms/block	
Count of rewriting		N_{WEC}	100*6	10000*7	—	Times	
Data retention time		T_{DRP}*8	10	—	—	Year	
Programming	Wait time after SWE1 bit setting*1	t_{sswe}	1	1	—	µs	
	Wait time after PSU1 bit setting*1	t_{spsu}	50	50	—	µs	
	Wait time after P1 bit setting*1*4	t_{sp10}	8	10	12	µs	
		t_{sp30}	28	30	32	µs	6 ≥ n ≥ 1
		t_{sp200}	198	200	202	µs	1000 ≥ n ≥ 7
	Wait time after P1 bit clear*1	t_{cp}	5	5	—	µs	
	Wait time after PSU1 bit clear*1	t_{cpsu}	4	4	—	µs	
	Wait time after PV1 bit setting*1	t_{spv}	2	2	—	µs	
	Wait time after H'FF dummy write*1	t_{spvr}	2	2	—	µs	
	Wait time after PV1 bit clear*1	t_{cpv}	100	100	—	µs	
	Wait time after SWE1 bit clear	t_{cswe}	—	—	—	µs	
	Maximum programming count*1*4	N1	—	—	6*4	Times	
		N2	—	—	994*4	Times	
Erase	Wait time after SWE1 bit setting*1	t_{sswe}	1	1	—	µs	
	Wait time after ESU1 bit setting*1	t_{sesu}	100	100	—	µs	
	Wait time after E1 bit setting*1*5	t_{se}	10	10	100	ms	
	Wait time after E1 bit clear*1	t_{ce}	10	10	—	µs	
	Wait time after ESU1 bit clear*1	t_{cesu}	10	10	—	µs	
	Wait time after EV1 bit setting*1	t_{sev}	20	20	—	µs	
	Wait time after H'FF dummy write*1	t_{sevr}	2	2	—	µs	
	Wait time after EV1 bit clear*1	t_{cev}	4	4	—	µs	
	Wait time after SWE1 bit clear	t_{cswe}	100	100	—	µs	
	Maximum erase count*1*5	N	—	—	100	Times	

Timing of On-Chip Peripheral Modules: Table 25.20 lists the timing of on-chip peripheral modules. Table 25.21 lists the I^2C bus timing.

Table 25.20 Timing of On-Chip Peripheral Modules

Condition B (Masked-ROM version): V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{ref} = 2.7 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 2 to 13.5 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Condition D (Masked-ROM version): V_{CC} = 4.0 V to 5.5 V, AV_{CC} = 4.0 V to 5.5 V, V_{ref} = 4.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 32.768 kHz, 10 to 20.5 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item			Symbol	Condition B Min.	Condition B Max.	Condition D Min.	Condition D Max.	Unit	Test Conditions
TPU	Timer clock pulse width	Single edge	t_{TCKWH}	1.5	—	1.5	—	t_{cyc}	Figure 25.7
		Both edges	t_{TCKWL}	2.5	—	2.5	—		
TMR_0, TMR_1	Timer clock pulse width	Single edge	t_{TMCWH}	1.5	—	1.5	—	t_{cyc}	Figure 25.8
		Both edges	t_{TMCWL}	2.5	—	2.5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	4	—	t_{cyc}	Figure 25.9
		Synchronous		6	—	6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	1.5	—	1.5	t_{cyc}	
	Input clock fall time		t_{SCKf}	—	1.5	—	1.5		
	Transmit data delay time		t_{TXD}	—	75	—	50	ns	Figure 25.10
	Receive data setup time (synchronous)		t_{RXS}	75	—	50	—	ns	
	Receive data hold time (synchronous)		t_{RXH}	75	—	50	—	ns	