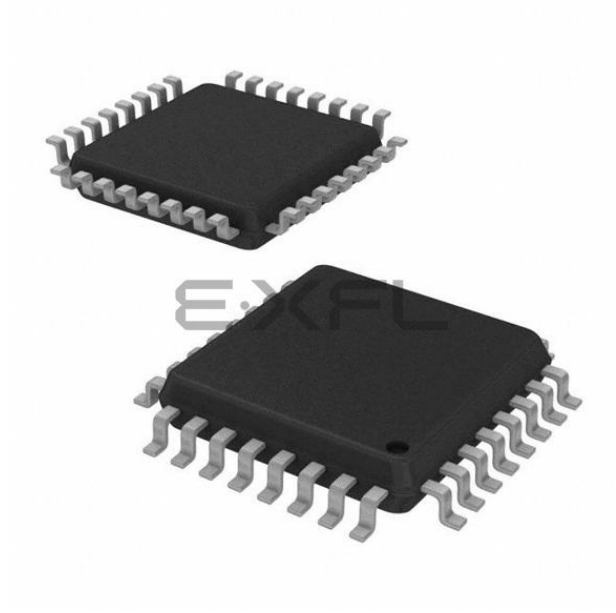

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What is "Embedded - Microcontrollers"?

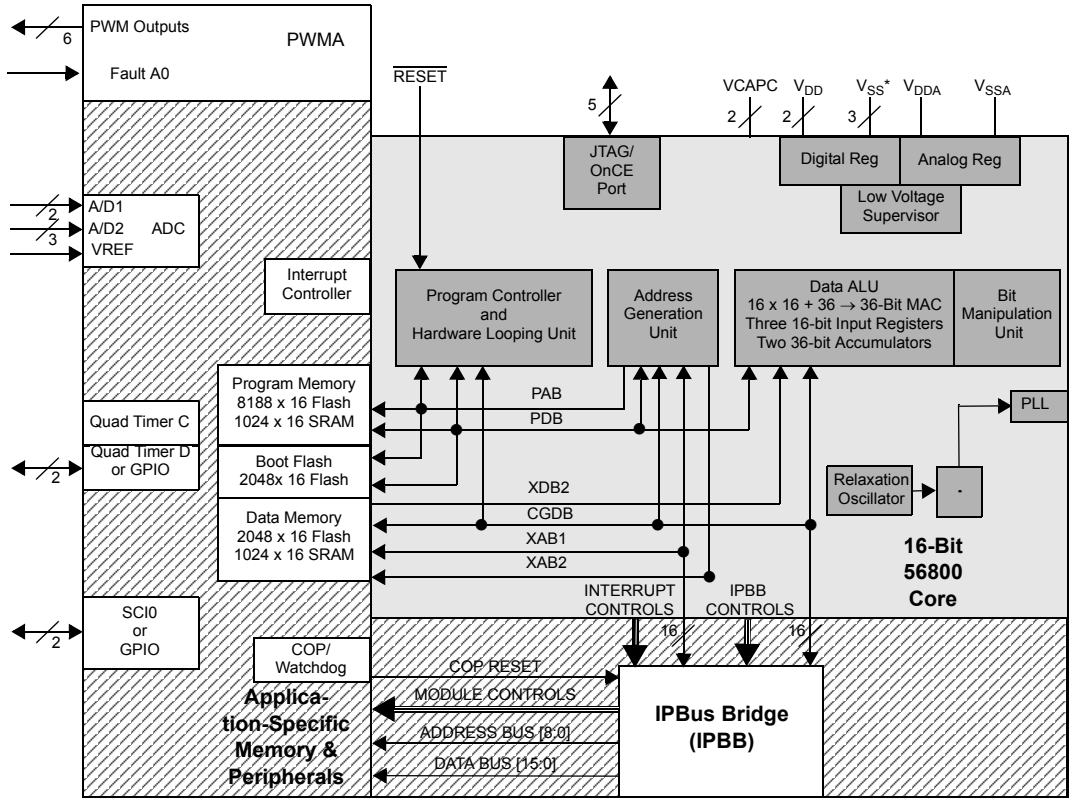
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	60MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	8
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f802ta60e

56F802 General Description

- Up to 30 MIPS operation at 60MHz core frequency
- Up to 40 MIPS operation at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- Hardware DO and REP loops
- 6-channel PWM Module with fault input
- Two 12-bit ADCs (1 x 2 channel, 1 x 3 channel)
- Serial Communications Interface (SCI)
- Two General Purpose Quad Timers with 2 external outputs
- 8K × 16-bit words (16KB) Program Flash
- 1K × 16-bit words (2KB) Program RAM
- 2K × 16-bit words (4KB) Data Flash
- 1K × 16-bit words (2KB) Data RAM
- 2K × 16-bit words (4KB) Boot Flash
- JTAG/OnCE™ port for debugging
- On-chip relaxation oscillator
- 4 shared GPIO
- 32-pin LQFP Package



*includes TCS pin which is reserved for factory use and is tied to VSS

56F802 Block Diagram

- Computer-Operating Properly (COP) watchdog timer
- External interrupts via GPIO
- Trimmable on-chip relaxation oscillator
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the controller core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- Integrated power supervisor

1.2 56F802 Description

The 56F802 is a member of the 56800 core-based family of processors. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F802 is well-suited for many applications. The 56F802 includes many peripherals that are especially useful for applications such as motion control, home appliances, encoders, tachometers, limit switches, power supply and control, engine management, and industrial control for power, lighting, automation and HVAC.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F802 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F802 also provides and up to 4 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F802 controller includes 8K words (16-bit) of Program Flash and 2K words of Data Flash (each programmable through the JTAG port) with 1K words of both Program and Data RAM. A total of 2K words of Boot Flash is incorporated for easy customer-inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F802 is the inclusion of a Pulse Width Modulator (PWM) module. This modules incorporates six complementary, individually programmable PWM signal outputs to enhance motor control functionality. Complementary operation permits programmable dead-time

insertion, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width control (0% to 100% modulation) are supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection with sufficient output drive capability to directly drive standard opto-isolators. A "smoke-inhibit", write-once protection feature for key parameters is also included. The PWM is double-buffered and includes interrupt control to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the Analog-to-Digital Converters.

The 56F802 incorporates two 12-bit Analog-to-Digital Converters (ADCs) with a total of five channels. A full set of standard programmable peripherals is provided that include a Serial Communications Interface (SCI), and two Quad Timers. Any of these interfaces can be used as General-Purpose Input/Outputs (GPIO) if that function is not required. An on-chip relaxation oscillator eliminates the need for an external crystal.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F802. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F802 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F802, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F802 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F802
56F802 Errata	Details any chip issues that might be present	56F802E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications

2.3 Interrupt and Program Control Signals

Table 2-5 Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RESET**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When RESET is asserted low, the controller is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert RESET, but do not assert TRST.

2.4 Pulse Width Modulator (PWM) Signals

Table 2-6 Pulse Width Modulator (PWMA) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0-5**	Output	Tri-stated	**PWMA0-5**— These are six PWMA output pins.
1	**FAULTA0**	Input (Schmitt)	Input	**FAULTA0** —This fault input is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.

2.5 Serial Communications Interface (SCI) Signals

Table 2-7 Serial Communications Interface (SCI0) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—SCI0 transmit data output
	GPIOB0	Input/Output	Input	**Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCI output.

Table 2-7 Serial Communications Interface (SCI0) Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RXD0**	Input	Input	**Receive Data (RXD0)**—SCI0 receive data input
	GPIOB1	Input/ Output	Input	**Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCI input.

2.6 Analog-to-Digital Converter (ADC) Signals

Table 2-8 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
3	**ANA2-4**	Input	Input	**ANA2-4**—Analog inputs to ADC, channel 1
2	**ANA6-7**	Input	Input	**ANA6-7**—Analog inputs to ADC, channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage. Must be set to V_{DDA} - 0.3V for optimal performance.

2.7 Quad Timer Module Signals

Table 2-9 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TD1-2**	Input/ Output	Input	**TD1-2**—Timer D Channel 1-2
	GPIOA1-2	Input/ Output	Input	**Port A GPIO**—These pins are General Purpose I/O (GPIO) pins that can be individually programmed as input or output pins. After reset, the default state is the quad timer input.

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
ADC reference voltage[1]	VREF	2.7	–	V_{DDA}	V
Ambient operating temperature	T_A	–40	–	85	°C

1. VREF must be 0.3V below V_{DDA}.

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			32-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.2	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	47.1	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	38.7	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	37.4	°C/W	1,2
Junction to case		$R_{\theta JC}$	17.8	°C/W	3
Junction to center of case		Ψ_{JT}	3.07	°C/W	4
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where s is the number of signal layers and p is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.

- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

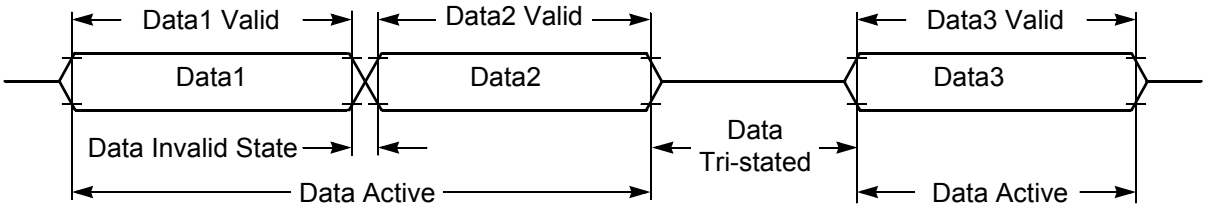


Figure 3-3 Signal States

3.4 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both blocks	Erase main memory block

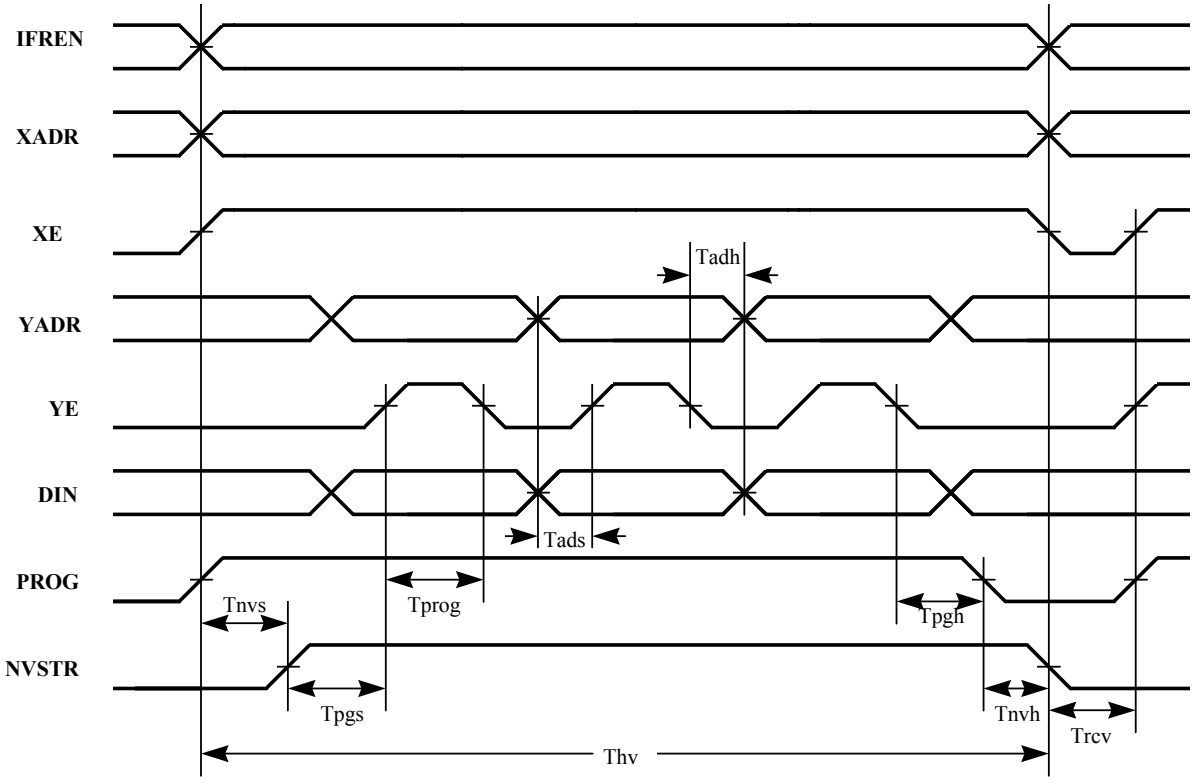


Figure 3-4 Flash Program Cycle

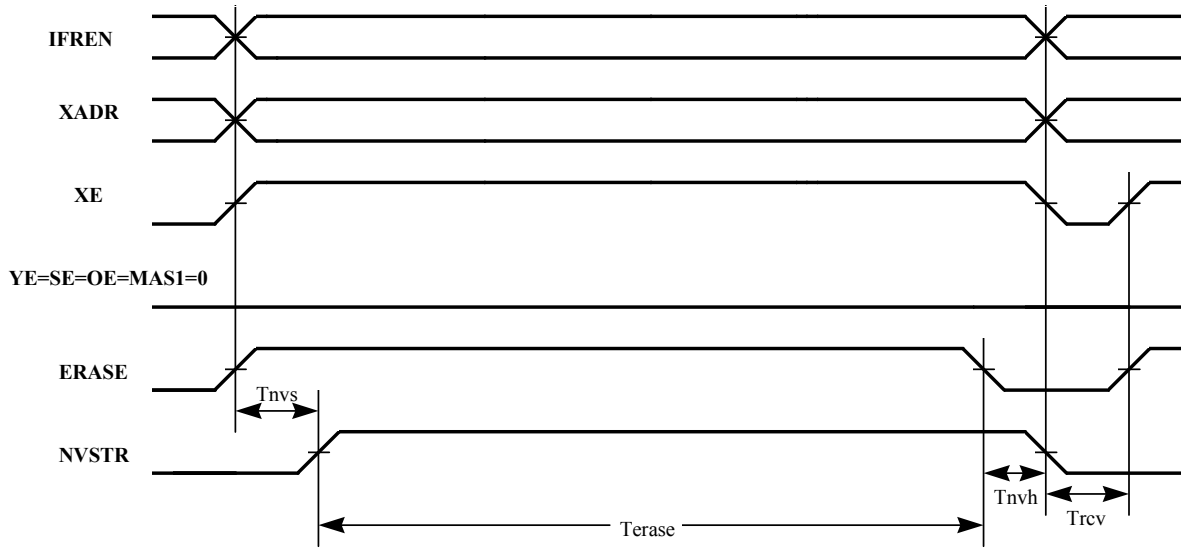


Figure 3-5 Flash Erase Cycle

Due to the inherent frequency tolerances required for SCI communication, changing the factory-trimmed oscillator frequency is not recommended. If modification of the Boot Flash contents are required, code must be included which retrieves the optimum trim value (from address $103F in the Data Flash Information Block) and writes it to the IOSCTL register. Note that the IFREN bit in the Data Flash control register must be set in order to read the Data Flash Information Block.

Table 3-8 Relaxation Oscillator Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Accuracy[1]	Δf	—	±2	±5	%
Frequency Drift over Temp	Δf/Δt	—	±0.1	—	%/°C
Frequency Drift over Supply	Δf/ΔV	—	0.1	—	%/V

1. Over full temperature range.

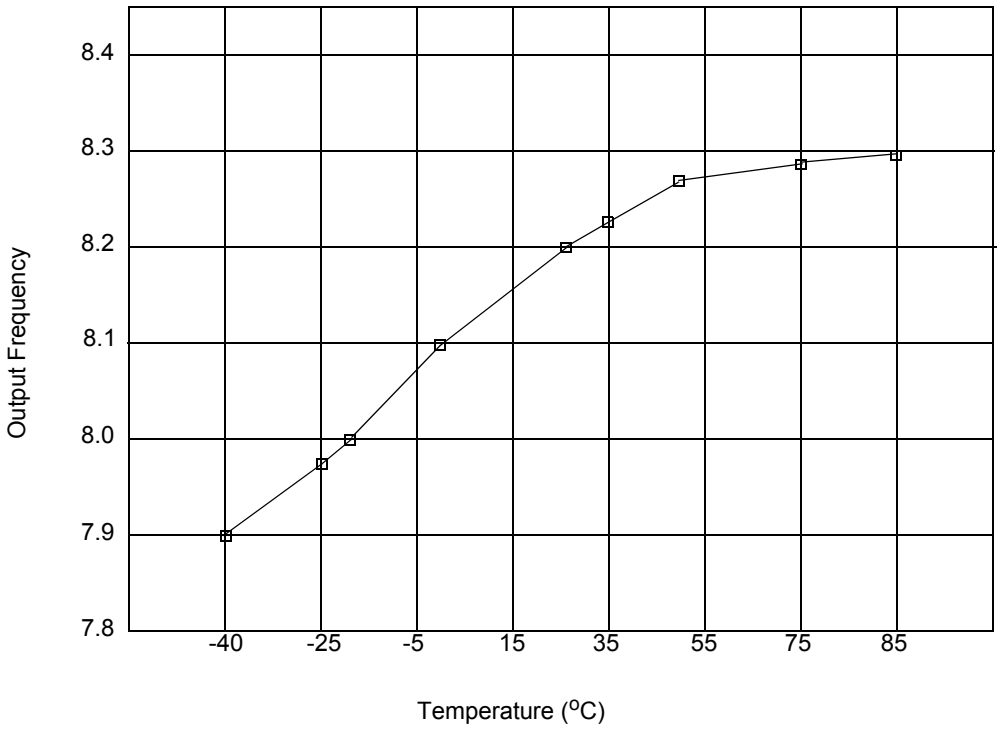


Figure 3-7 Typical Relaxation Oscillator Frequency vs. Temperature (Trimmed to 8MHz @ 25°C)

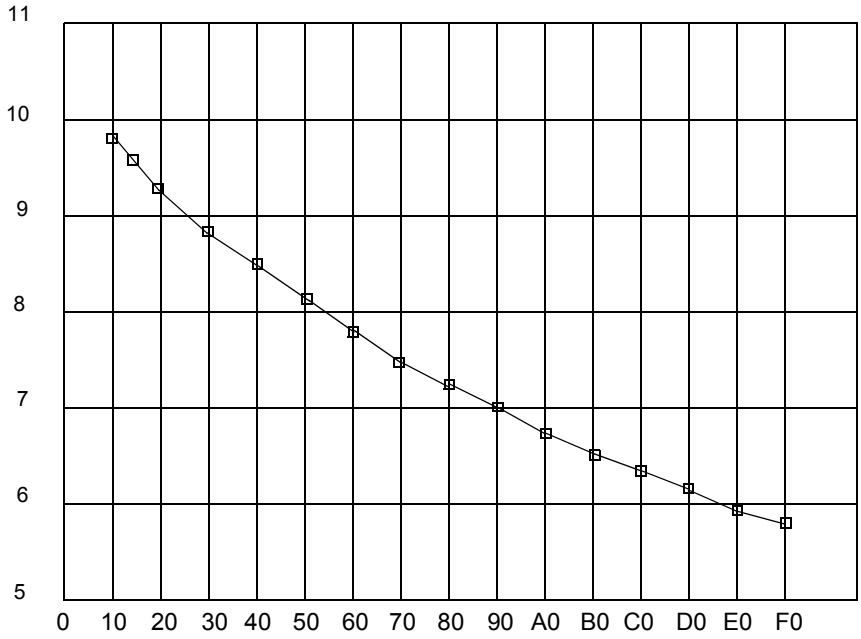


Figure 3-8 Typical Relaxation Oscillator Frequency vs. Trim Value @ 25°C

3.5.2 Phase Locked Loop Timing

Table 3-9 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency for the PLL[1]	f_{osc}	4	8	10	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	80[3]	MHz
PLL stabilization time[4] 0° to +85°C	t_{plls}	—	10	—	ms
PLL stabilization time[4] -40° to 0°C	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. Will not exceed 60MHz for the DSP56F802TA60 device.
4. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

3.7 Quad Timer Timing

Table 3-11 Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T	—	ns
Timer output high/low period	P_{OUTHL}	1T	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5 ns.
2. Parameters listed are guaranteed by design.

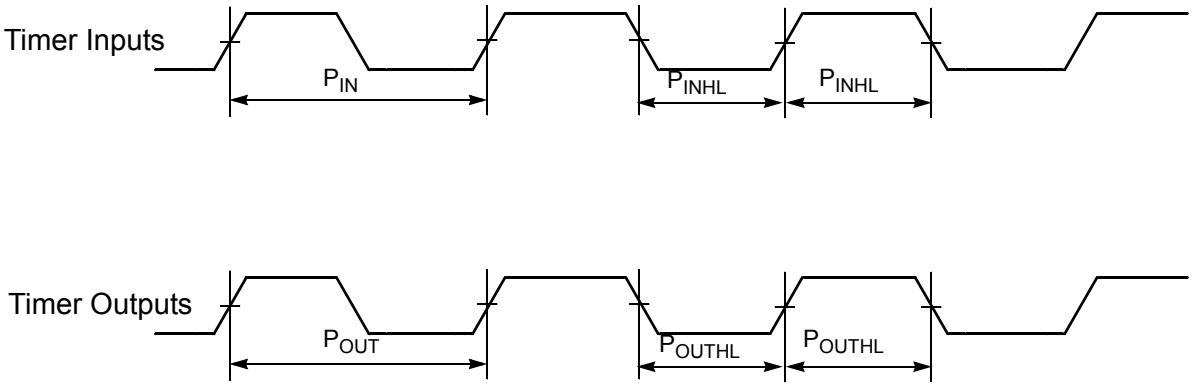
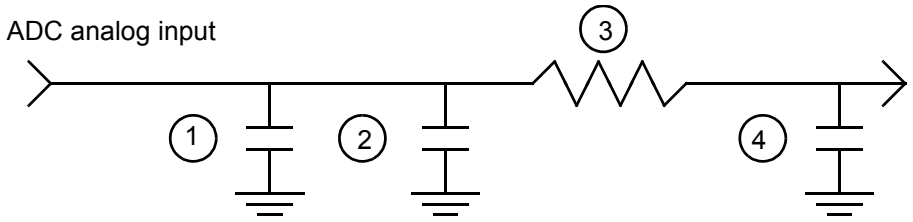


Figure 3-10 Timer Timing



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. (1pf)

Figure 3-13 Equivalent Analog Input Circuit

3.10 JTAG Timing

Table 3-14 JTAG Timing [1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data setup time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

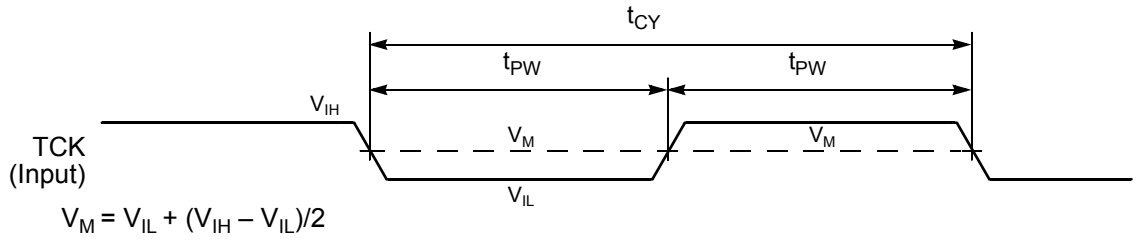


Figure 3-14 Test Clock Input Timing Diagram

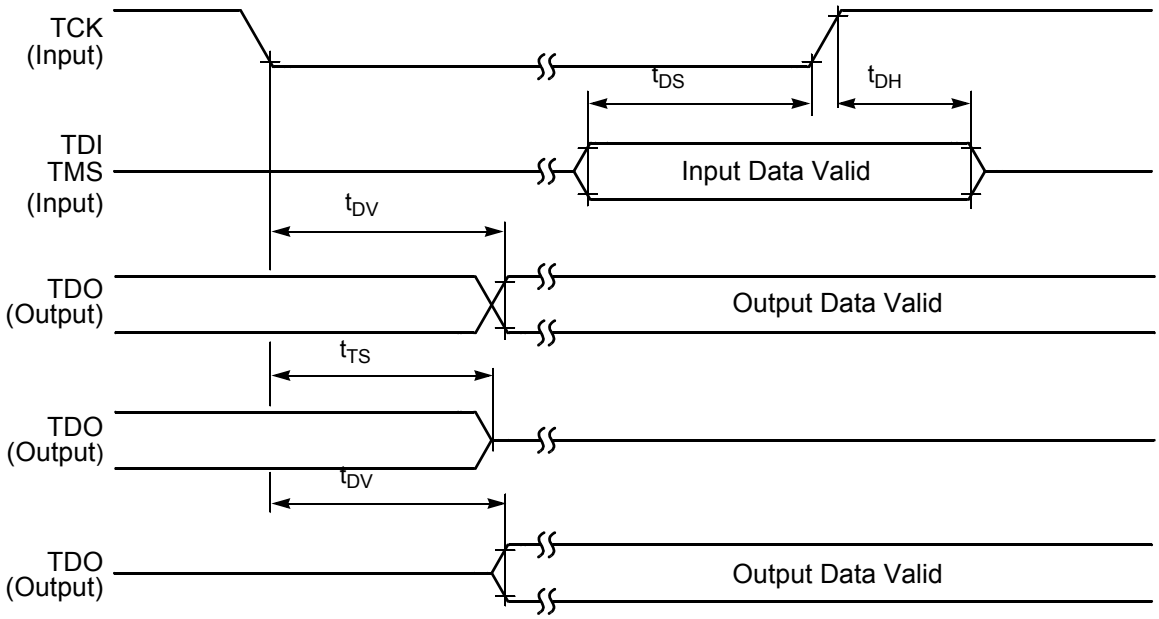


Figure 3-15 Test Access Port Timing Diagram

Figure 3-16 $\overline{\text{TRST}}$ Timing Diagram

Part 4 Packaging

4.1 Package and Pin-Out Information 56F802

This section contains package and pin-out information for the 32-pin LQFP configuration of the 56F802.

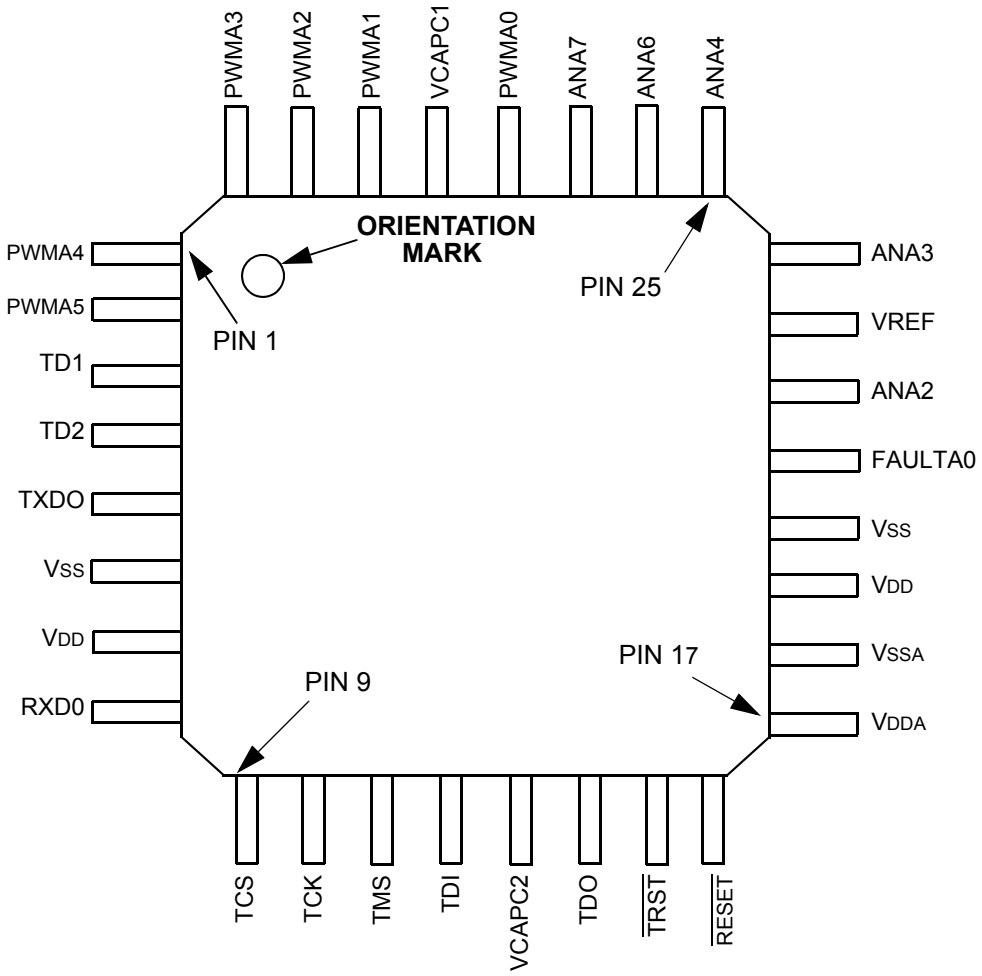
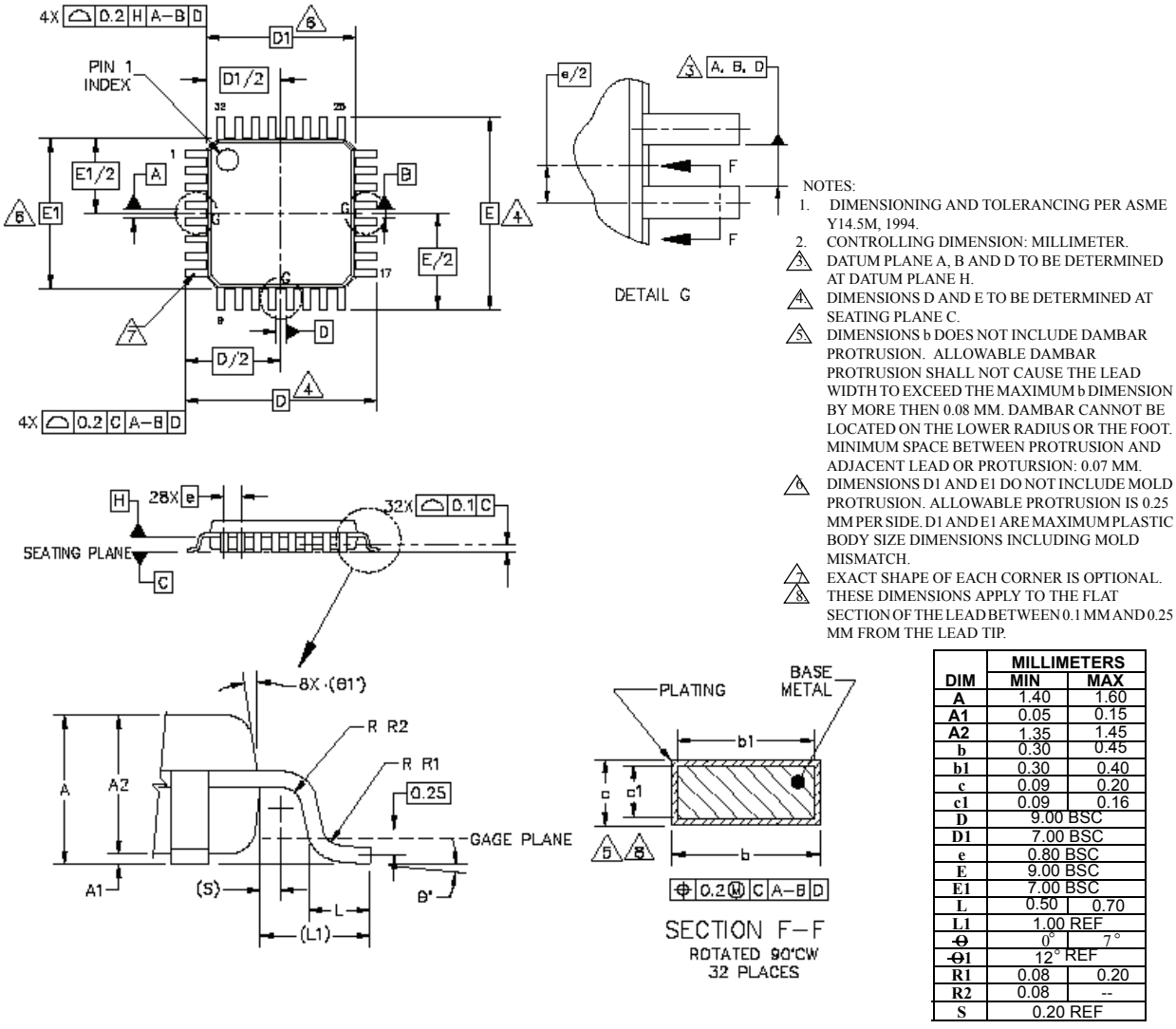


Figure 4-1 Top View, 56F802 32-pin LQFP Package



DIM	MILLIMETERS MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
θ	0°	7°
θ1	12° REF	
R1	0.08	0.20
R2	0.08	--
S	0.20 REF	

Figure 4-2 32-pin LQFP Mechanical Information (Case 873A)

Please see **www.freescale.com** for the most current case outline.

- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.

Part 6 Ordering Information

Table 6-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 6-1 56F802 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F802	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	32	80	DSP56F802TA80
56F802	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	32	60	DSP56F802TA60
56F802	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	32	80	DSP56F802TA80E*
56F802	3.0–3.6 V	Low Profile Plastic Quad Flat Pack (LQFP)	32	60	DSP56F802TA60E*

*This package is RoHS compliant.

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RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to http://www.freescale.com/epp.

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