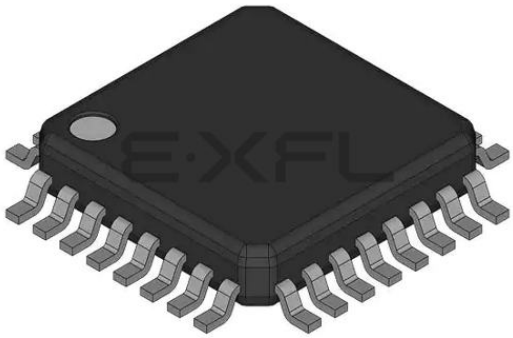


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	8
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56f802ta80e

- Computer-Operating Properly (COP) watchdog timer
- External interrupts via GPIO
- Trimmable on-chip relaxation oscillator
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the controller core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available
- Integrated power supervisor

1.2 56F802 Description

The 56F802 is a member of the 56800 core-based family of processors. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F802 is well-suited for many applications. The 56F802 includes many peripherals that are especially useful for applications such as motion control, home appliances, encoders, tachometers, limit switches, power supply and control, engine management, and industrial control for power, lighting, automation and HVAC.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The 56F802 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F802 also provides and up to 4 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F802 controller includes 8K words (16-bit) of Program Flash and 2K words of Data Flash (each programmable through the JTAG port) with 1K words of both Program and Data RAM. A total of 2K words of Boot Flash is incorporated for easy customer-inclusion of field-programmable software routines that can be used to program the main Program and Data Flash memory areas. Both Program and Data Flash memories can be independently bulk erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F802 is the inclusion of a Pulse Width Modulator (PWM) module. This modules incorporates six complementary, individually programmable PWM signal outputs to enhance motor control functionality. Complementary operation permits programmable dead-time

insertion, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Both edge- and center-aligned synchronous pulse width control (0% to 100% modulation) are supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection with sufficient output drive capability to directly drive standard opto-isolators. A "smoke-inhibit", write-once protection feature for key parameters is also included. The PWM is double-buffered and includes interrupt control to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the Analog-to-Digital Converters.

The 56F802 incorporates two 12-bit Analog-to-Digital Converters (ADCs) with a total of five channels. A full set of standard programmable peripherals is provided that include a Serial Communications Interface (SCI), and two Quad Timers. Any of these interfaces can be used as General-Purpose Input/Outputs (GPIO) if that function is not required. An on-chip relaxation oscillator eliminates the need for an external crystal.

1.3 State of the Art Development Environment

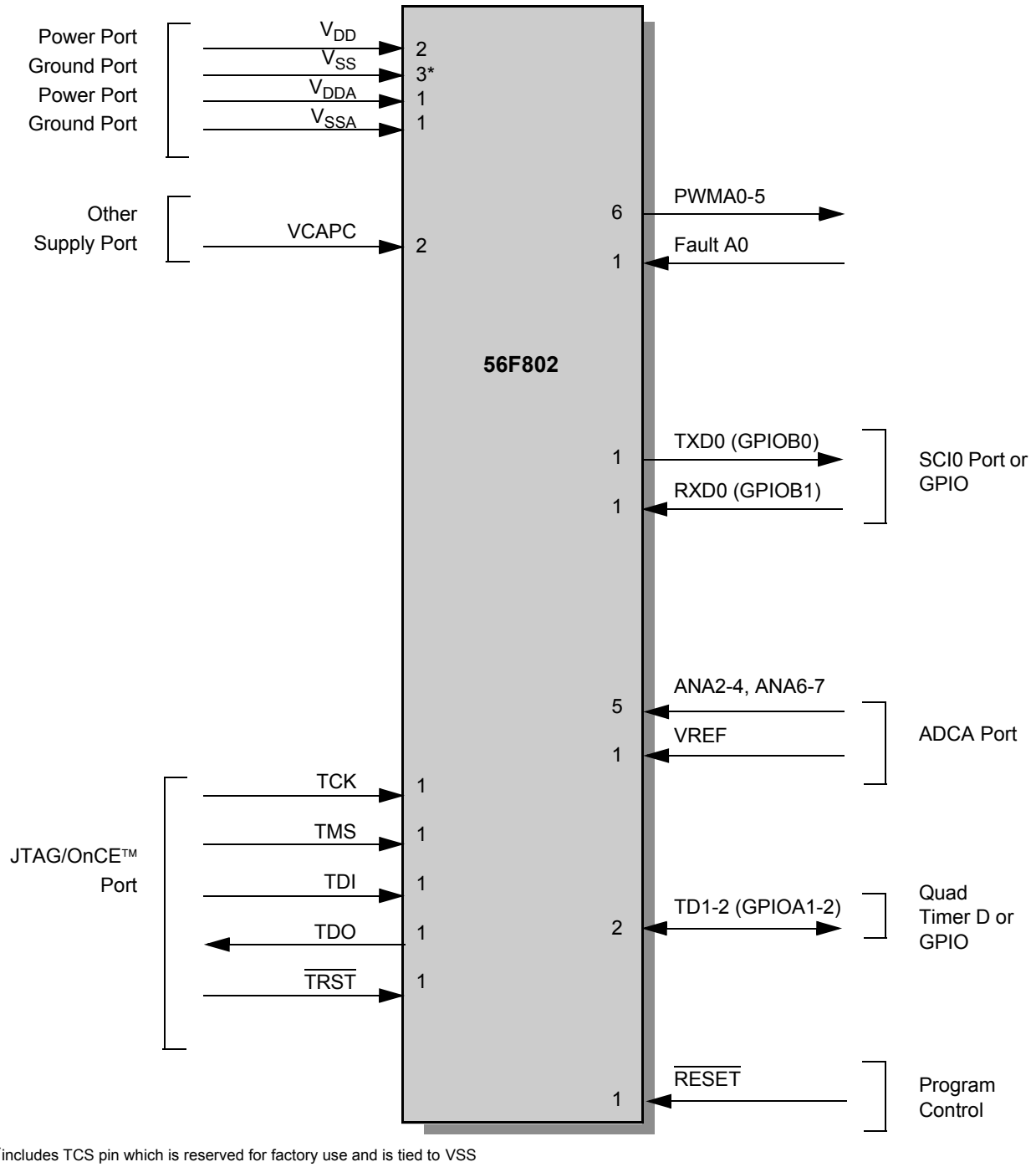
- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F802. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F802 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F802, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F802 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F802
56F802 Errata	Details any chip issues that might be present	56F802E



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F802 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Power and Ground Signals

Table 2-2 Power Inputs

No. of Pins	Signal Name	Signal Description
2	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
1	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the chip and should be connected to a low noise 3.3V supply.

Table 2-3 Grounds

No. of Pins	Signal Name	Signal Description
2	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip, and should all be attached to V_{SS}.
1	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This Schmitt pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 2-4 Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC**—Connect each pin to a 2.2 μF or greater bypass capacitor in order to bypass the core logic voltage regulator (required for proper chip operation). For more information, refer to **Section 5.2**

2.3 Interrupt and Program Control Signals

Table 2-5 Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RESET**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When RESET is asserted low, the controller is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert RESET, but do not assert TRST.

2.4 Pulse Width Modulator (PWM) Signals

Table 2-6 Pulse Width Modulator (PWMA) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0-5**	Output	Tri-stated	**PWMA0-5**— These are six PWMA output pins.
1	**FAULTA0**	Input (Schmitt)	Input	**FAULTA0** —This fault input is used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.

2.5 Serial Communications Interface (SCI) Signals

Table 2-7 Serial Communications Interface (SCI0) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—SCI0 transmit data output
	GPIOB0	Input/Output	Input	**Port B GPIO**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as an input or output pin. After reset, the default state is SCI output.

The 56F802 DC and AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog Inputs ANAx, V_{REF}	V_{IN}	V_{SS} – 0.3	V_{DDA} + 0.3V	V
Current drain per pin excluding V_{DD}, V_{SS}, & PWM ouputs	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V

5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[1]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[2]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[2]	I_{ILA}	-15	—	15	µA
Output High Voltage (at IOH)	V_{OH}	V_{DD} – 0.7	—	—	V

10. Power—on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.5V typical no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self regulates.

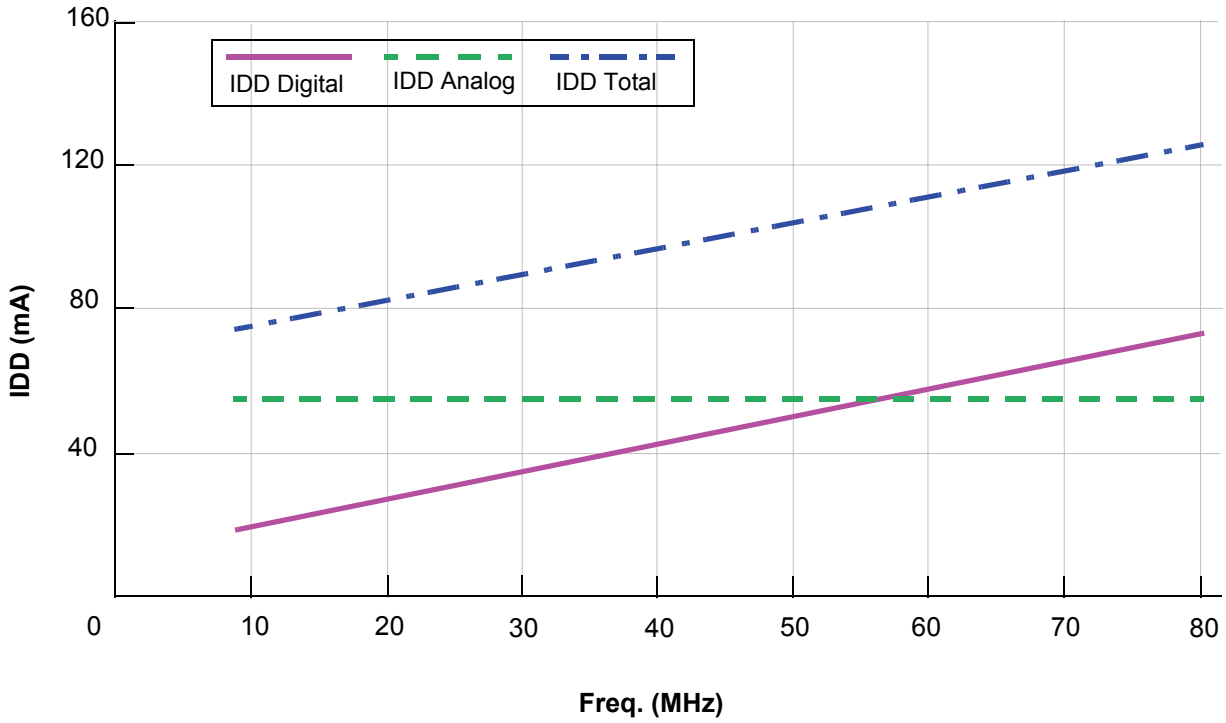
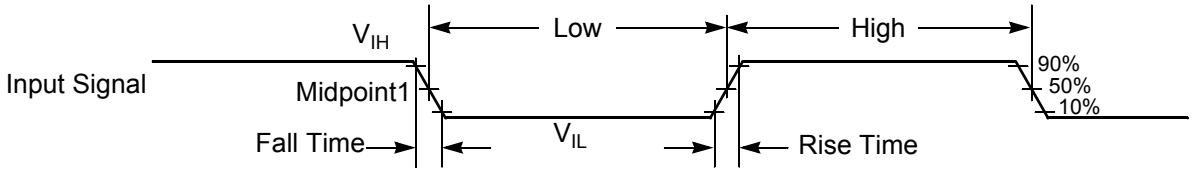


Figure 3-1 Maximum Run IDD vs. Frequency (see Note 6. in Table 3-4)

3.3 AC Electrical Characteristics

Timing waveforms in Section 3.3 are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In Figure 3-2 the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-2 Input Signal Measurement References

Figure 3-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state

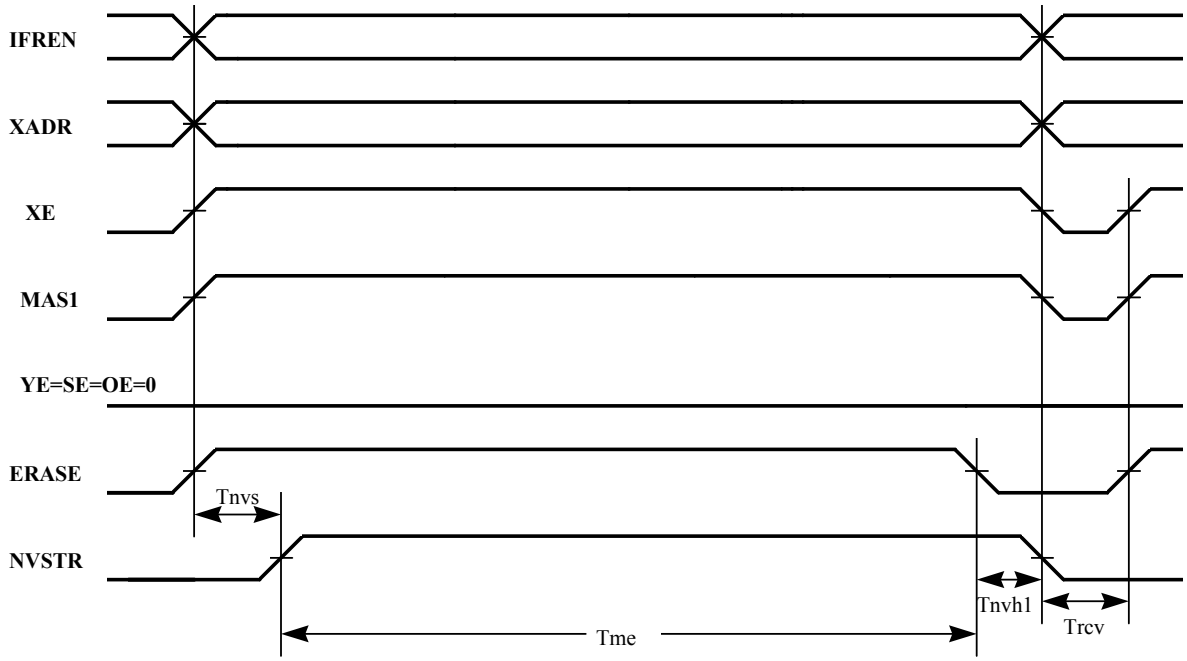


Figure 3-6 Flash Mass Erase Cycle

3.5 Clock Operation

The 56F802 device clock is derived from an on-chip relaxation oscillator. The internal PLL generates a master reference frequency that determines the speed at which chip operations occur.

The PRECS bit in the PLLCR (phase-locked loop control register) word (bit 2) must be set to 0 for internal oscillator use.

3.5.1 Use of On-Chip Relaxation Oscillator

The 56F802 internal relaxation oscillator provides the chip clock without the need for an external crystal or ceramic resonator. The frequency output of this internal oscillator can be corrected by adjusting the 8-bit IOSCTL (internal oscillator control) register. Each bit added or deleted changes the output frequency of the oscillator allowing incremental adjustment until the desired frequency is achieved. Figures 9 and 10 show the typical characteristics of the 56F802 relaxation oscillator with respect to temperature and trim value.

During factory production test, an oscillator calibration procedure is executed which determines an optimum trim value for a given device (8MHz at 25^{o}C). This optimum trim value is then stored at address $103F in the Data Flash Information Block and recalled during a trim routine in the boot sequence (executed after power-up and RESET). This trim routine automatically sets the oscillator frequency by programming the IOSCTL register with the optimum trim value.

Due to the inherent frequency tolerances required for SCI communication, changing the factory-trimmed oscillator frequency is not recommended. If modification of the Boot Flash contents are required, code must be included which retrieves the optimum trim value (from address $103F in the Data Flash Information Block) and writes it to the IOSCTL register. Note that the IFREN bit in the Data Flash control register must be set in order to read the Data Flash Information Block.

Table 3-8 Relaxation Oscillator Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Accuracy[1]	Δf	—	±2	±5	%
Frequency Drift over Temp	Δf/Δt	—	±0.1	—	%/°C
Frequency Drift over Supply	Δf/ΔV	—	0.1	—	%/V

1. Over full temperature range.

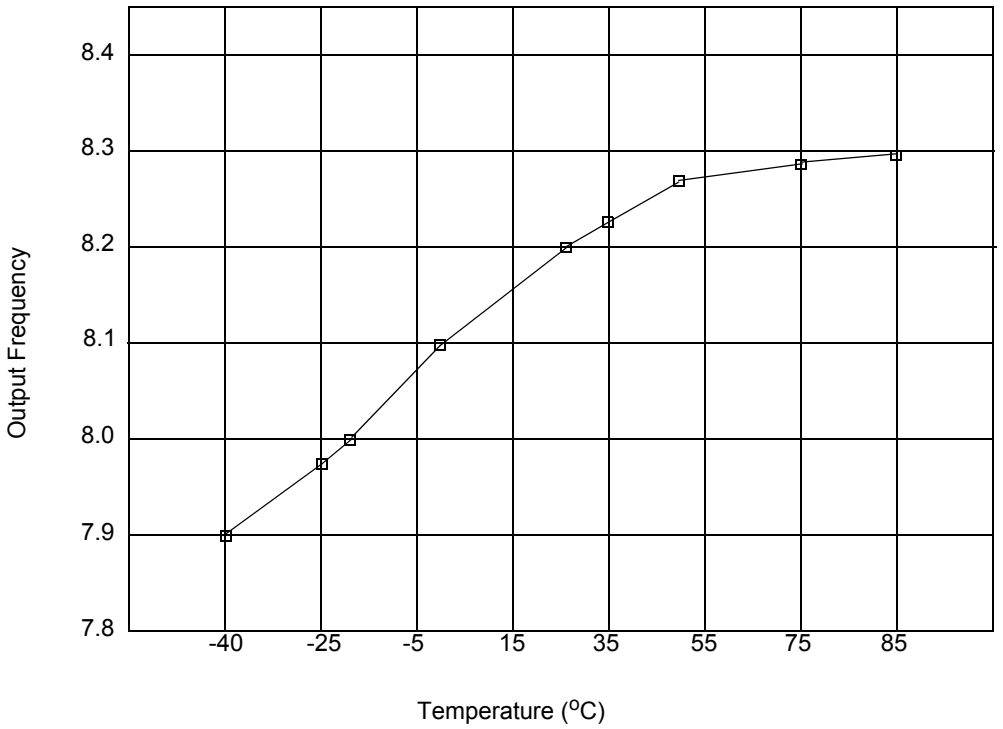


Figure 3-7 Typical Relaxation Oscillator Frequency vs. Temperature (Trimmed to 8MHz @ 25°C)

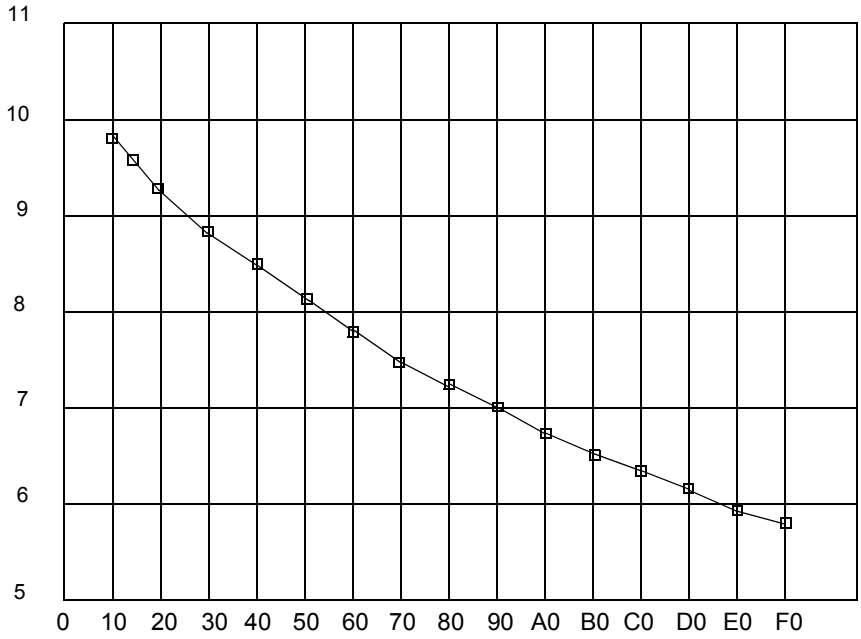


Figure 3-8 Typical Relaxation Oscillator Frequency vs. Trim Value @ 25°C

3.5.2 Phase Locked Loop Timing

Table 3-9 PLL Timing

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency for the PLL[1]	f_{osc}	4	8	10	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	80[3]	MHz
PLL stabilization time[4] 0° to +85°C	t_{plls}	—	10	—	ms
PLL stabilization time[4] -40° to 0°C	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. Will not exceed 60MHz for the DSP56F802TA60 device.
4. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

3.8 Serial Communication Interface (SCI) Timing

Table 3-12 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

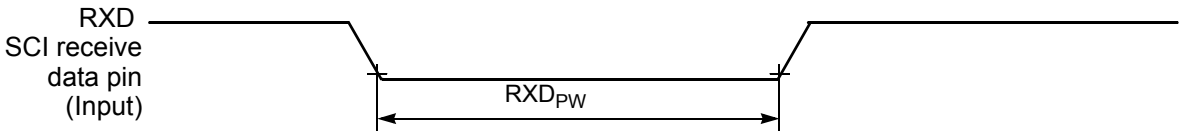


Figure 3-11 RXD Pulse Width

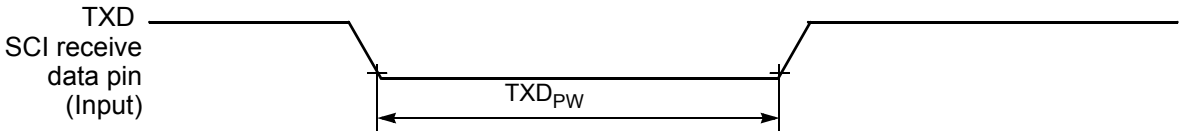


Figure 3-12 TXD Pulse Width

3.9 Analog-to-Digital Converter (ADC) Characteristics

Table 3-13 ADC Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/- 4	+/- 5	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[3]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Power-up time	t_{ADPU}	—	2.5	—	msec
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	1.00	1.10	1.15	—
Offset Voltage[5]	V_{OFFSET}	+10	+230	+325	mV
Total Harmonic Distortion[5]	THD	55	60	—	dB
Signal-to-Noise plus Distortion[5]	SINAD	54	56	—	—
Effective Number of Bits[5]	ENOB	8.5	9.5	—	bit
Spurious Free Dynamic Range[5]	SFDR	60	65	—	dB
Spurious Free Dynamic Range	SFDR	65	70	—	dB
ADC Quiescent Current (both ADCs)	I_{ADC}	—	50	—	mA
V_{REF} Quiescent Current (both ADCs)	I_{VREF}	—	12	16.5	mA

1. For optimum ADC performance, keep the minimum V_{ADCIN} value $\geq$ 250mV. Inputs less than 250mV volts may convert to a digital output code of 0 or cause erroneous conversions.
2. V_{REF} must be equal to or less than V_{DDA} - 0.3V and must be greater than 2.7V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
6. $t_{AIC} = 1/f_{ADIC}$

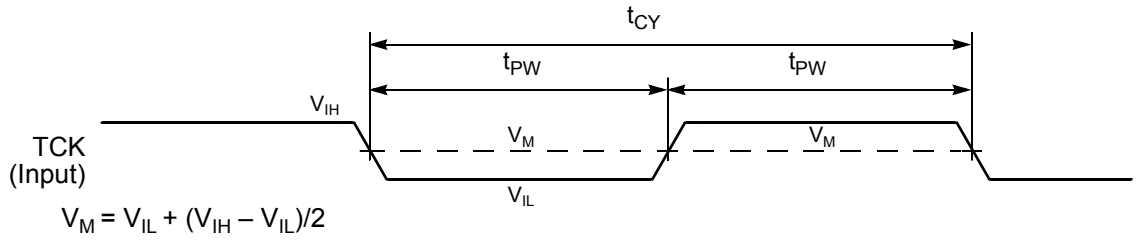


Figure 3-14 Test Clock Input Timing Diagram

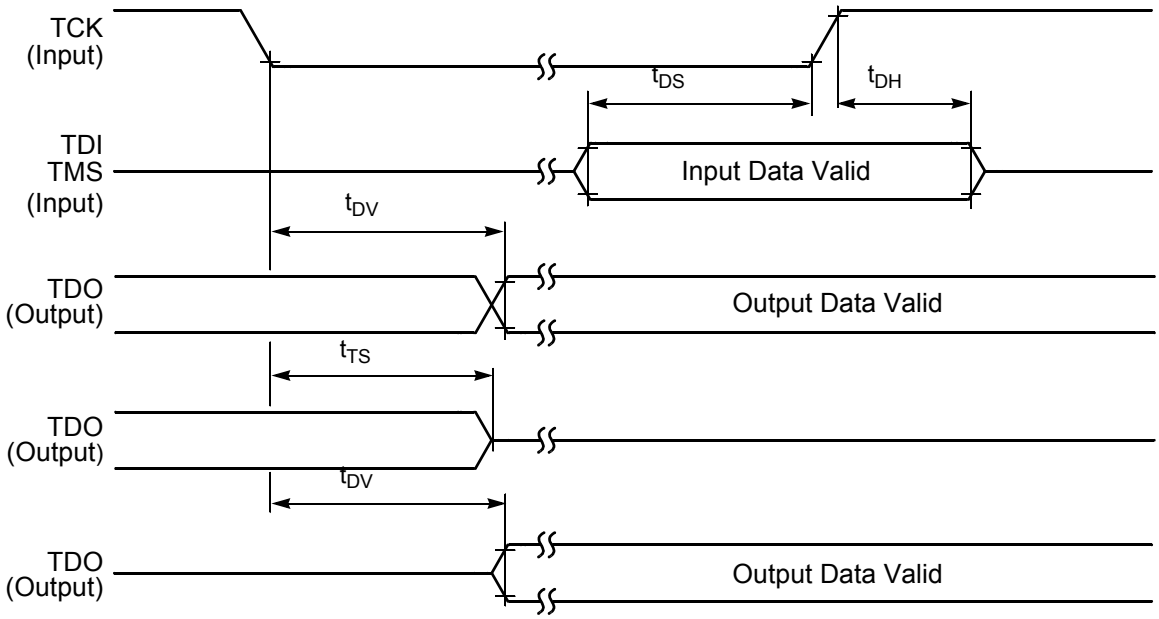


Figure 3-15 Test Access Port Timing Diagram

Figure 3-16 $\overline{\text{TRST}}$ Timing Diagram

Part 4 Packaging

4.1 Package and Pin-Out Information 56F802

This section contains package and pin-out information for the 32-pin LQFP configuration of the 56F802.

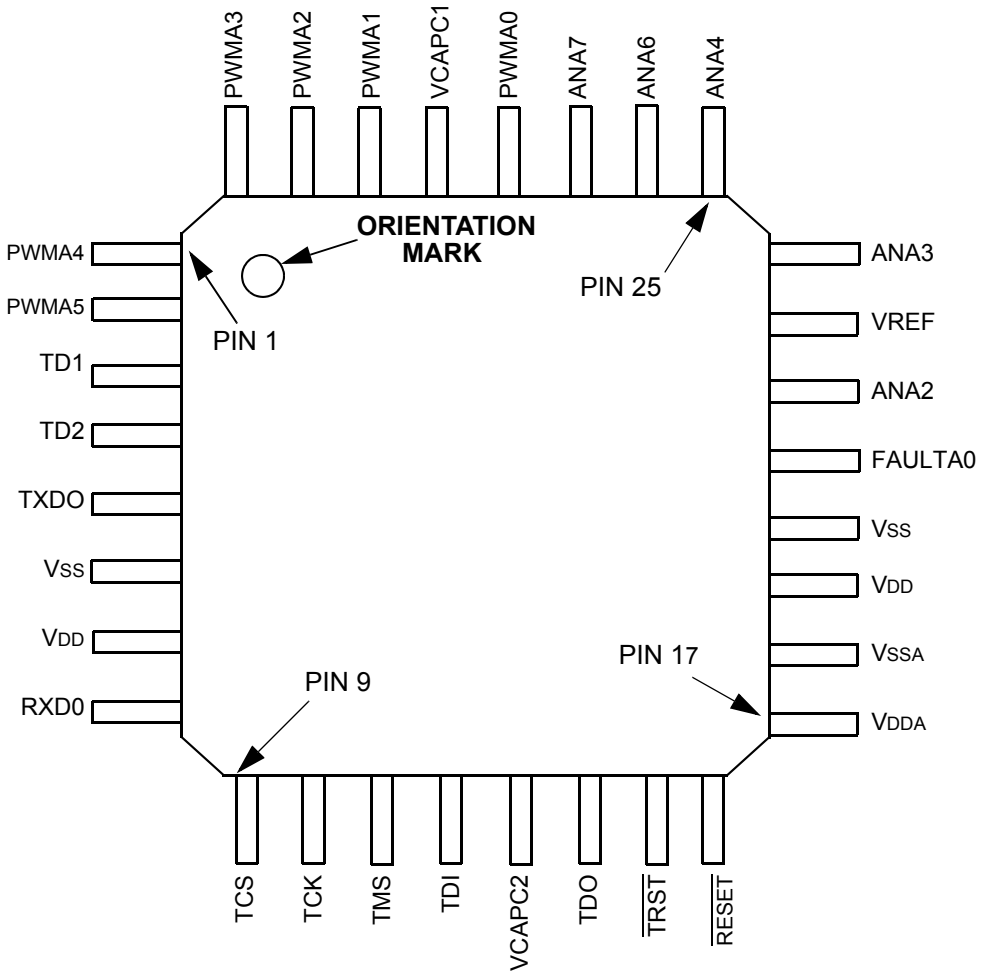
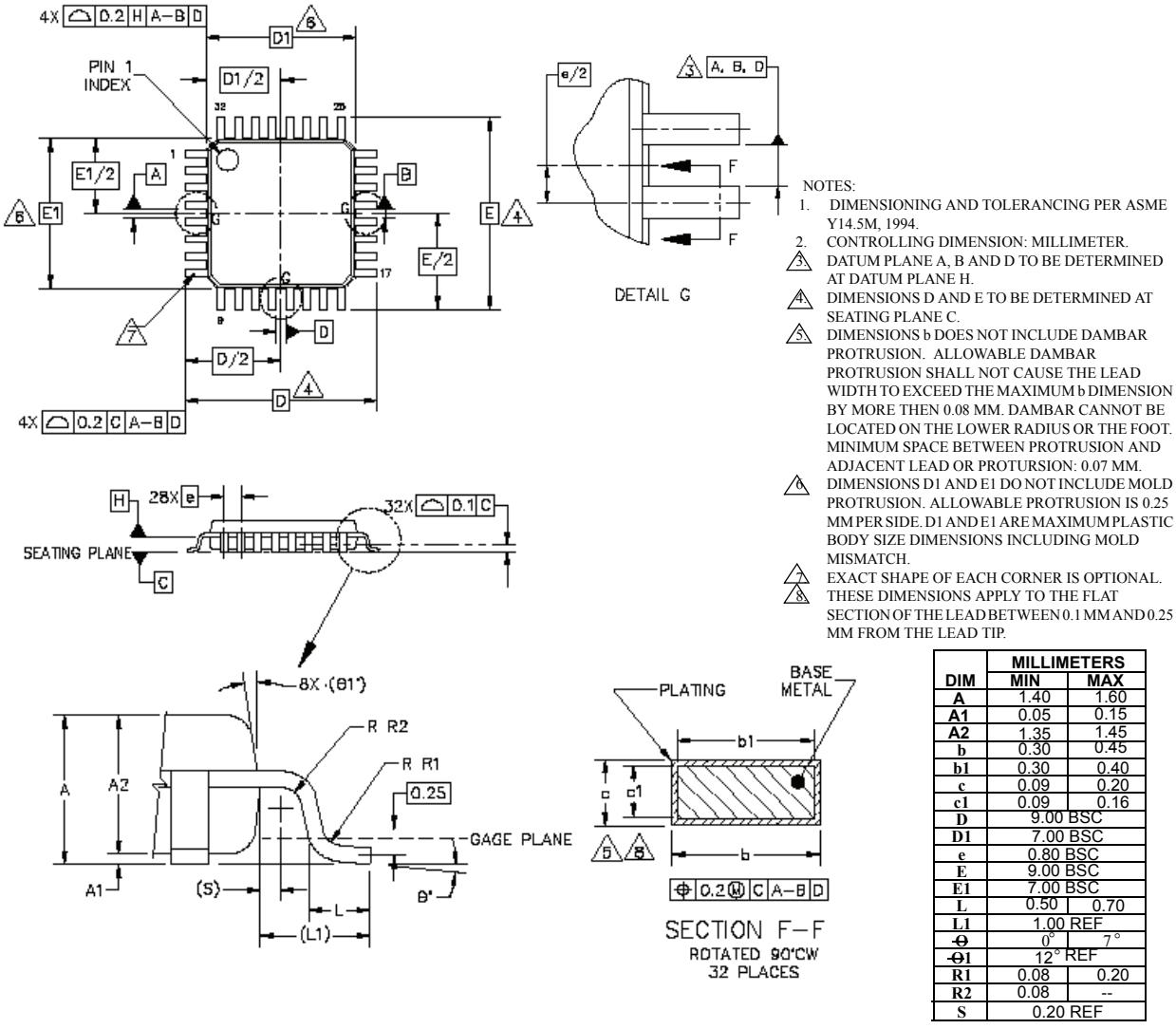


Figure 4-1 Top View, 56F802 32-pin LQFP Package

Table 4-1 56F802 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	PWMA4	9	TCS	17	V_{DDA}	25	ANA4
2	PWMA5	10	TCK	18	V_{SSA}	26	ANA6
3	TD1	11	TMS	19	V_{DD}	27	ANA7
4	TD2	12	TDI	20	V_{SS}	28	PWMA0
5	TXDO	13	VCAPC2	21	FAULTA0	29	VCAPC1
6	V_{SS}	14	TDO	22	ANA2	30	PWMA1
7	V_{DD}	15	$\overline{\text{TRST}}$	23	VREF	31	PWMA2
8	RXD0	16	$\overline{\text{RESET}}$	24	ANA3	32	PWMA3



DIM	MILLIMETERS MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
θ	0°	7°
θ1	12° REF	
R1	0.08	0.20
R2	0.08	--
S	0.20 REF	

Figure 4-2 32-pin LQFP Mechanical Information (Case 873A)

Please see **www.freescale.com** for the most current case outline.

- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.

- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 μF, preferably with ceramic or tantalum capacitors which tend to provide better performance tolerances.
- Because the controller's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.