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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Obsolete
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3188tax

Table 1. Device summary

Reference	Part number
STM8AL318x	STM8AL3188, STM8AL3189, STM8AL318A
STM8AL3L8x	STM8AL3L88, STM8AL3L89, STM8AL3L8A

Contents

STM8AL ultra-low-power microcontrollers operates either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8AL ultra-low-power microcontroller families suitable for a wide range of applications.

The devices are offered in three different packages from 48 to 80 pins. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8AL ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the high-density STM8AL3x8x families.

DAC: Digital-to-analog converter
I²C: Inter-integrated circuit multimaster interface
IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The high-density STM8AL3x8x devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset is used to exit the microcontroller from Wait mode (WFE or WFI mode).

- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and exits from this mode by software or by a reset.
  All interrupts must be masked and are not used to exit the microcontroller from this mode.

- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked and arenot used to exit the microcontroller from this mode.

- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup is triggered by RTC interrupts, external interrupts or reset.

- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 μs.

3.12   System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence.

3.13   Timers

The high-density STM8AL3x8x devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers are served by DMA1.

Table 3 compares the features of the advanced control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM1			Any integer from 1 to 65536		3 + 1	3
TIM2	16-bit	up/down	Any power of 2 from 1 to 128	Yes	2	None
TIM3						
TIM5						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.13.1   16-bit advanced control timer (TIM1)

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler

- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output

- 1 additional capture/compare channel which is not connected to an external I/O

- Synchronization module to control the timer with external signals

- Break input to force timer outputs into a defined state

- 3 complementary outputs with adjustable dead time

- Encoder mode

- Interrupt capability on various events (capture, compare, overflow, break, trigger)

3.13.2 16-bit general purpose timers (TIM2, TIM3, TIM5)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.13.3 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. This timer is used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

3.14 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.14.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.14.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) is used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.17 Infrared (IR) interface

The high-density STM8AL3x8x devices contain an infrared interface which is used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.18 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface is activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation is also monitored in real-time by means of shadow registers.

Bootloader

A bootloader is available to reprogram the Flash memory using the USART1, USART2, USART3 (USARTs in asynchronous mode), SPI1 or SPI2 interfaces.

Table 5. High-density STM8AL3x8x pin description (continued)

LQFP80	LQFP64	LQFP48	Pin name	Type	I/O level	Input floating	Input wpu	Input Ext. interrupt	Output High sink/source	Output OD	Output PP	Main function (after reset)	Default alternate function
5	1	1	PA0[8]/*[USART1_CK]*[2]/ SWIM/BEEP/IR_TIM [9]	I/O	-	X	**X**	X	HS	X	X	**Port A0**	*[USART1 synchronous clock]*[2] / SWIM input and output / Beep output / Infrared Timer output
68	56	40	V_{SS2}	S	-	-	-	-	-	-	-	IOs ground voltage
67	55	39	V_{DD2}	S	-	-	-	-	-	-	-	IOs supply voltage
48	-	-	V_{SS4}	S	-	-	-	-	-	-	-	IOs ground voltage
47	-	-	V_{DD4}	S	-	-	-	-	-	-	-	IOs supply voltage

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

3. Available onSTM8AL3L8xdevices only.

4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.

5. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.

6. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).

7. Available on STM8AL3L8x devices only. On STM8AL318x devices it is reserved and must be tied to V_{DD}.

8. The PA0 pin is in input pull-up during the reset phase and after reset release.

9. High Sink LED driver capability available on PA0.

Note: *The slope control of all GPIO pins, except true open drain pins, are programmable. By default the slope control is limited to 2 MHz.*

System configuration options

As shown in *Table 5: High-density STM8AL3x8x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU[1]	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x00
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x03
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CCR	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 byte)			
0x00 7F60	CPU	CFG_GCR	Global configuration register	0x00
0x00 7F70	ITC-SPR	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF
0x00 7F78 to 0x00 7F79	Reserved area (2 byte)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 byte)			

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 19. General operating conditions

| Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}[1]	System clock frequency	1.65 V $\leq V_{DD}$ < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector enabled		1.65[2]	3.6	V
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65[2]	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D[3]	Power dissipation at T_A= 85 °C for suffix A devices	LQFP80	-	-	288	mW
		LQFP64	-	-	288	
		LQFP48	-	-	288	
	Power dissipation at T_A= 125 °C for suffix C devices	LQFP80	-	-	131	
		LQFP64	-	-	104	
		LQFP48	-	-	77	
T_A	Temperature range	1.65 V $\leq V_{DD}$ < 3.6 V (A suffix version)	-	-40	85	°C
		1.65 V $\leq V_{DD}$ < 3.6 V (C suffix version)	-	-40	125	
T_J	Junction temperature range	-40 °C $\leq T_A$ < 85 °C (A suffix version)		-40	105	
		-40 °C$\leq T_A$ < 125 °C (C suffix version)		-40	130	

1. f_{SYSCLK} = f_{CPU}

2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled.

3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} -T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in "Thermal characteristics" table.

1. CPU executing typical data processing

2. The run from RAM consumption is approximated with the linear formula:
    I_{DD}(run_from_RAM) = Freq. * 95 µA/MHz + 250 µA

3. Guaranteed by characterization results.

4. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.

5. The run from Flash consumption is approximated with the linear formula:
    I_{DD}(run_from_Flash) = Freq. * 200 µA/MHz + 330 µA

6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*.

Figure 13. Typical $I_{DD(RUN)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} =16 MHz[1]
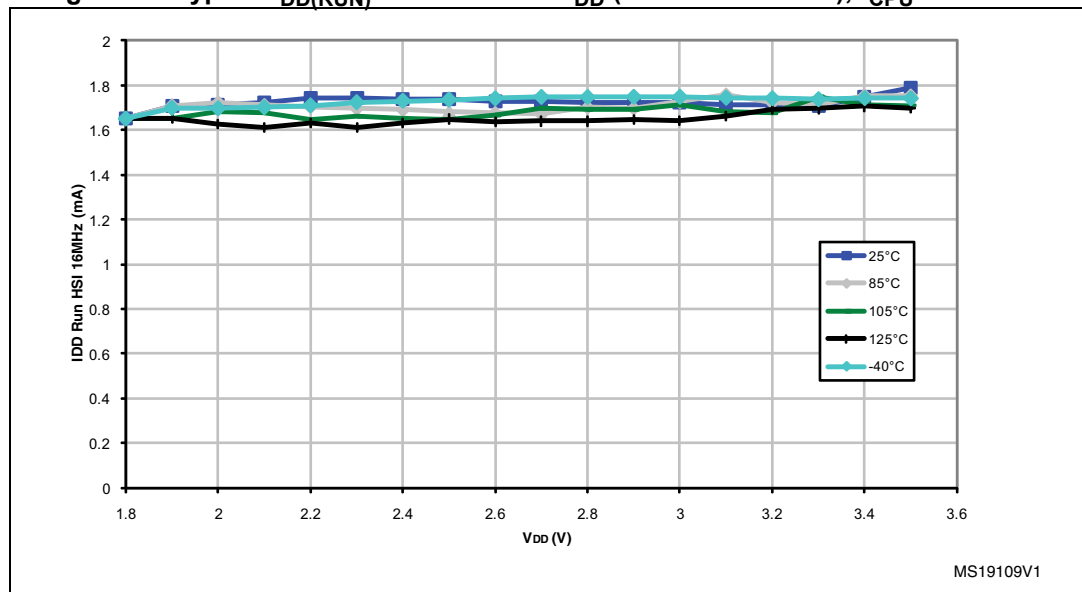

1. Typical current consumption measured with code executed from RAM.

In the following table, data are based on characterization results, unless otherwise specified.

Table 25. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions[1]			Typ.	Max.[2]	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC (at 38 kHz)	LCD OFF[3]	T_A = -40 °C to 25 °C	0.90	2.10	µA
				T_A = 85 °C	1.50	3.40	
				T_A = 125 °C	5.10	12.00	
			LCD ON (static duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.40	3.10	
				T_A = 85 °C	1.90	4.30	
				T_A = 125 °C	5.50	13.00	
			LCD ON (1/4 duty/ external V_{LCD}) [5]	T_A = -40 °C to 25 °C	1.90	4.30	
				T_A = 85 °C	2.40	5.40	
				T_A = 125 °C	6.00	15.00	
			LCD ON (1/4 duty/ internal V_{LCD}) [6]	T_A = -40 °C to 25 °C	3.90	8.75	
				T_A = 85 °C	4.50	10.20	
				T_A = 125 °C	6.80	16.30	
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) [7]	LCD OFF[8]	T_A = -40 °C to 25 °C	0.50	1.20	µA
				T_A = 85 °C	0.90	2.10	
				T_A = 125 °C	4.80	11.00	
			LCD ON (static duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	0.85	1.90	
				T_A = 85 °C	1.30	3.20	
				T_A = 125 °C	5.00	12.00	
			LCD ON (1/4 duty/ external V_{LCD}) [5]	T_A = -40 °C to 25 °C	1.50	2.50	
				T_A = 85 °C	1.80	4.20	
				T_A = 125 °C	5.70	14.00	
			LCD ON (1/4 duty/ internal V_{LCD}) [6]	T_A = -40 °C to 25 °C	3.40	7.60	
				T_A = 85 °C	3.90	9.20	
				T_A = 125 °C	6.30	15.20	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.40	-	mA

Figure 36. Typical NRST pull-up current I_{pu} vs. V_{DD}
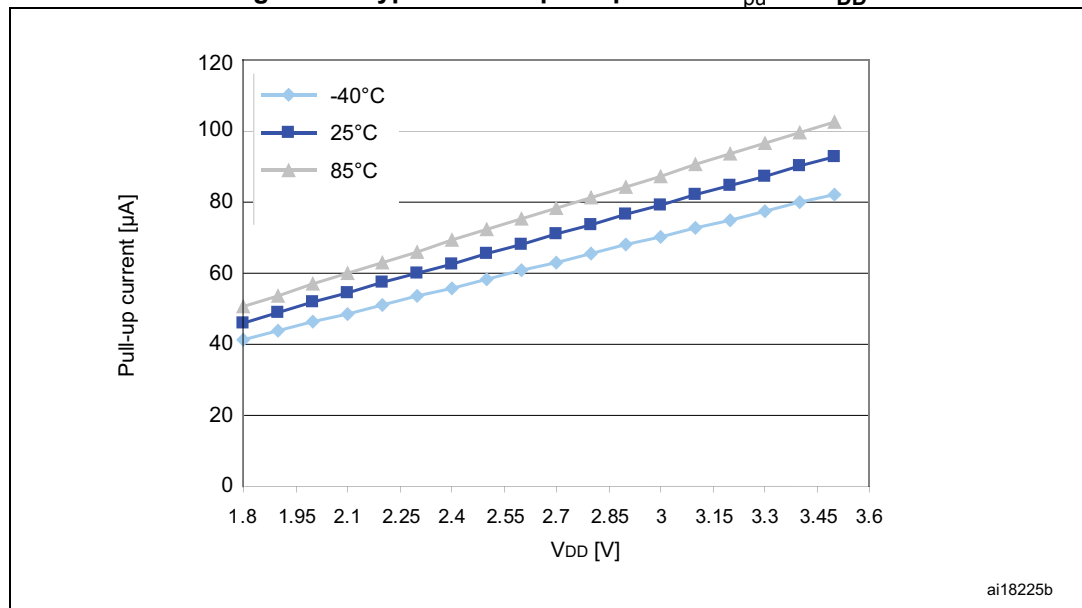
The reset network shown in *Figure 37* protects the device against parasitic resets. The user must ensure that the level on the NRST pin goes below the V_{IL} max. level specified in *Table 45*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor has to be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

**Figure 37. Recommended NRST pin configuration**
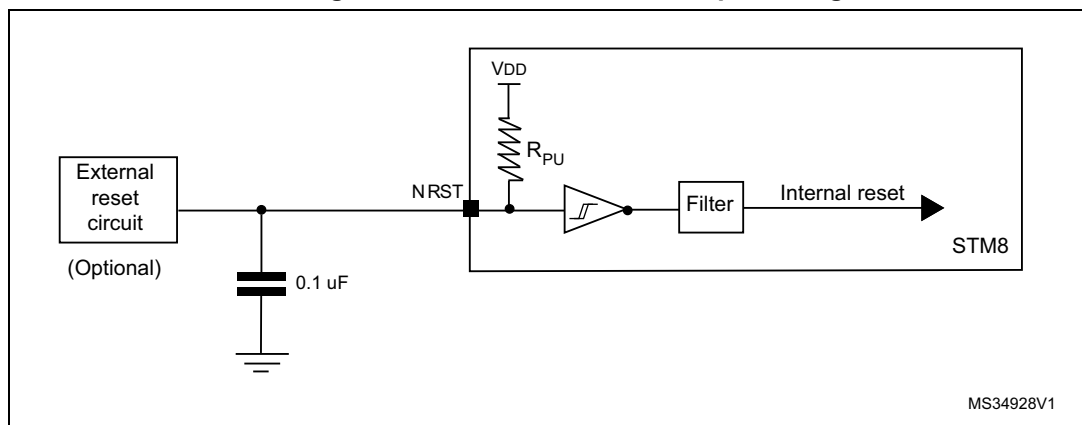
In the following table, data are guaranteed by design, not tested in production, unless otherwise specified.

Table 52. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	μs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay[2] in slow mode	1.65 V $\leq V_{DDA} \leq$ 2.7 V	-	1.8	3.5	
		2.7 V $\leq V_{DDA} \leq$ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay[2] in fast mode	1.65 V $\leq V_{DDA} \leq$ 2.7 V	-	0.8	2	
		2.7 V $\leq V_{DDA} \leq$ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
$d_{Threshold}/dt$	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REF+}, 3/4 V_{REF+}, 1/2 V_{REF+}, 1/4 V_{REF+}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption[3]	Fast mode	-	3.5	5	μA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint
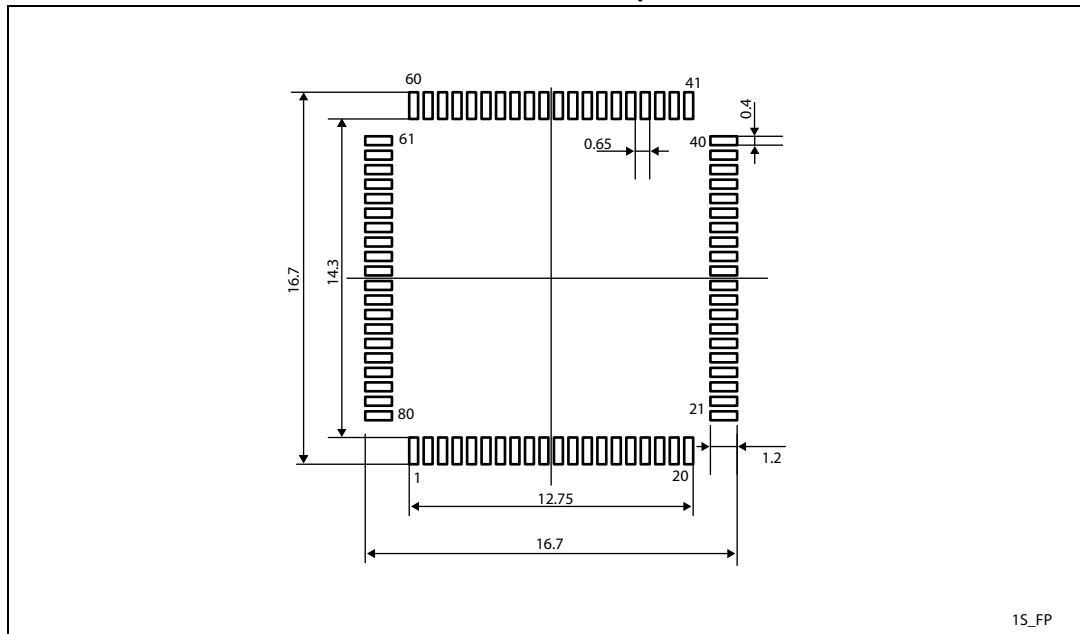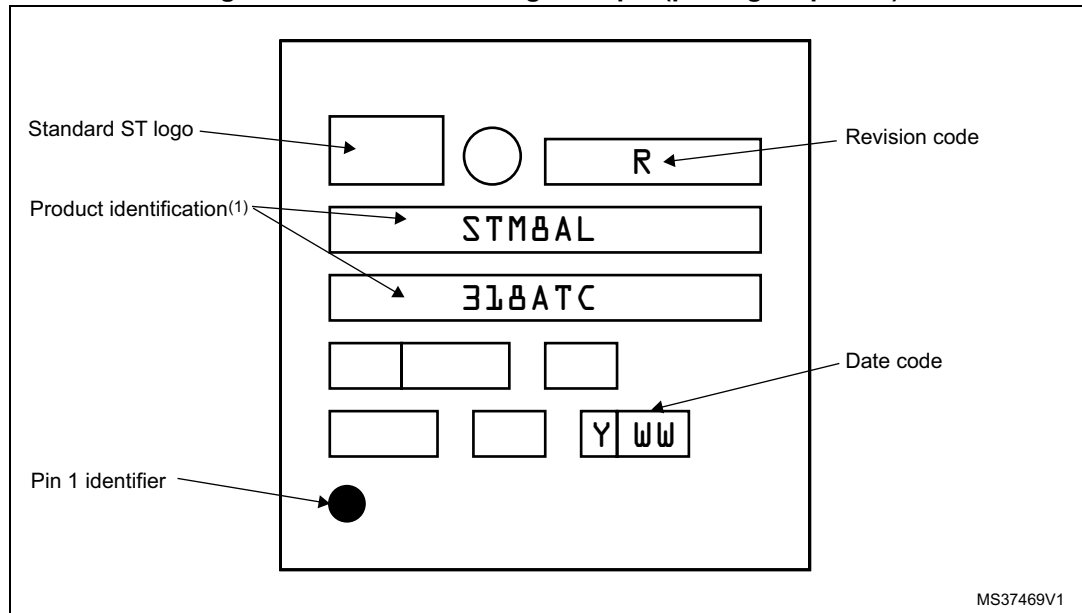

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

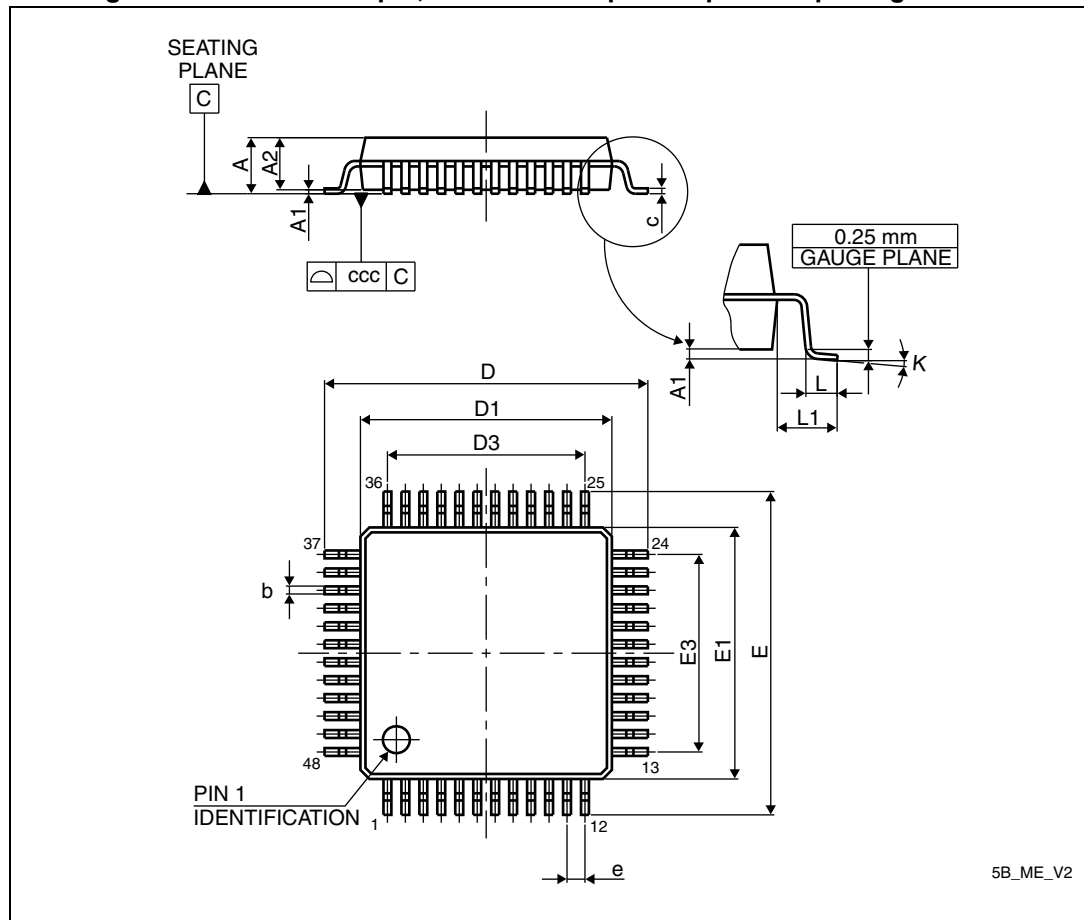**Figure 48. LQFP80 marking example (package top view)**

1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

**Table 66. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat
package mechanical data (continued)**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 50. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package
recommended footprint**

1. Dimensions are expressed in millimeters.

10.3 LQFP48 package information

Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline
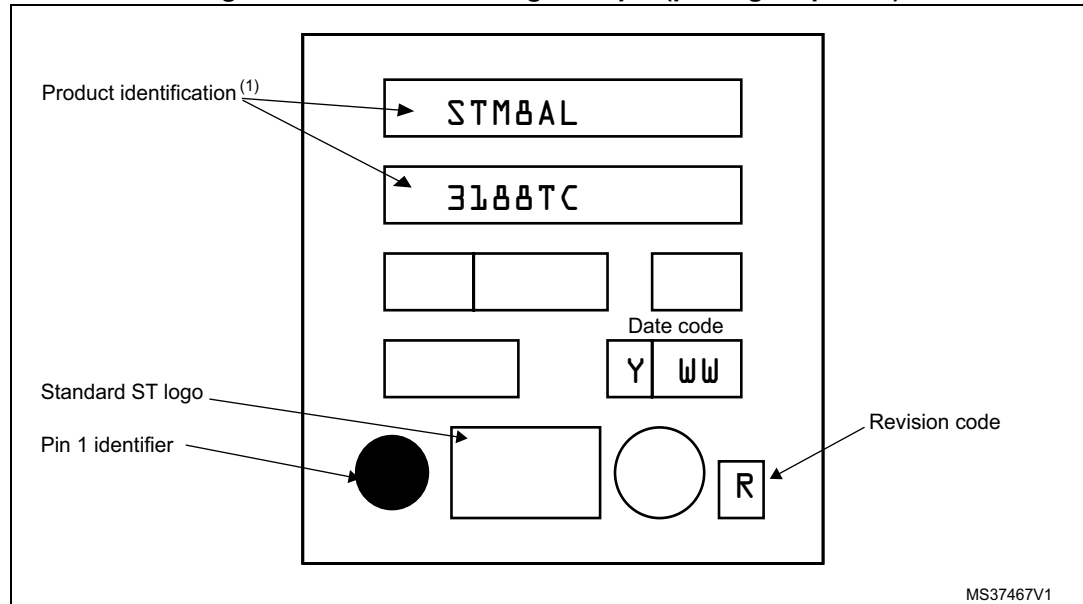

1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 54. LQFP48 marking example (package top view)

1. Parts marked as "ES","E" or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.