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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3188tay

2 Description

The high-density STM8AL3x8x ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density STM8AL3x8x microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, 8x40 or 4x44-segment LCD, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. One 8x40 or 4x44-segment LCD is available on the STM8AL3L8x devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

2.1 STM8AL ultra-low-power 8-bit family benefits

High-density STM8AL3x8x devices are part of the STM8AL automotive ultra-low-power 8-bit family providing the following benefits:

- Integrated system
  - 64 Kbytes of high-density embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - 4 Kbytes of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- Ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8AL3L8x devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. This LCD is configurable to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels programmable to blink.
- The LCD controller operating in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8AL3x8x devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option byte.

The memory supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
45	37	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ ADC1_IN12/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/Comparator 1 positive input
-	-	30	PB6/SPI1_MOSI/ LCD_SEG16(3)/ ADC1_IN12/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/Comparator 1 positive input
46	38	31	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/Comparator 1 positive input
65	53	37	PC0/I2C1_SDA	I/O	FT(5)	**X**		X		T(6)	-	**Port C0**	I2C1 data
66	54	38	PC1/I2C1_SCL	I/O	FT(5)	**X**		X		T(6)	-	**Port C1**	I2C1 clock
69	57	41	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/Comparator 1 positive input/Internal reference voltage output
-	-	42	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5
70	58	-	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5/COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 2 negative input /Comparator 1 input positive
71	59	43	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(3)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input
72	60	44	PC5/OSC32_IN /*[SPI1_NSS]*(2)/ *[USART1_TX]*(2)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50CA	CLK	CLK_CSSR	Clock security system register	0x00
0x00 50CB		CLK_CBEEPR	Clock BEEP register	0x00
0x00 50CC		CLK_HSICALR	HSI calibration register	0xXX
0x00 50CD		CLK_HSITRIMR	HSI clock calibration trimming register	0x00
0x00 50CE		CLK_HSIUNLCKR	HSI unlock register	0x00
0x00 50CF		CLK_REGCSR	Main regulator control status register	0bxx11 100X
0x00 50D0		CLK_PCKENR3	Peripheral clock gating register 3	0x00
0x00 50D1 to 0x00 50D2	Reserved area (2 byte)			
0x00 50D3	WWDG	WWDG_CR	WWDG control register	0x7F
0x00 50D4		WWDG_WR	WWDR window register	0x7F
0x00 50D5 to 00 50DF	Reserved area (11 byte)			
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 byte)			
0x00 50F0	BEEP	BEEP_CSR1	BEEP control/status register 1	0x00
0x00 50F1 0x00 50F2		Reserved area (2 byte)		
0x00 50F3		BEEP_CSR2	BEEP control/status register 2	0x1F
0x00 50F4 to0x00 513F	Reserved area (76 byte)			
0x00 5140	RTC	RTC_TR1	Time register 1	0x00
0x00 5141		RTC_TR2	Time register 2	0x00
0x00 5142		RTC_TR3	Time register 3	0x00
0x00 5143	Reserved area (1 byte)			
0x00 5144	RTC	RTC_DR1	Date register 1	0x01
0x00 5145		RTC_DR2	Date register 2	0x21
0x00 5146		RTC_DR3	Date register 3	0x00
0x00 5147	Reserved area (1 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5386 to 0x00 5387	Reserved area (2 byte)			
0x00 5388	DAC	DAC_CH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 5389		DAC_CH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 538A to 0x00 538B	Reserved area (2 byte)			
0x00 538C	DAC	DAC_CH1LDHRH	DAC channel 1 left aligned data holding register high	0x00
0x00 538D		DAC_CH1LDHRL	DAC channel 1 left aligned data holding register low	0x00
0x00 538E to 0x00 538F	Reserved area (2 byte)			
0x00 5390	DAC	DAC_CH1DHR8	DAC channel 1 8-bit data holding register	0x00
0x00 5391 to 0x00 5393	Reserved area (3 byte)			
0x00 5394	DAC	DAC_CH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 5395		DAC_CH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 5396 to 0x00 5397	Reserved area (2 byte)			
0x00 5398	DAC	DAC_CH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 5399		DAC_CH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 539A to 0x00 539B	Reserved area (2 byte)			
0x00 539C	DAC	DAC_CH2DHR8	DAC channel 2 8-bit data holding register	0x00
0x00 539D to 0x00 539F	Reserved area (3 byte)			
0x00 53A0	DAC	DAC_DCH1RDHRH	DAC channel 1 right aligned data holding register high	0x00
0x00 53A1		DAC_DCH1RDHRL	DAC channel 1 right aligned data holding register low	0x00
0x00 53A2 to 0x00 53AB	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53AC	DAC	DAC_DORH	DAC data output register high	0x00
0x00 53AD		DAC_DORL	DAC data output register low	0x00
0x00 53A2		DAC_DCH2RDHRH	DAC channel 2 right aligned data holding register high	0x00
0x00 53A3		DAC_DCH2RDHRL	DAC channel 2 right aligned data holding register low	0x00
0x00 53A4		DAC_DCH1LDHRH	DAC channel 1left aligned data holding register high	0x00
0x00 53A5		DAC_DCH1LDHRL	DAC channel 1left aligned data holding register low	0x00
0x00 53A6		DAC_DCH2LDHRH	DAC channel 2 left aligned data holding register high	0x00
0x00 53A7		DAC_DCH2LDHRL	DAC channel 2 left aligned data holding register low	0x00
0x00 53A8		DAC_DCH1DHR8	DAC channel 1 8-bit mode data holding register	0x00
0x00 53A9		DAC_DCH2DHR8	DAC channel 2 8-bit mode data holding register	0x00
0x00 53AA to 0x00 53AB	Reserved area (2 byte)			
0x00 53AC	DAC	DAC_CH1DORH Reset value	DAC channel 1 data output register high	0x00
0x00 53AD		DAC_CH1DORL Reset value	DAC channel 1 data output register low	0x00
0x00 53AE to 0x00 53AF	Reserved area (2 byte)			
0x00 53B0	DAC	DAC_CH2DORH Reset value	DAC channel 2 data output register high	0x00
0x00 53B1		DAC_CH2DORL Reset value	DAC channel 2 data output register low	0x00
0x00 53B2 to 0x00 53BF	Reserved area			
0x00 53C0	SPI2	SPI2_CR1	SPI2 control register 1	0x00
0x00 53C1		SPI2_CR2	SPI2 control register 2	0x00
0x00 53C2		SPI2_ICR	SPI2 interrupt control register	0x00
0x00 53C3		SPI2_SR	SPI2 status register	0x02
0x00 53C4		SPI2_DR	SPI2 data register	0x00
0x00 53C5		SPI2_CRCPR	SPI2 CRC polynomial register	0x07
0x00 53C6		SPI2_RXCRCR	SPI2 Rx CRC register	0x00
0x00 53C7		SPI2_TXCRCR	SPI2 Tx CRC register	0x00

9.3.2 Embedded reset and power control block characteristics

Table 20. Embedded reset and power control block characteristics

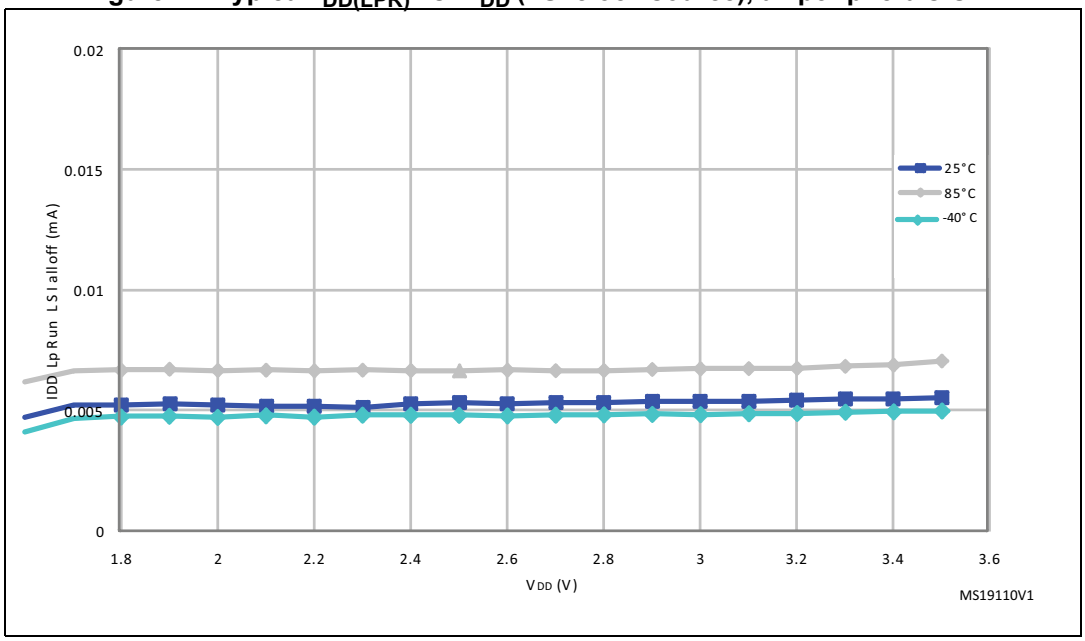
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
V_{PDR}	Power-down reset threshold	Falling edge	1.3	1.5	1.65(2)	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.7	1.74(2)	
		Rising edge	1.69(2)	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97(2)	
		Rising edge	1.96(2)	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35(2)	
		Rising edge	2.31(2)	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60(2)	
		Rising edge	2.54(2)	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85(2)	
		Rising edge	2.78(2)	2.90	2.95	
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88(2)	V
		Rising edge	1.88(2)	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09(2)	
		Rising edge	2.08(2)	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28(2)	
		Rising edge	2.28(2)	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48(2)	
		Rising edge	2.47(2)	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69(2)	
		Rising edge	2.68(2)	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88(2)	
		Rising edge	2.87(2)	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09(2)	
		Rising edge	3.08(2)	3.15	3.20	

Table 23. Total current consumption and timing in low-power run mode at V_{DD} = 1.65 V to 3.6 V

Symbol	Parameter	Conditions(1)			Typ.	Max.	Unit
$I_{DD(LPR)}$	Supply current in low-power run mode	LSI RC osc. (at 38 kHz)	all peripherals OFF	T_A = -40 °C to 25 °C	5.10	6.50(2)	µA
				T_A = 85 °C	6.80	11.00(3)	
				T_A = 125 °C	13.40	20.00(3)	
		LSE (4) external clock (32.768 kHz)		T_A = -40 °C to 25 °C	5.25	5.60(2)	
				T_A = 85 °C	5.85	6.30(2)	
				T_A = 125 °C	14.00	16.50(2)	

1. No floating I/Os
2. Guaranteed by characterization results.
3. Tested at 85°C for temperature range A or 125°C for temperature range C.
4. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 33*

Figure 17. Typical $I_{DD(LPR)}$ vs. V_{DD} (LSI clock source), all peripherals OFF



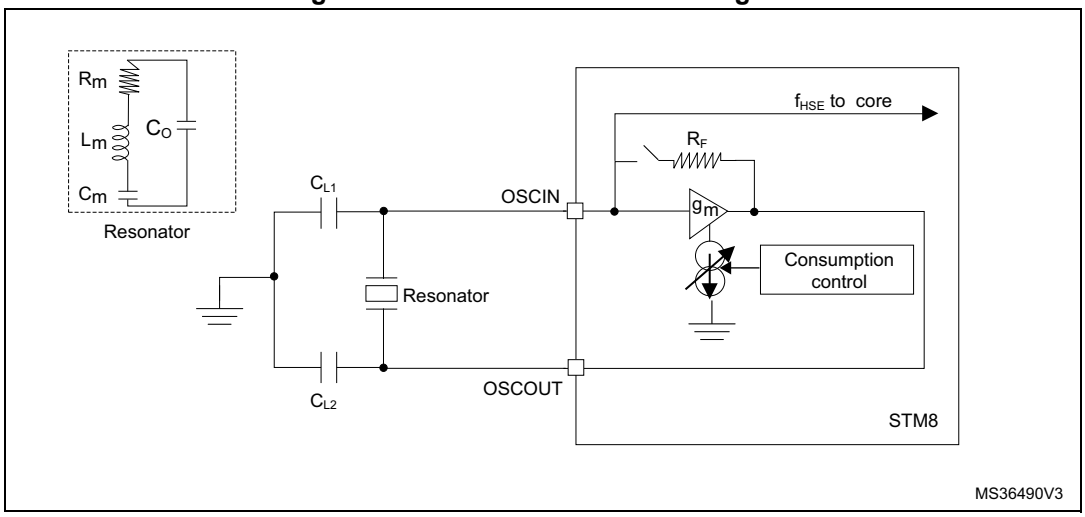
Current consumption of on-chip peripherals

Table 28. Peripheral current consumption

Symbol	Parameter		Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM1)}$	TIM1 supply current(1)		10	µA/MHz
$I_{DD(TIM2)}$	TIM2 supply current (1)		7	
$I_{DD(TIM3)}$	TIM3 supply current (1)		7	
$I_{DD(TIM5)}$	TIM5 supply current (1)		7	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)		3	
$I_{DD(USART1)}$	USART1 supply current (2)		5	
$I_{DD(USART2)}$	USART2 supply current (2)		5	
$I_{DD(USART3)}$	USART3 supply current (2)		5	
$I_{DD(SPI1)}$	SPI1 supply current (2)		3	
$I_{DD(SPI2)}$	SPI2 supply current (2)		3	
$I_{DD(I2C1)}$	I^2C1 supply current (2)		4	
$I_{DD(DMA1)}$	DMA1 supply current(2)		3	
$I_{DD(WWDG)}$	WWDG supply current(2)		1	
$I_{DD(ALL)}$	Peripherals ON(3)		63	
$I_{DD(ADC1)}$	ADC1 supply current(4)		1500	µA
$I_{DD(DAC)}$	DAC supply current(5)		370	
$I_{DD(COMP1)}$	Comparator 1 supply current(6)		0.160	
$I_{DD(COMP2)}$	Comparator 2 supply current(6)	Slow mode	2	
		Fast mode	5	
$I_{DD(PVD/BOR)}$	Power voltage detector and brownout Reset unit supply current (7)		2.6	
$I_{DD(BOR)}$	Brownout Reset unit supply current (7)		2.4	
$I_{DD(IDWDG)}$	Independent watchdog supply current	including LSI supply current	0.45	
		excluding LSI supply current	0.05	

1. Data based on a differential I_{DD} measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion.

Figure 21. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification), C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), C_{L1}=C_{L2}=C: Grounded external capacitance

$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE is available on STM8AL318x devices only.

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 40. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins	-5	+0	mA
	Injected current on all 5 V tolerant (FT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

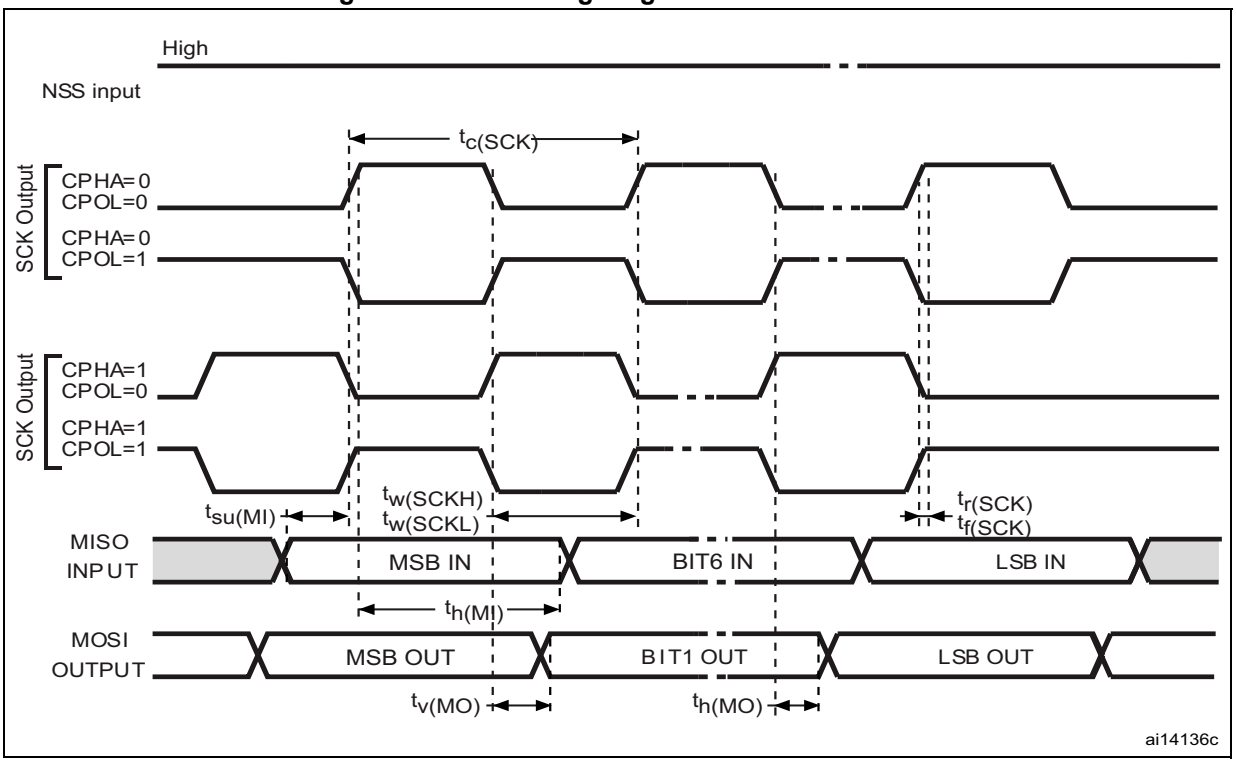
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 41. I/O static characteristics

Symbol	Parameter	Conditions[1]	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level voltage	Input voltage on all pins	Vss-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high-level voltage	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2[2]	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5[2]	
		Input voltage on five-volt tolerant (FT) pins with V_{DD} < 2 V		-	5.2[2]	
		Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V		-	5.5[2]	
		Input voltage on any other pin		-	V_{DD}+0.3[2]	
V_{hys}	Schmitt trigger voltage hysteresis [3]	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current [4]	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200	
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN}=V_{SS}$	30[6]	45	60[6]	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

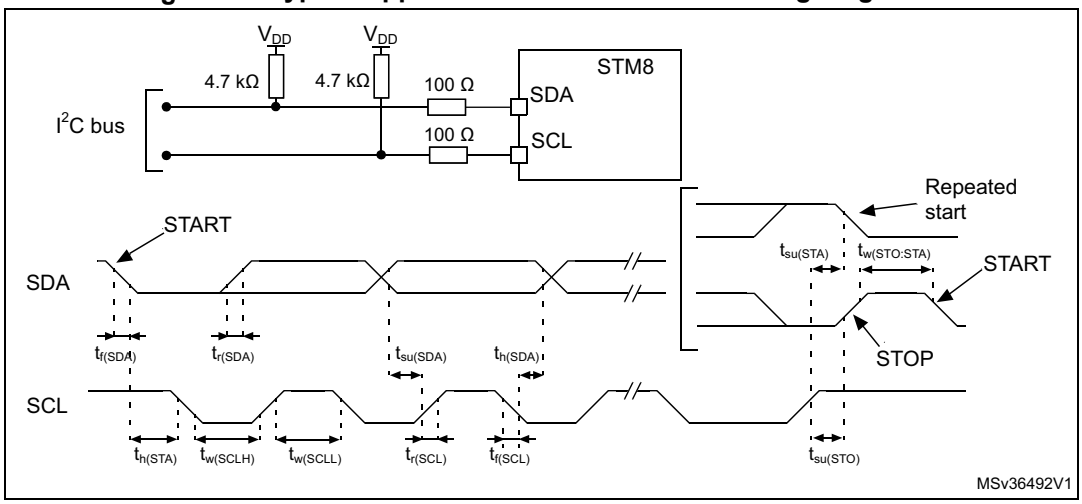
1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. If V_{IH} maximum is not respected, the injection current must be limited externally to $I_{INJ(PIN)}$ maximum.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 28*).
6. Guaranteed by characterization results.

Figure 40. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 41. Typical application with I²C bus and timing diagram(1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}

Table 56. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12000000 / f_{ADC} + t_S			
		16 MHz	1(3)	-	-	
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 49*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. In the RM0031, t_{IDLE} defines the time between 2 conversions, or between ADC ON and the first conversion. t_{IDLE} is not relevant for this device.

Static latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 63. Electrical sensitivities

Symbol	Parameter	Conditions	Class (1)
LU	Static latch-up class	T_A = 125 °C	A

1. Class description: the class is an STMicroelectronics internal specification. The class limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 19: General operating conditions on page 68*.

The maximum chip-junction temperature, T_{Jmax}, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high-level in the application.

Table 64. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm	65	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 64- 10 x 10 mm	48	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 80- 14 x 14 mm	38	°C/W

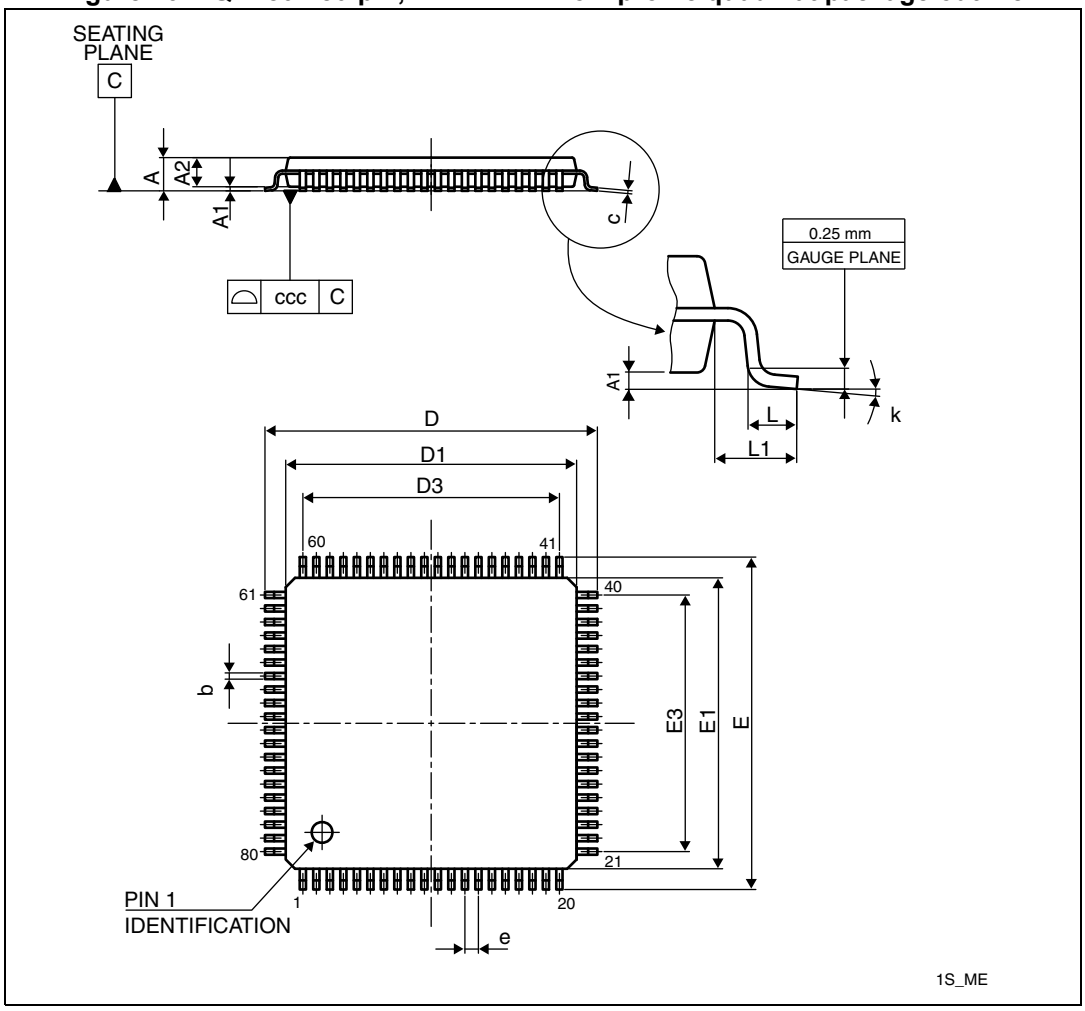
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 LQFP80 package information

Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
03-Feb-2015	1	Initial release.
22-Apr-2015	2	Added: – *Figure 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, – *Figure 48: LQFP80 marking example (package top view)*, – *Figure 51: LQFP64 marking example (package top view)*, – *Figure 54: LQFP48 marking example (package top view)*. Corrected OPT0 default value in *Table 12: Option byte addresses*.
27-Jul-2015	3	Updated – the document confidentiality level to “Public”, – *Table 1: Device summary*, replacing STM8AL318AT with STM8AL318A.
19-Aug-2015	4	Datasheet status changed to “production data”.
1-Dec-2016	5	– Updated *Table 5: High-density STM8AL3x8x pin description*: two pin names changed from PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH3 to PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH1 and from PF2/ADC1_IN26/[SPI2_SCK]/[USART3_SCK] to PF2/ADC1_IN26/[SPI1_SCK]/[USART3_SCK] – Updated device marking part of *Section 10.1: LQFP80 package information*, *Section 10.2: LQFP64 package information* and *Section 10.3: LQFP48 package information* – Updated *Section 9.2: Absolute maximum ratings* – Updated table footnotes in *Chapter 9: Electrical parameters* – Updated *Figure 12: Power supply thresholds*
5-Dec-2016	6	– Updated *Table 5: High-density STM8AL3x8x pin description*: pin name changed from PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP_IN3M/COMP2_INM/COMP1_INP to PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP2_INM/COMP1_INP.