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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3188tcy

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3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 28 channels (including 4 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.10 Digital-to-analog converter

- 12-bit DAC with 2 buffered outputs (two digital signals are converted into two analog voltage signal outputs)
- Synchronized update capability using timers
- DMA capability for each channel
- External triggers for conversion
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- Input reference voltage V_{REF+} for better resolution

Note: DAC can be served by DMA1.

3.11 Ultra-low-power comparators

The high-density STM8AL3x8x devices embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference is an internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold is one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators are usable together to offer a window function. They wake up from Halt mode.

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.16.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.

USART interfaces are used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 509D	SYSCFG	SYSCFG_RMPCR3	Remapping register 3	0x00
0x00 509E		SYSCFG_RMPCR1	Remapping register 1	0x00
0x00 509F		SYSCFG_RMPCR2	Remapping register 2	0x00
0x00 50A0	ITC - EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF1	External interrupt port select register 1	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8		WFE_CR3	WFE control register 3	0x00
0x00 50A9		WFE_CR4	WFE control register 4	0x00
0x00 50AA	ITC - EXTI	EXTI_CR4	External interrupt control register 4	0x00
0x00 50AB		EXTI_CONF2	External interrupt port select register 2	0x00
0x00 50A9 to 0x00 50AF	Reserved area (7 byte)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2	PWR	PWR_CSR1	Power control and status register 1	0x00
0x00 50B3		PWR_CSR2	Power control and status register 2	0x00
0x00 50B4 to 0x00 50BF	Reserved area (12 byte)			
0x00 50C0	CLK	CLK_CKDIVR	Clock master divider register	0x03
0x00 50C1		CLK_CRTCR	Clock RTC register	0x00(1)
0x00 50C2		CLK_ICKCR	Internal clock control register	0x11
0x00 50C3		CLK_PCKENR1	Peripheral clock gating register 1	0x00
0x00 50C4		CLK_PCKENR2	Peripheral clock gating register 2	0x00
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6		CLK_ECKCR	External clock control register	0x00
0x00 50C7		CLK_SCSR	System clock status register	0x01
0x00 50C8		CLK_SWR	System clock switch register	0x01
0x00 50C9		CLK_SWCR	Clock switch control register	0xX0

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408		LCD_PM4	LCD Port mask register 4	0x00
0x00 5409		LCD_PM5	LCD Port mask register 5	0x00
0x00 540A to 0x00 540B	Reserved area (2 byte)			
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A		LCD_RAM14	LCD display memory 14	0x00
0x00 541B		LCD_RAM15	LCD display memory 15	0x00
0x00 541C		LCD_RAM16	LCD display memory 16	0x00
0x00 541D		LCD_RAM17	LCD display memory 17	0x00
0x00 541E		LCD_RAM18	LCD display memory 18	0x00
0x00 541F		LCD_RAM19	LCD display memory 19	0x00
0x00 5420		LCD_RAM20	LCD display memory 20	0x00
0x00 5421		LCD_RAM21	LCD display memory 21	0x00

6 Interrupt vector mapping

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(3)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(3)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(3)	0x00 8014
4	RTC/LSE_ CSS	RTC alarm interrupt/LSE CSS interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(4)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(3)	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes(3)	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes(3)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(3)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(3)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(3)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(3)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(3)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(3)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(3)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(3)	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2 ADC1	Comparator 1 and 2 interrupt/ADC1	Yes	Yes	Yes	Yes(3)	0x00 8050

Table 11. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
19	TIM2/ USART2	TIM2 update /overflow/trigger/break/ USART2 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 8054
20	TIM2/ USART2	Capture/Compare/USART 2 interrupt	-	-	Yes	Yes(3)	0x00 8058
21	TIM3/ USART3	TIM3 Update /Overflow/Trigger/Break/ USART3 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 805C
22	TIM3/ USART3	TIM3 Capture/Compare/ USART3 Receive register data full/overrun/idle line detected/parity error/ interrupt	-	-	Yes	Yes(3)	0x00 8060
23	TIM1	Update /overflow/trigger/ COM	-	-	-	Yes(3)	0x00 8064
24	TIM1	Capture/Compare	-	-	-	Yes(3)	0x00 8068
25	TIM4	Update/overflow/trigger	-	-	Yes	Yes(3)	0x00 806C
26	SPI1	End of Transfer	Yes	Yes	Yes	Yes(3)	0x00 8070
27	USART 1/ TIM5	USART1 transmission complete/transmit data register empty/ TIM5 update/overflow/ trigger/break	-	-	Yes	Yes(3)	0x00 8074
28	USART 1/ TIM5	USART1 Receive register data full/overrun/idle line detected/parity error/ TIM5 capture/compare	-	-	Yes	Yes(3)	0x00 8078
29	I^2C1/SPI2	I^2C1 interrupt(5)/ SPI2	Yes	Yes	Yes	Yes(3)	0x00 807C

1. The Low-power wait mode is entered when executing a WFE instruction in Low-power run mode.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
4. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt. See more details about the external interrupt port select register (EXTI_CONF) in the STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
5. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

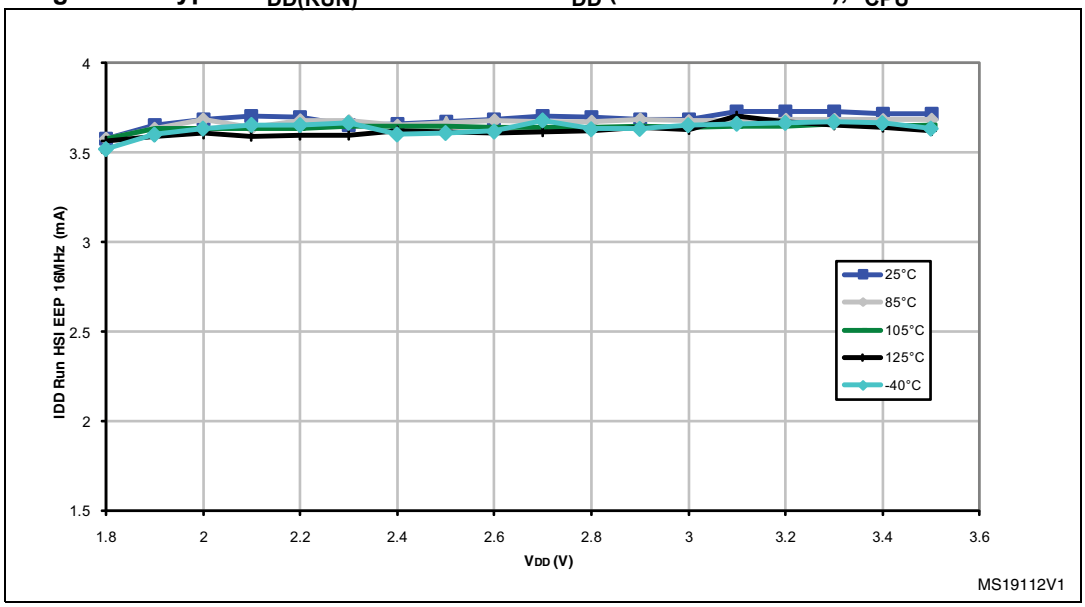
9.3.1 General operating conditions

Table 19. General operating conditions

Symbol	Parameter	Conditions		Min.	Max.	Unit
f_{SYSCLK}(1)	System clock frequency	1.65 V ≤V_{DD} < 3.6 V		0	16	MHz
V_{DD}	Standard operating voltage	BOR detector enabled		1.65(2)	3.6	V
V_{DDA}	Analog operating voltage	ADC and DAC not used	Must be at the same potential as V_{DD}	1.65(2)	3.6	V
		ADC or DAC used		1.8	3.6	V
P_D(3)	Power dissipation at T_A= 85 °C for suffix A devices	LQFP80	-	-	288	mW
		LQFP64	-	-	288	
		LQFP48	-	-	288	
	Power dissipation at T_A= 125 °C for suffix C devices	LQFP80	-	-	131	
		LQFP64	-	-	104	
		LQFP48	-	-	77	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (A suffix version)	-	-40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (C suffix version)	-	-40	125	
T_J	Junction temperature range	-40 °C ≤T_A < 85 °C (A suffix version)		-40	105	
		-40 °C≤ T_A < 125 °C (C suffix version)		-40	130	

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in “Thermal characteristics” table.

Figure 14. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from Flash.

In the following table, data are based on characterization results, unless otherwise specified.

Table 22. Total current consumption in Wait mode

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode,[2] V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.35	0.45[4]	mA
				f_{CPU} = 1 MHz	0.35	0.50[4]	
				f_{CPU} = 4 MHz	0.40	0.60[4]	
				f_{CPU} = 8 MHz	0.50	0.60[4]	
				f_{CPU} = 16 MHz	0.70	0.85	
			HSE external clock (f_{CPU}=f_{HSE})[3]	f_{CPU} = 125 kHz	0.05	0.10[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.20	0.40[4]	
				f_{CPU} = 8 MHz	0.40	0.65[4]	
				f_{CPU} = 16 MHz	0.76	1.15[4]	
			LSI	f_{CPU} = f_{LSI}	60	80[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	70[4]	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.55[4]	mA
				f_{CPU} = 1 MHz	0.40	0.60[4]	
				f_{CPU} = 4 MHz	0.50	0.65[4]	
				f_{CPU} = 8 MHz	0.60	0.75[4]	
				f_{CPU} = 16 MHz	0.80	0.90	
			HSE[3] external clock (f_{CPU}= HSE)	f_{CPU} = 125 kHz	0.07	0.15[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.25	0.45[4]	
				f_{CPU} = 8 MHz	0.50	0.65[4]	
				f_{CPU} = 16 MHz	1.00	1.20[4]	
			LSI	f_{CPU} = f_{LSI}	50	100[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	80[4]	

1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., f_{CPU} = f_{SYSCLK}
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
4. Guaranteed by characterization results.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*

Figure 25. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

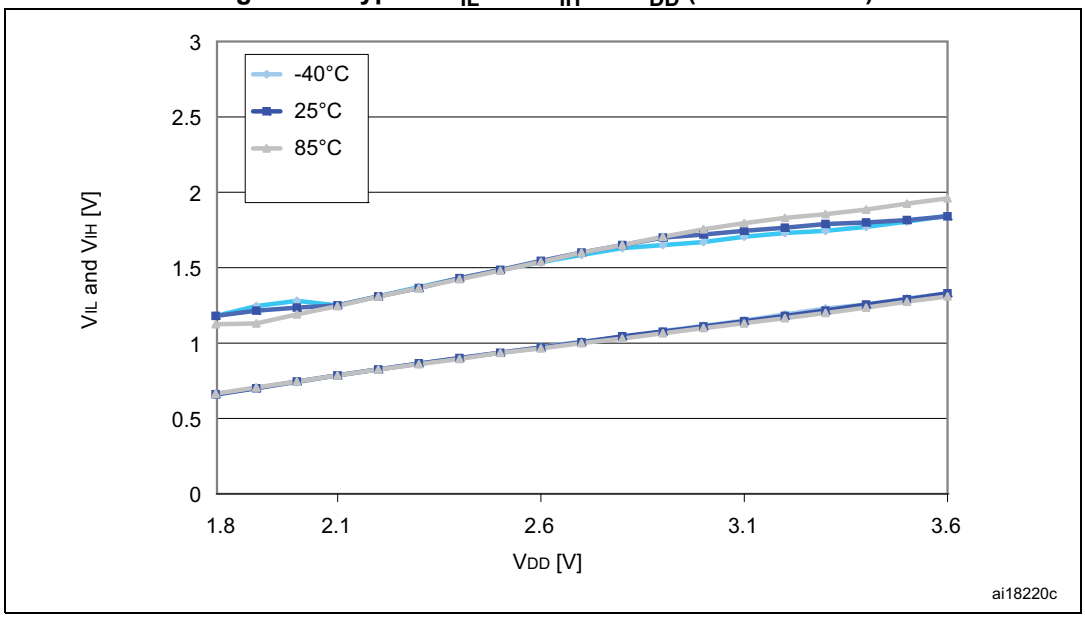


Figure 26. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

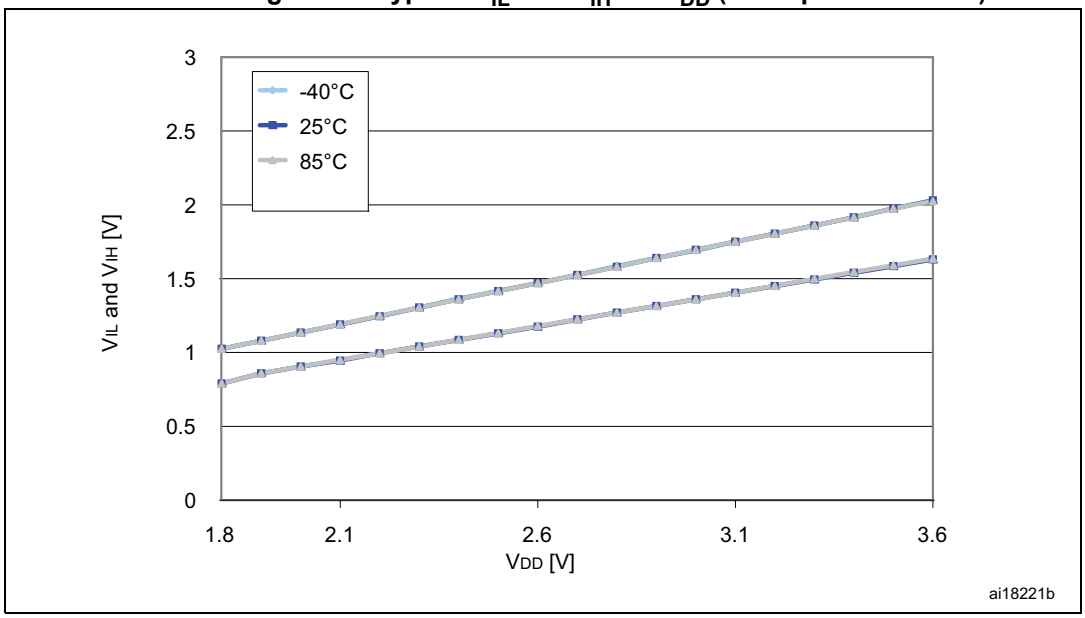


Figure 29. Typical V_{OL} @ V_{DD} = 3.0 V (high sink ports)

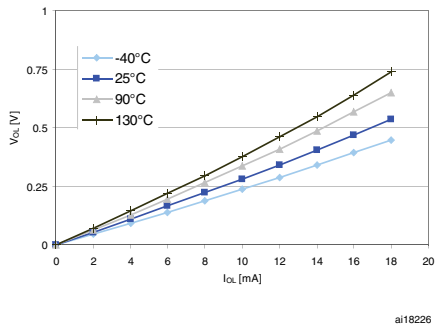


Figure 30. Typical V_{OL} @ V_{DD} = 1.8 V (high sink ports)

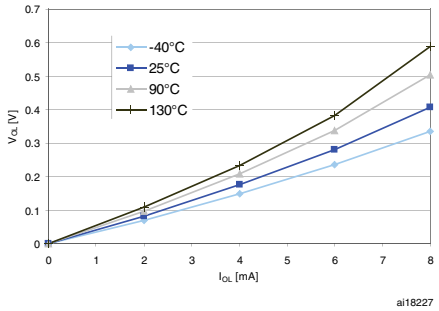


Figure 31. Typical V_{OL} @ V_{DD} = 3.0 V (true open drain ports)

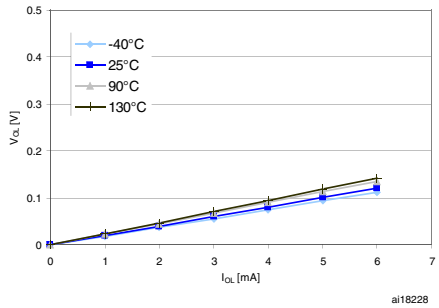


Figure 32. Typical V_{OL} @ V_{DD} = 1.8 V (true open drain ports)

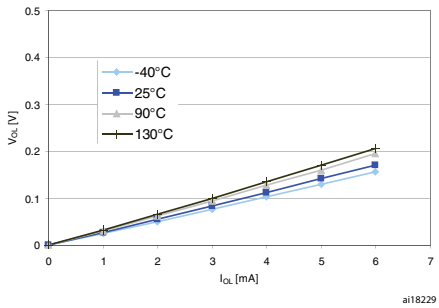


Figure 33. Typical V_{DD} - V_{OH} @ V_{DD} = 3.0 V (high sink ports)

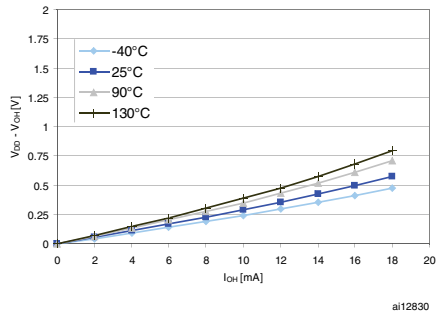


Figure 34. Typical V_{DD} - V_{OH} @ V_{DD} = 1.8 V (high sink ports)

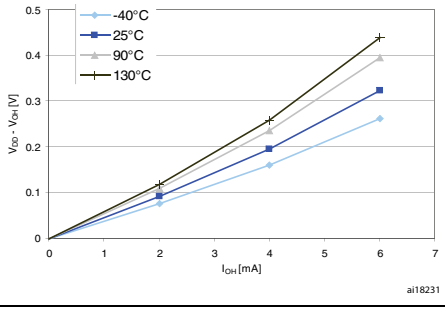
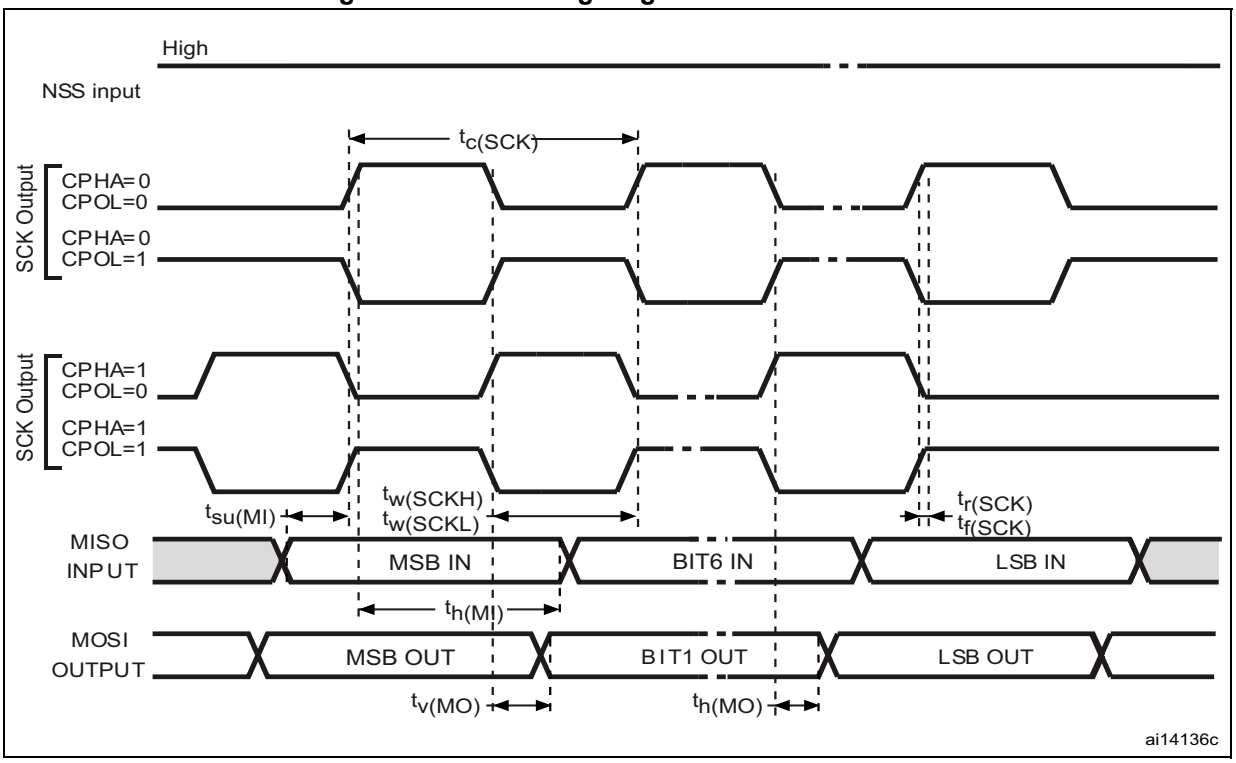


Figure 40. SPI1 timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

I²C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8AL I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 47. I2C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min.(2)	Max. (2)	Min. (2)	Max. (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

Note: For speeds around 200 kHz, the achieved speed has a ±5% tolerance.
For other speed ranges, the achieved speed has a ±2% tolerance.
The above variations depend on the accuracy of the external components used.

In the following table, data are based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.(1)	Unit
DNL	Differential non linearity(2)	R_L ≥5 kΩ, C_L≤50 pF DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(5)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	R_L ≥5 kΩ, C_L≤ 50 pF DACOUT buffer ON(3)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

Figure 44. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

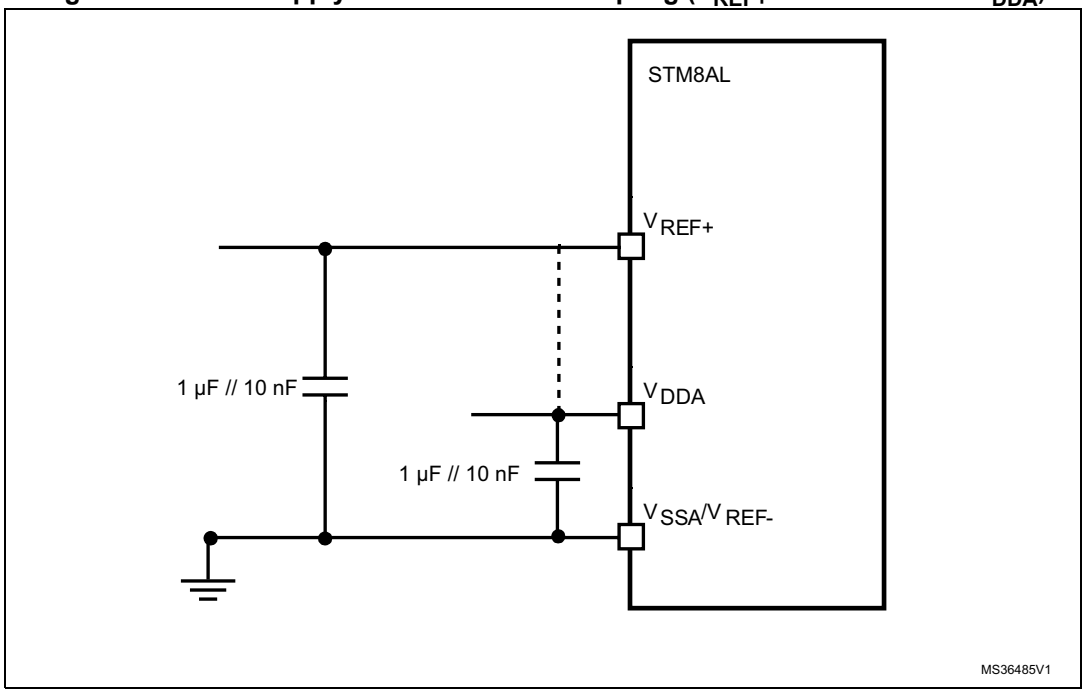
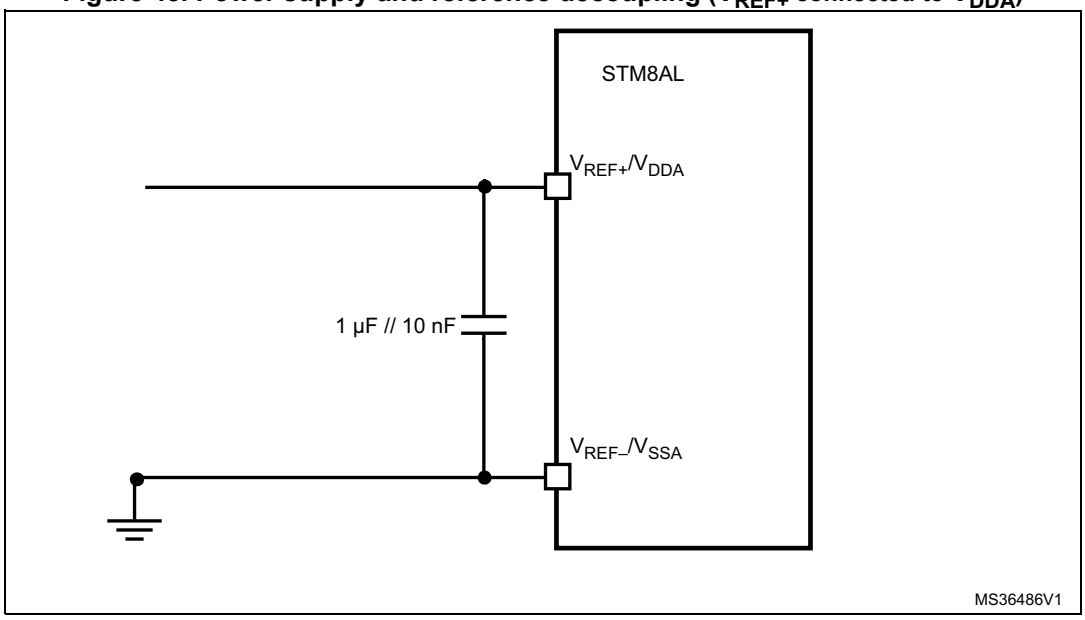


Figure 45. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

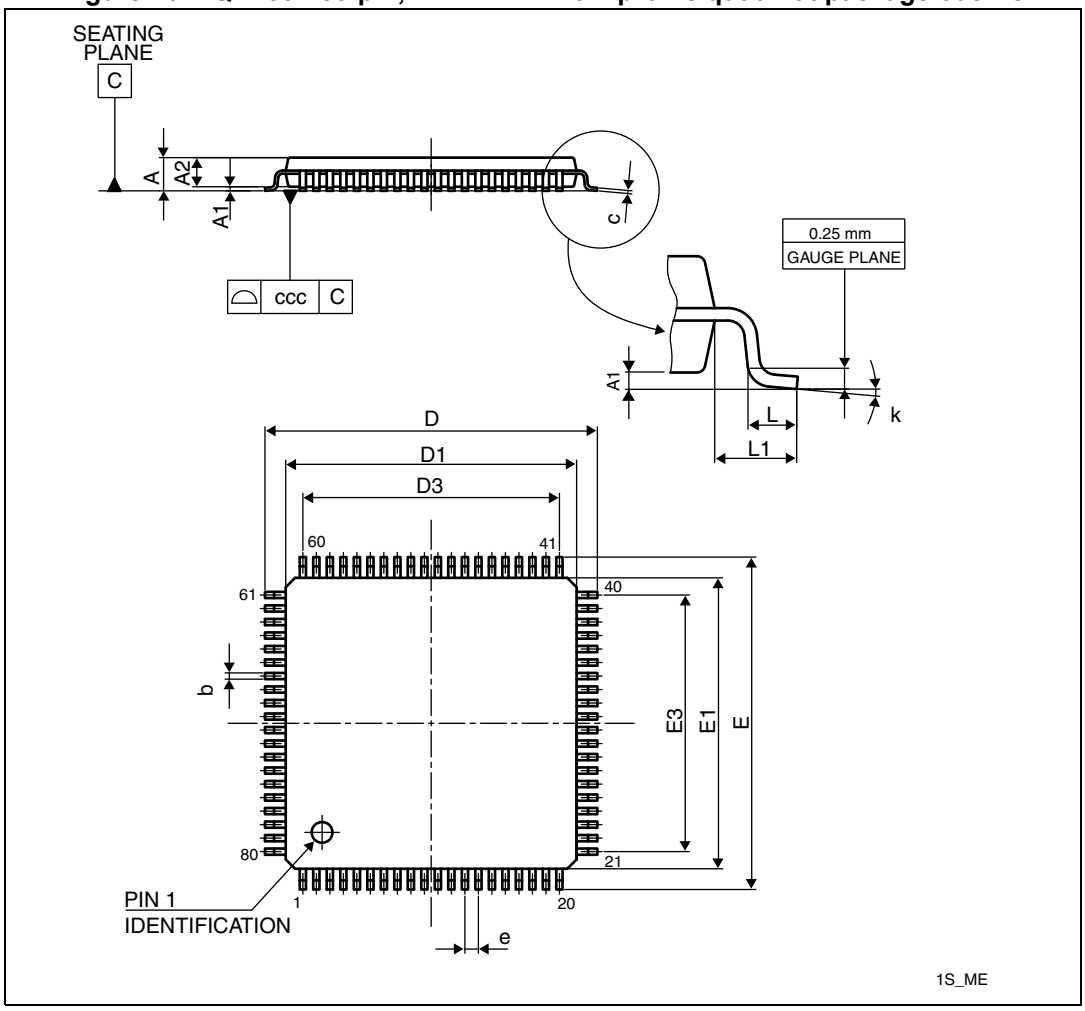


10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 LQFP80 package information

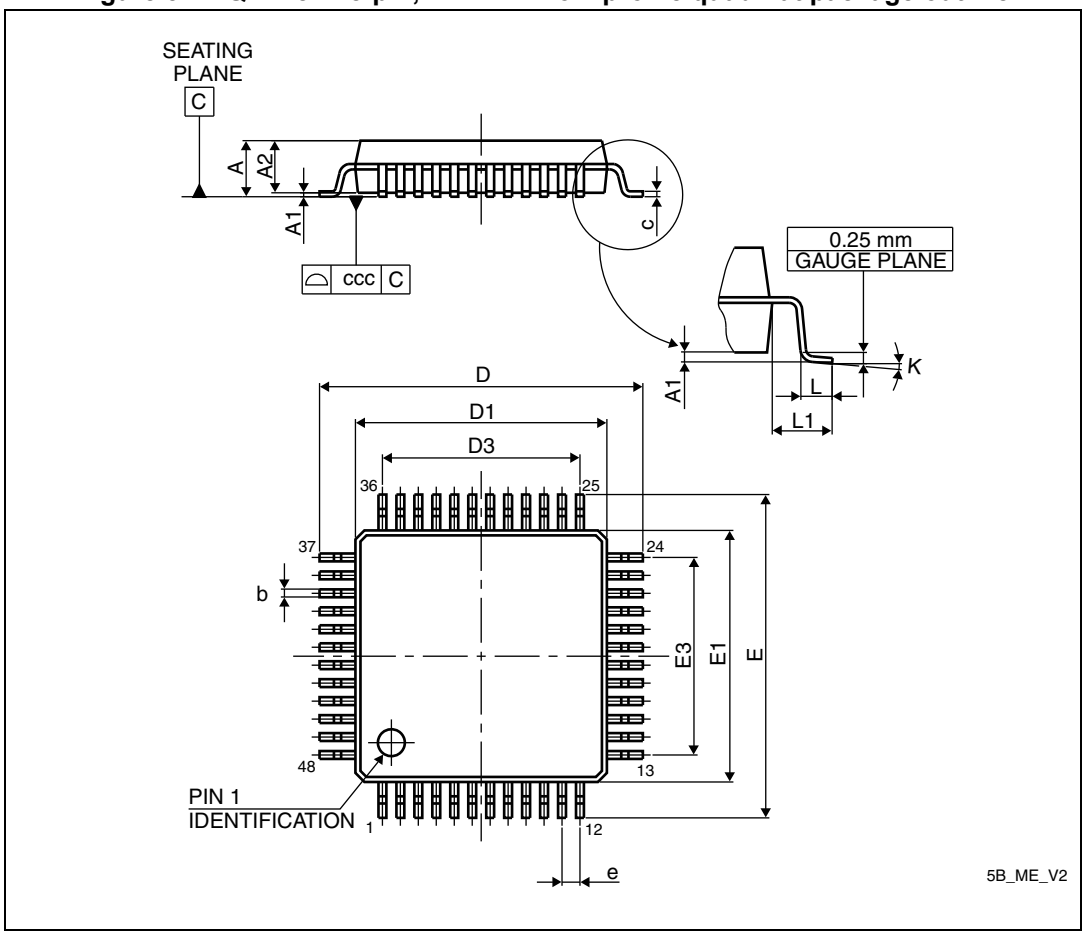
Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

10.3 LQFP48 package information

Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 67. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.