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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l88tcx

List of figures

2.2 Device overview

Table 2. High-density STM8AL3x8x low-power device features and peripheral counts

Features		STM8AL3xx8	STM8AL3xx9	STM8AL3xxA
Flash (Kbyte)		64		
Data EEPROM (Kbyte)		2		
LCD		8x28 or 4x32(1)	8x36 or 4x40(1)	8x40 or 4x44(1)
Timers	Basic	1 (8-bit)	1 (8-bit)	1 (8-bit)
	General purpose	3 (16-bit)	3 (16-bit)	3 (16-bit)
	Advanced control	1 (16-bit)	1 (16-bit)	1 (16-bit)
Communication interfaces	SPI	2	2	2
	I2C	1	1	1
	USART	3	3	3
GPIOs		41(2)	54(2)	68(2)
12-bit synchronized ADC (number of channels)		1 (25)	1 (28)	1 (28)
12-Bit DAC Number of channels		2 2	2 2	2 2
Comparators (COMP1/COMP2)		2	2	2
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator		
CPU frequency		16 MHz		
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR		
Operating temperature		-40 to +85 °C / -40 to +125 °C		
Packages		LQFP48	LQFP64	LQFP80

1. STM8AL3L8x versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3.16 Communication interfaces

3.16.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s (f_{SYSCLK}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 and SPI2 can be served by the DMA1 Controller.

3.16.2 I^2C

The I^2C bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.16.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

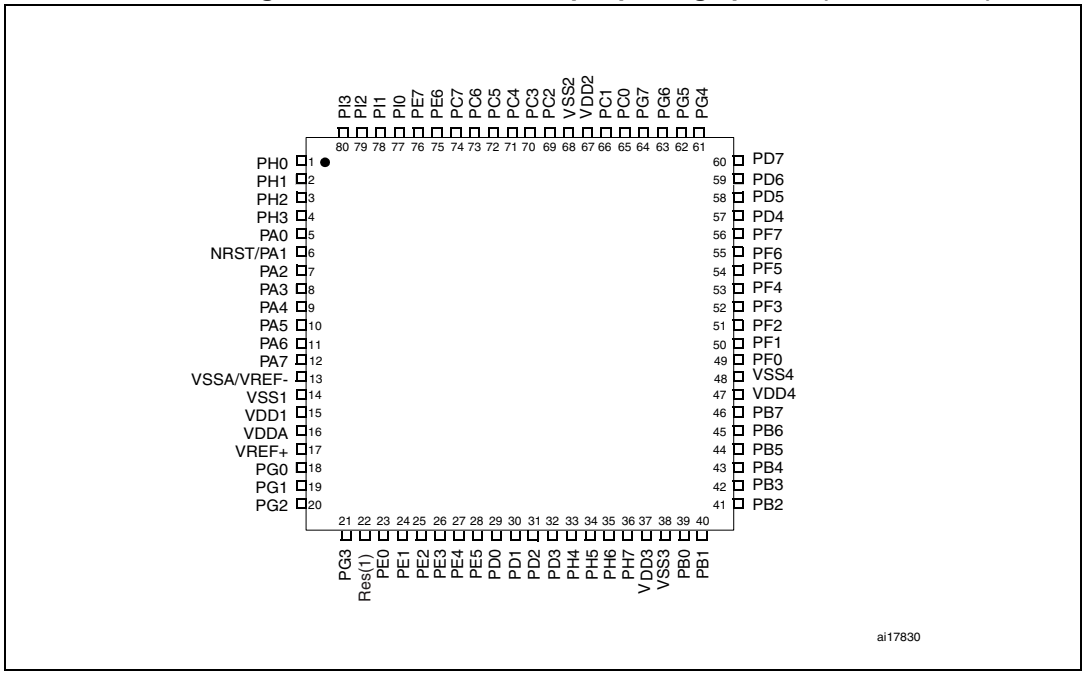
- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.

USART interfaces are used to implement LIN slave communication, with LIN Break detection on the framing error flag (FE in USART_SR register) with a value of 0 in the USART data register (USART_DR).

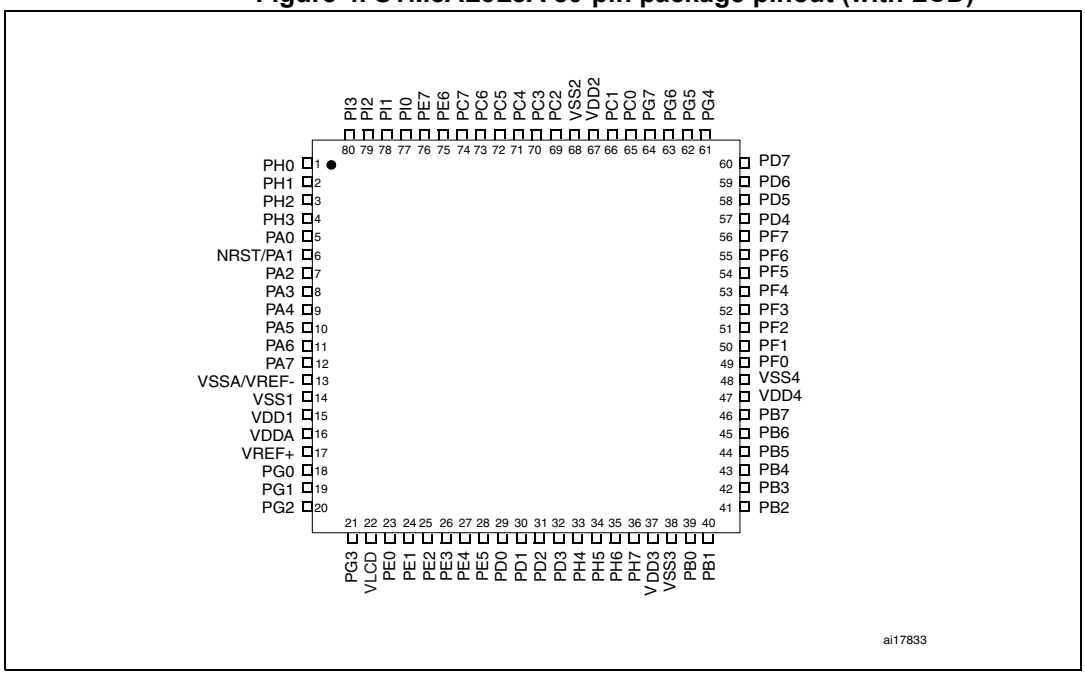
4 Pin description

Figure 3. STM8AL318A 80-pin package pinout (without LCD)



1. Pin 22 is reserved and must be tied to V_{DD}.
2. The above figure shows the package top view.

Figure 4. STM8AL3L8A 80-pin package pinout (with LCD)



1. The above figure shows the package top view.

Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	FT: Five-volt tolerant	
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. High-density STM8AL3x8x pin description

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	-	-	PH0/LCD SEG 36 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H0**	LCD segment 36
2	-	-	PH1/LCD SEG 37 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H1**	LCD segment 37
3	-	-	PH2/LCD SEG 38 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H2**	LCD segment 38
4	-	-	PH3/LCD SEG 39 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H3**	LCD segment 39
6	2	2	NRST/PA1(1)	I/O	-	-	**X**	-	HS	X	X	**Reset**	PA1
7	3	3	PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2)	I/O	-	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
8	4	4	PA3/OSC_OUT/*[USART1 _RX](2)/[SPI1_MOSI](2)*	I/O	-	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
9	5	5	PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / */[Timer 2 - trigger] /* LCD COM 0 / ADC1 input 2/Comparator 1 positive input
10	6	6	PA5/TIM3_BKIN/ *[TIM3_ETR](2)*/ LCD_COM1(3)/ADC1_IN1/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger] /* LCD_COM 1 / ADC1 input 1/Comparator 1 positive input
11	7	7	PA6/ADC1_TRIG/ LCD_COM2(3)/ADC1_IN0/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A6**	ADC1 - trigger / LCD_COM2 / ADC1 input 0/Comparator 1 positive input

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
12	8	8	PA7/LCD_SEG0(3)/ TIM5_CH1	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A7**	LCD segment 0 / TIM5 channel 1
39	31	24	PB0(4)/TIM2_CH1/ LCD_SEG10(3)/ ADC1_IN18/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / LCD segment 10 / ADC1_IN18/Comparator 1 positive input
40	32	25	PB1/TIM3_CH1/ LCD_SEG11(3)/ ADC1_IN17/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17/Comparator 1 positive input
41	33	26	PB2/ TIM2_CH2/ LCD_SEG12(3)/ ADC1_IN16/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/Comparator 1 positive input
42	34	27	PB3/TIM2_ETR/ LCD_SEG13(3)/ ADC1_IN15/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / LCD segment 13 /ADC1_IN15/Comparator 1 positive input
43	35	-	PB4(4)/SPI1_NSS/ LCD_SEG14(3)/ ADC1_IN14/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B4**	SPI1 master/slave select / LCD segment 14 / ADC1_IN14/Comparator 1 positive input
-	-	28	PB4(4)/SPI1_NSS/ LCD_SEG14(3)/ ADC1_IN14/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B4**	SPI1 master/slave select / LCD segment 14 / ADC1_IN14 / DAC channel 2 output/Comparator 1 positive input
44	36	-	PB5/SPI1_SCK/ LCD_SEG15(3)/ ADC1_IN13 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B5**	SPI1 clock / LCD segment 15 / ADC1_IN13/Comparator 1 positive input
-	-	29	PB5/SPI1_SCK/ LCD_SEG15(3)/ ADC1_IN13/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B5**	[SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/Comparator 1 positive input

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
75	63	-	PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26 /PVD_IN /TIM5 break input
76	64	-	PE7/LED_SEG27/ TIM5_ETR	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27/ TIM5 trigger
-	-	48	PE7/LED_SEG27/ TIM5_ETR/ USART3_RX	I/O	FT(5)	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27/TIM5 trig-ger/USART3 receive
77	-	-	PI0/RTC_TAMP1/ *[SPI2_NSS]/[TIM3_CH1*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port I0**	RTC tamper 1 output *[SPI2 master/slave select]* *[TIM3 channel 1]*
78	-	-	PI1/RTC_TAMP2/ *[SPI2_SCK]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port I1**	RTC tamper 2 output *[SPI2 clock]*
79	-	-	PI2/RTC_TAMP3/ *[SPI2_MOSI]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port I2**	RTC tamper 3 output *[SPI2 master out- slave in]*
80	-	-	PI3/TIM5_CH1/ *[SPI2_MISO]/[TIM3_CH2]*	I/O	FT(5)	**X**	X	X	HS	X	X	**Port I3**	TIM5 Channel 1 *[SPI2 master in- slave out]* *[TIM3 channel 2]*
-	-	32	PF0/ADC1_IN24/ DAC_OUT1	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output
-	39	-	PF0/ADC1_IN24/ DAC_OUT1 *[USART3_TX]*	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]*
49	-	-	PF0/ADC1_IN24/ DAC_OUT1/ *[USART3_TX]/[SPI1_MIS O]*	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]* *[SPI1* master in- slave out*]*
50	-	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]* *[SPI1* master out- slave in*]*
-	40	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]*
51	-	-	PF2/ADC1_IN26/ [SPI1_SCK]/ [USART3_SCK]	I/O	-	**X**	X	X	HS	X	X	**Port F2**	ADC1_IN26 *[SPI1 clock]* *[USART3 clock]*
52	-	-	PF3/ADC1_IN27/ [SPI1_NSS]	I/O	-	**X**	X	X	HS	X	X	**Port F3**	ADC1_IN26 *[SPI1 master/slave select]*

Table 8. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	Reserved area (1 byte)			
0x00 5085	DMA1	DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088	Reserved area (2 byte)			
0x00 5089	DMA1	DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092	Reserved area (2 byte)			
0x00 5093	DMA1	DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408		LCD_PM4	LCD Port mask register 4	0x00
0x00 5409		LCD_PM5	LCD Port mask register 5	0x00
0x00 540A to 0x00 540B	Reserved area (2 byte)			
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A		LCD_RAM14	LCD display memory 14	0x00
0x00 541B		LCD_RAM15	LCD display memory 15	0x00
0x00 541C		LCD_RAM16	LCD display memory 16	0x00
0x00 541D		LCD_RAM17	LCD display memory 17	0x00
0x00 541E		LCD_RAM18	LCD display memory 18	0x00
0x00 541F		LCD_RAM19	LCD display memory 19	0x00
0x00 5420		LCD_RAM20	LCD display memory 20	0x00
0x00 5421		LCD_RAM21	LCD display memory 21	0x00

6 Interrupt vector mapping

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Table 11. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(3)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(3)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(3)	0x00 8014
4	RTC/LSE_ CSS	RTC alarm interrupt/LSE CSS interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(4)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(3)	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes(3)	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes(3)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(3)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(3)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(3)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(3)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(3)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(3)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(3)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(3)	0x00 8044
16	LCD	LCD interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2 ADC1	Comparator 1 and 2 interrupt/ADC1	Yes	Yes	Yes	Yes(3)	0x00 8050

9.3.2 Embedded reset and power control block characteristics

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{VDD}	V_{DD} rise time rate	BOR detector enabled	0(1)	-	∞(1)	µs/V
	V_{DD} fall time rate	BOR detector enabled	20(1)	-	∞(1)	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising BOR detector enabled	-	3	-	ms
V_{PDR}	Power-down reset threshold	Falling edge	1.3	1.5	1.65(2)	V
V_{BOR0}	Brown-out reset threshold 0 (BOR_TH[2:0]=000)	Falling edge	1.67	1.7	1.74(2)	
		Rising edge	1.69(2)	1.75	1.80	
V_{BOR1}	Brown-out reset threshold 1 (BOR_TH[2:0]=001)	Falling edge	1.87	1.93	1.97(2)	
		Rising edge	1.96(2)	2.04	2.07	
V_{BOR2}	Brown-out reset threshold 2 (BOR_TH[2:0]=010)	Falling edge	2.22	2.3	2.35(2)	
		Rising edge	2.31(2)	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3 (BOR_TH[2:0]=011)	Falling edge	2.45	2.55	2.60(2)	
		Rising edge	2.54(2)	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4 (BOR_TH[2:0]=100)	Falling edge	2.68	2.80	2.85(2)	
		Rising edge	2.78(2)	2.90	2.95	
V_{PVD0}	PVD threshold 0	Falling edge	1.80	1.84	1.88(2)	V
		Rising edge	1.88(2)	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09(2)	
		Rising edge	2.08(2)	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.2	2.24	2.28(2)	
		Rising edge	2.28(2)	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48(2)	
		Rising edge	2.47(2)	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69(2)	
		Rising edge	2.68(2)	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88(2)	
		Rising edge	2.87(2)	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09(2)	
		Rising edge	3.08(2)	3.15	3.20	

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

General conditions for V_{DD} apply, TA = -40 °C to 125 °C.

Table 21. Total current consumption in Run mode

Symbol	Parameter	Conditions			Typ.	Max.	Unit
$I_{DD(RUN)}$	Supply current in run mode(1)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(2)	f_{CPU} = 125 kHz	0.40	0.55(3)	mA
				f_{CPU} = 1 MHz	0.50	0.65(3)	
				f_{CPU} = 4 MHz	0.75	1.00(3)	
				f_{CPU} = 8 MHz	1.10	1.40(3)	
				f_{CPU} = 16 MHz	1.85	2.35	
			HSE external clock (f_{CPU}=f_{HSE})(4)	f_{CPU} = 125 kHz	0.07	0.20(3)	
				f_{CPU} = 1 MHz	0.20	0.25(3)	
				f_{CPU} = 4 MHz	0.55	0.75(3)	
				f_{CPU} = 8 MHz	1.00	1.25(3)	
				f_{CPU} = 16 MHz	1.90	2.30(3)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	40	50(3)	µA
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	40	60(3)	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(5)	f_{CPU} = 125 kHz	0.45	0.60(3)	mA
				f_{CPU} = 1 MHz	0.60	0.85(3)	
				f_{CPU} = 4 MHz	1.10	1.45(3)	
				f_{CPU} = 8 MHz	1.90	2.40(3)	
				f_{CPU} = 16 MHz	3.80	4.90	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.30	0.45(3)	
				f_{CPU} = 1 MHz	0.40	0.55(3)	
				f_{CPU} = 4 MHz	1.15	1.50(3)	
				f_{CPU} = 8 MHz	2.15	2.75(3)	
				f_{CPU} = 16 MHz	4.00	4.75(3)	
			LSI RC osc.	f_{CPU} = f_{LSI}	100	150(3)	µA
			LSE external clock (32.768 kHz)(6)	f_{CPU} = f_{LSE}	100	120(3)	

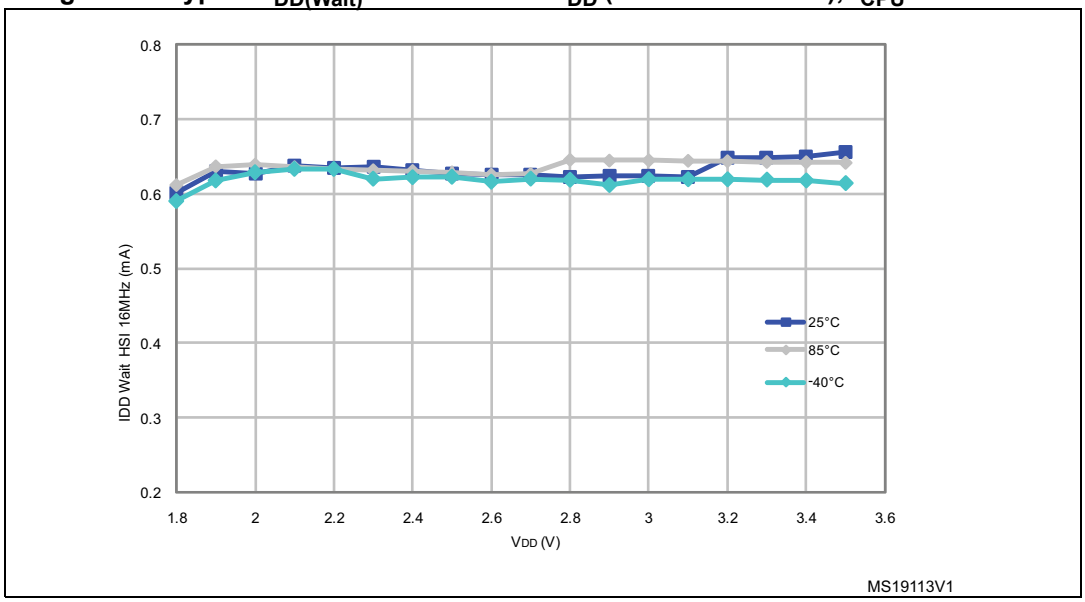
In the following table, data are based on characterization results, unless otherwise specified.

Table 22. Total current consumption in Wait mode

Symbol	Parameter	Conditions[1]			Typ	Max	Unit
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from RAM with Flash in I_{DDQ} mode,[2] V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.35	0.45[4]	mA
				f_{CPU} = 1 MHz	0.35	0.50[4]	
				f_{CPU} = 4 MHz	0.40	0.60[4]	
				f_{CPU} = 8 MHz	0.50	0.60[4]	
				f_{CPU} = 16 MHz	0.70	0.85	
			HSE external clock (f_{CPU}=f_{HSE})[3]	f_{CPU} = 125 kHz	0.05	0.10[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.20	0.40[4]	
				f_{CPU} = 8 MHz	0.40	0.65[4]	
				f_{CPU} = 16 MHz	0.76	1.15[4]	
			LSI	f_{CPU} = f_{LSI}	60	80[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	70[4]	
$I_{DD(Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI	f_{CPU} = 125 kHz	0.38	0.55[4]	mA
				f_{CPU} = 1 MHz	0.40	0.60[4]	
				f_{CPU} = 4 MHz	0.50	0.65[4]	
				f_{CPU} = 8 MHz	0.60	0.75[4]	
				f_{CPU} = 16 MHz	0.80	0.90	
			HSE[3] external clock (f_{CPU}= HSE)	f_{CPU} = 125 kHz	0.07	0.15[4]	
				f_{CPU} = 1 MHz	0.10	0.20[4]	
				f_{CPU} = 4 MHz	0.25	0.45[4]	
				f_{CPU} = 8 MHz	0.50	0.65[4]	
				f_{CPU} = 16 MHz	1.00	1.20[4]	
			LSI	f_{CPU} = f_{LSI}	50	100[4]	µA
			LSE[5] external clock (32.768 kHz)	f_{CPU} = f_{LSE}	50	80[4]	

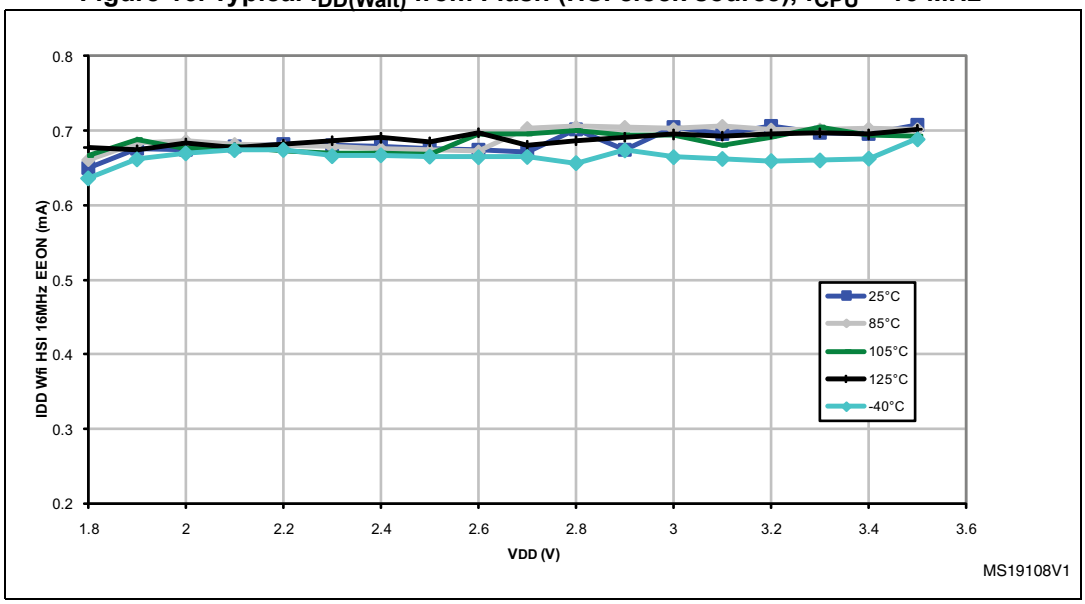
1. All peripherals OFF, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., f_{CPU} = f_{SYSCLK}
2. Flash is configured in I_{DDQ} mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
3. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*.
4. Guaranteed by characterization results.
5. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 33*

Figure 15. Typical $I_{DD(Wait)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from RAM.

Figure 16. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from Flash.

5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD} /2. Floating DAC output.
6. Data based on a differential I_{DD} measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

Table 29. Current consumption under external reset

Symbol	Parameter	Conditions		Typ.	Unit
$I_{DD(RST)}$	Supply current under external reset (1)	PB1/PB3/PA5 pins are externally tied to V_{DD}	V_{DD} = 1.8 V	48	µA
			V_{DD} = 3 V	80	
			V_{DD} = 3.6 V	95	

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

9.3.4 Clock and timing characteristics

HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for V_{DD} and T_A.

Table 30. HSE external clock characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE_ext} (1)	External clock source frequency	-	1	-	16	MHz
V_{HSEH}	OSC_IN input pin high-level voltage		0.7 x V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low-level voltage		V_{SS}	-	0.3 x V_{DD}	
$C_{in(HSE)}$ (1)	OSC_IN input capacitance	-	-	2.6	-	pF
I_{LEAK_HSE}	OSC_IN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-	-	±500	nA

1. Guaranteed by design.

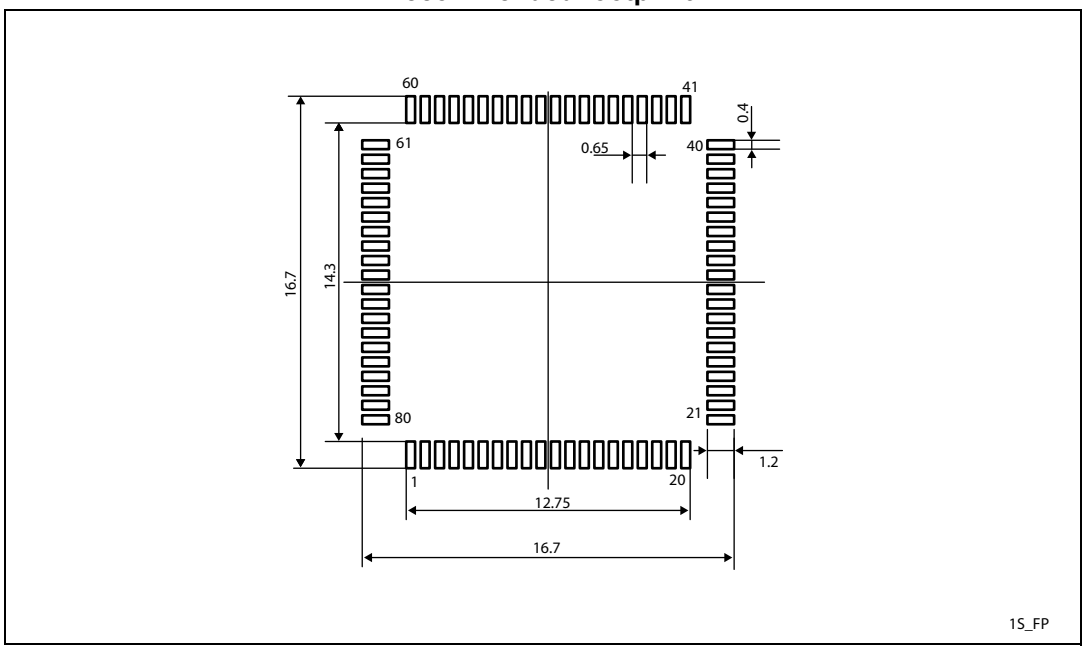
In the following table, data are guaranteed by design, not tested in production.

Table 55. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel is routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

Figure 47. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

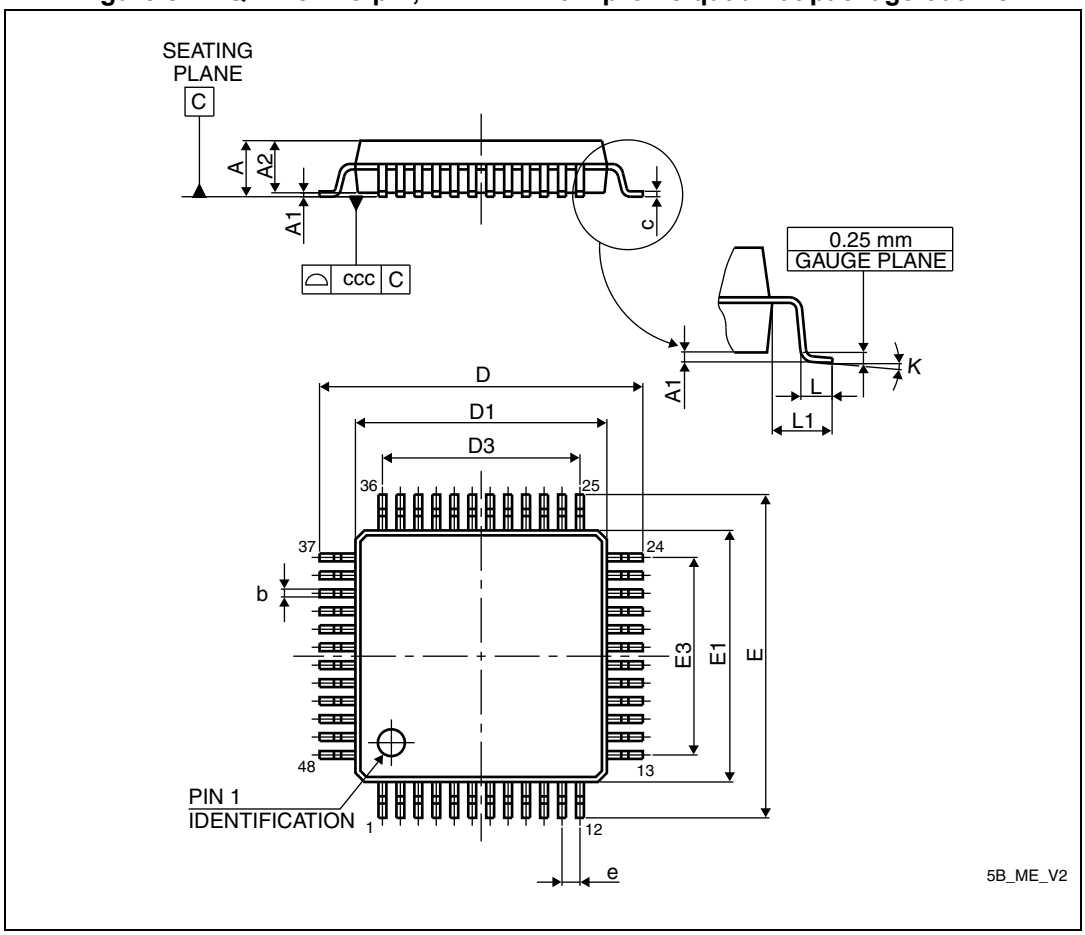
Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

10.3 LQFP48 package information

Figure 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.