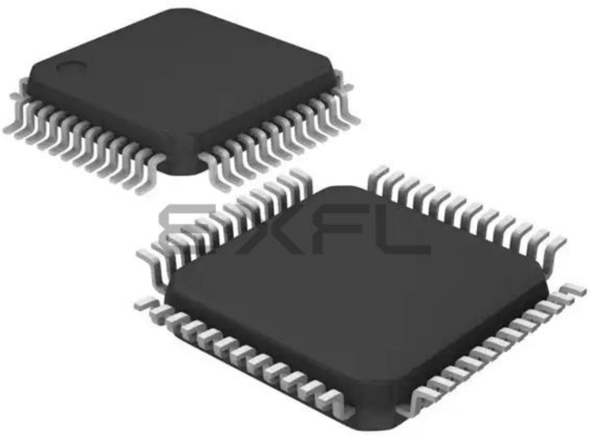

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 25x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l88tcy

2 Description

The high-density STM8AL3x8x ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density STM8AL3x8x microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, 8x40 or 4x44-segment LCD, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an I^2C interface, and three USARTs. One 8x40 or 4x44-segment LCD is available on the STM8AL3L8x devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

2.1 STM8AL ultra-low-power 8-bit family benefits

High-density STM8AL3x8x devices are part of the STM8AL automotive ultra-low-power 8-bit family providing the following benefits:

- Integrated system
  - 64 Kbytes of high-density embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - 4 Kbytes of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- Ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
58	46	-	PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/Comparator 1 positive input
-	-	34	PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/SPI2_MOSI/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ SPI2 master out/slave in/Comparator 1 positive input
59	47		PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ COMP1_INP/VREFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/Comparator 1 positive input/Internal reference voltage output
-	-	35	PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ SPI2_SCK/COMP1_INP/ VREFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/SPI2 clock/Comparator 1 positive input/Internal reference voltage output
60	48	-	PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM/ COMP1_INP/VREFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm/Comparator 1 positive input/Internal reference voltage output
-	-	36	PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM/ SPI2_NSS/COMP1_INP/V REFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm /SPI2 master/slave select/Comparator 1 positive input/Internal reference voltage output
61	49	-	PG4/LCD_SEG32/ SPI2_NSS	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G4**	LCD segment 32 / SPI2 master/slave select
62	50	-	PG5/LCD_SEG33/ SPI2_SCK	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G5**	LCD segment 33 / SPI2 clock
63	51	-	PG6/LCD_SEG34/ SPI2_MOSI	I/O	FT(5)	**X**	X	X	HS	X	X	**Port G6**	LCD segment 34 / SPI2 master out- slave in

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
75	63	-	PE6/LCD_SEG26[3]/ PVD_IN/TIM5_BKIN	I/O	FT[5]	**X**	X	X	HS	X	X	**Port E6**	LCD segment 26 /PVD_IN /TIM5 break input
76	64	-	PE7/LED_SEG27/ TIM5_ETR	I/O	FT[5]	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27/ TIM5 trigger
-	-	48	PE7/LED_SEG27/ TIM5_ETR/ USART3_RX	I/O	FT[5]	**X**	X	X	HS	X	X	**Port E7**	LCD segment 27/TIM5 trig-ger/USART3 receive
77	-	-	PI0/RTC_TAMP1/ *[SPI2_NSS]/[TIM3_CH1*	I/O	FT[5]	**X**	X	X	HS	X	X	**Port I0**	RTC tamper 1 output *[SPI2 master/slave select]* *[TIM3 channel 1]*
78	-	-	PI1/RTC_TAMP2/ *[SPI2_SCK]*	I/O	FT[5]	**X**	X	X	HS	X	X	**Port I1**	RTC tamper 2 output *[SPI2 clock]*
79	-	-	PI2/RTC_TAMP3/ *[SPI2_MOSI]*	I/O	FT[5]	**X**	X	X	HS	X	X	**Port I2**	RTC tamper 3 output *[SPI2 master out- slave in]*
80	-	-	PI3/TIM5_CH1/ *[SPI2_MISO]/[TIM3_CH2]*	I/O	FT[5]	**X**	X	X	HS	X	X	**Port I3**	TIM5 Channel 1 *[SPI2 master in- slave out]* *[TIM3 channel 2]*
-	-	32	PF0/ADC1_IN24/ DAC_OUT1	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output
-	39	-	PF0/ADC1_IN24/ DAC_OUT1 *[USART3_TX]*	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]*
49	-	-	PF0/ADC1_IN24/ DAC_OUT1/ *[USART3_TX]/[SPI1_MISO]*	I/O	-	**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]* *[SPI1* master in- slave out*]*
50	-	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]* *[SPI1* master out- slave in*]*
-	40	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]*	I/O	-	**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]*
51	-	-	PF2/ADC1_IN26/ [SPI1_SCK]/ [USART3_SCK]	I/O	-	**X**	X	X	HS	X	X	**Port F2**	ADC1_IN26 *[SPI1 clock]* *[USART3 clock]*
52	-	-	PF3/ADC1_IN27/ [SPI1_NSS]	I/O	-	**X**	X	X	HS	X	X	**Port F3**	ADC1_IN26 *[SPI1 master/slave select]*

Table 9. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 502E to 0x00 5049	Reserved area (44 byte)			
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash program memory unprotection key register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection key register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0x00
0x00 5055 to 0x00 506F	Reserved area (27 byte)			
0x00 5070	DMA1	DMA1_GCSR	DMA1 global configuration & status register	0xFC
0x00 5071		DMA1_GIR1	DMA1 global interrupt register 1	0x00
0x00 5072 to 0x00 5074	Reserved area (3 byte)			
0x00 5075	DMA1	DMA1_C0CR	DMA1 channel 0 configuration register	0x00
0x00 5076		DMA1_C0SPR	DMA1 channel 0 status & priority register	0x00
0x00 5077		DMA1_C0NDTR	DMA1 number of data to transfer register (channel 0)	0x00
0x00 5078		DMA1_C0PARH	DMA1 peripheral address high register (channel 0)	0x52
0x00 5079		DMA1_C0PARL	DMA1 peripheral address low register (channel 0)	0x00
0x00 507A		Reserved area (1 byte)		
0x00 507B		DMA1_C0M0ARH	DMA1 memory 0 address high register (channel 0)	0x00
0x00 507C		DMA1_C0M0ARL	DMA1 memory 0 address low register (channel 0)	0x00
0x00 507D to 0x00 507E	Reserved area (2 byte)			
0x00 507F	DMA1	DMA1_C1CR	DMA1 channel 1 configuration register	0x00
0x00 5080		DMA1_C1SPR	DMA1 channel 1 status & priority register	0x00
0x00 5081		DMA1_C1NDTR	DMA1 number of data to transfer register (channel 1)	0x00
0x00 5082		DMA1_C1PARH	DMA1 peripheral address high register (channel 1)	0x52
0x00 5083		DMA1_C1PARL	DMA1 peripheral address low register (channel 1)	0x00

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5084	Reserved area (1 byte)			
0x00 5085	DMA1	DMA1_C1M0ARH	DMA1 memory 0 address high register (channel 1)	0x00
0x00 5086		DMA1_C1M0ARL	DMA1 memory 0 address low register (channel 1)	0x00
0x00 5087 0x00 5088	Reserved area (2 byte)			
0x00 5089	DMA1	DMA1_C2CR	DMA1 channel 2 configuration register	0x00
0x00 508A		DMA1_C2SPR	DMA1 channel 2 status & priority register	0x00
0x00 508B		DMA1_C2NDTR	DMA1 number of data to transfer register (channel 2)	0x00
0x00 508C		DMA1_C2PARH	DMA1 peripheral address high register (channel 2)	0x52
0x00 508D		DMA1_C2PARL	DMA1 peripheral address low register (channel 2)	0x00
0x00 508E		Reserved area (1 byte)		
0x00 508F		DMA1_C2M0ARH	DMA1 memory 0 address high register (channel 2)	0x00
0x00 5090		DMA1_C2M0ARL	DMA1 memory 0 address low register (channel 2)	0x00
0x00 5091 0x00 5092	Reserved area (2 byte)			
0x00 5093	DMA1	DMA1_C3CR	DMA1 channel 3 configuration register	0x00
0x00 5094		DMA1_C3SPR	DMA1 channel 3 status & priority register	0x00
0x00 5095		DMA1_C3NDTR	DMA1 number of data to transfer register (channel 3)	0x00
0x00 5096		DMA1_C3PARH_ C3M1ARH	DMA1 peripheral address high register (channel 3)	0x40
0x00 5097		DMA1_C3PARL_ C3M1ARL	DMA1 peripheral address low register (channel 3)	0x00
0x00 5098		DMA_C3M0EAR	DMA channel 3 memory 0 extended address register	0x00
0x00 5099		DMA1_C3M0ARH	DMA1 memory 0 address high register (channel 3)	0x00
0x00 509A		DMA1_C3M0ARL	DMA1 memory 0 address low register (channel 3)	0x00
0x00 509B to 0x00 509C	Reserved area (3 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 53C8 to 0x00 53DF	Reserved area			
0x00 53E0	USART2	USART2_SR	USART2 status register	0xC0
0x00 53E1		USART2_DR	USART2 data register	0xXX
0x00 53E2		USART2_BRR1	USART2 baud rate register 1	0x00
0x00 53E3		USART2_BRR2	USART2 baud rate register 2	0x00
0x00 53E4		USART2_CR1	USART2 control register 1	0x00
0x00 53E5		USART2_CR2	USART2 control register 2	0x00
0x00 53E6		USART2_CR3	USART2 control register 3	0x00
0x00 53E7		USART2_CR4	USART2 control register 4	0x00
0x00 53E8		USART2_CR5	USART2 control register 5	0x00
0x00 53E9		USART2_GTR	USART2 guard time register	0x00
0x00 53EA		USART2_PSCR	USART2 prescaler register	0x00
0x00 53EB to 0x00 53EF	Reserved area			
0x00 53F0	USART3	USART3_SR	USART3 status register	0xC0
0x00 53F1		USART3_DR	USART3 data register	0xXX
0x00 53F2		USART3_BRR1	USART3 baud rate register 1	0x00
0x00 53F3		USART3_BRR2	USART3 baud rate register 2	0x00
0x00 53F4		USART3_CR1	USART3 control register 1	0x00
0x00 53F5		USART3_CR2	USART3 control register 2	0x00
0x00 53F6		USART3_CR3	USART3 control register 3	0x00
0x00 53F7		USART3_CR4	USART3 control register 4	0x00
0x00 53F8		USART3_CR5	USART3 control register 5	0x00
0x00 53F9		USART3_GTR	USART3 guard time register	0x00
0x00 53FA		USART3_PSCR	USART3 prescaler register	0x00
0x00 53FB to 0x00 53FF	Reserved area			

7 Option byte

Option byte contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option byte can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option byte can also be modified 'on the fly' by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which are only taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8AL318x/STM8AL3L8x Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 12. Option byte addresses

<table>
<tr><th rowspan="2">Address</th><th rowspan="2">Option name</th><th rowspan="2">Option byte No.</th><th colspan="8">Option bits</th><th rowspan="2">Factory default setting</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00 4800</td><td>Read-out protection (ROP)</td><td>OPT0</td><td colspan="8">ROP[7:0]</td><td>0xAA</td></tr>
<tr><td>00 4802</td><td>UBC (User Boot code size)</td><td>OPT1</td><td colspan="8">UBC[7:0]</td><td>0x00</td></tr>
<tr><td>00 4807</td><td>PCODESIZE</td><td>OPT2</td><td colspan="8">PCODE[7:0]</td><td>0x00</td></tr>
<tr><td>00 4808</td><td>Independent watchdog option</td><td>OPT3 [3:0]</td><td colspan="4">Reserved</td><td>WWDG _HALT</td><td>WWDG _HW</td><td>IWDG _HALT</td><td>IWDG _HW</td><td>0x00</td></tr>
<tr><td>00 4809</td><td>Number of stabilization clock cycles for HSE and LSE oscillators</td><td>OPT4</td><td colspan="4">Reserved</td><td colspan="2">LSECNT[1:0]</td><td colspan="2">HSECNT[1:0]</td><td>0x00</td></tr>
<tr><td>00 480A</td><td>Brownout reset (BOR)</td><td>OPT5 [3:0]</td><td colspan="4">Reserved</td><td colspan="3">BOR_TH</td><td>BOR_ ON</td><td>0x01</td></tr>
<tr><td>00 480B</td><td rowspan="2">Bootloader option byte (OPTBL)</td><td rowspan="2">OPTBL [15:0]</td><td colspan="8" rowspan="2">OPTBL[15:0]</td><td>0x00</td></tr>
<tr><td>00 480C</td><td>0x00</td></tr>
</table>

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier are never altered by the user.

The unique device identifier is read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

General conditions for V_{DD} apply, TA = -40 °C to 125 °C.

Table 21. Total current consumption in Run mode

Symbol	Parameter	Conditions			Typ.	Max.	Unit
$I_{DD(RUN)}$	Supply current in run mode(1)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(2)	f_{CPU} = 125 kHz	0.40	0.55(3)	mA
				f_{CPU} = 1 MHz	0.50	0.65(3)	
				f_{CPU} = 4 MHz	0.75	1.00(3)	
				f_{CPU} = 8 MHz	1.10	1.40(3)	
				f_{CPU} = 16 MHz	1.85	2.35	
			HSE external clock (f_{CPU}=f_{HSE})(4)	f_{CPU} = 125 kHz	0.07	0.20(3)	
				f_{CPU} = 1 MHz	0.20	0.25(3)	
				f_{CPU} = 4 MHz	0.55	0.75(3)	
				f_{CPU} = 8 MHz	1.00	1.25(3)	
				f_{CPU} = 16 MHz	1.90	2.30(3)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	40	50(3)	µA
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	40	60(3)	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(5)	f_{CPU} = 125 kHz	0.45	0.60(3)	mA
				f_{CPU} = 1 MHz	0.60	0.85(3)	
				f_{CPU} = 4 MHz	1.10	1.45(3)	
				f_{CPU} = 8 MHz	1.90	2.40(3)	
				f_{CPU} = 16 MHz	3.80	4.90	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.30	0.45(3)	
				f_{CPU} = 1 MHz	0.40	0.55(3)	
				f_{CPU} = 4 MHz	1.15	1.50(3)	
				f_{CPU} = 8 MHz	2.15	2.75(3)	
				f_{CPU} = 16 MHz	4.00	4.75(3)	
			LSI RC osc.	f_{CPU} = f_{LSI}	100	150(3)	µA
			LSE external clock (32.768 kHz)(6)	f_{CPU} = f_{LSE}	100	120(3)	

Table 42. Output driving current (high sink ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Standard	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +2 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +2 mA, V_{DD} = 1.8 V	-	0.45	V
			I_{IO} = +10 mA, V_{DD} = 3.0 V	-	0.7	V
	V_{OH} (2)	Output high-level voltage for an I/O pin	I_{IO} = -2 mA, V_{DD} = 3.0 V	V_{DD}-0.45	-	V
			I_{IO} = -1 mA, V_{DD} = 1.8 V	V_{DD}-0.45	-	V
			I_{IO} = -10 mA, V_{DD} = 3.0 V	V_{DD}-0.7	-	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

Table 43. Output driving current (true open drain ports)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
Open drain	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +3 mA, V_{DD} = 3.0 V	-	0.45	V
			I_{IO} = +1 mA, V_{DD} = 1.8 V	-	0.45	

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

Table 44. Output driving current (PA0 with high sink LED driver capability)

I/O Type	Symbol	Parameter	Conditions	Min.	Max.	Unit
IR	V_{OL} (1)	Output low-level voltage for an I/O pin	I_{IO} = +20 mA, V_{DD} = 2.0 V	-	0.45	V

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

NRST pin

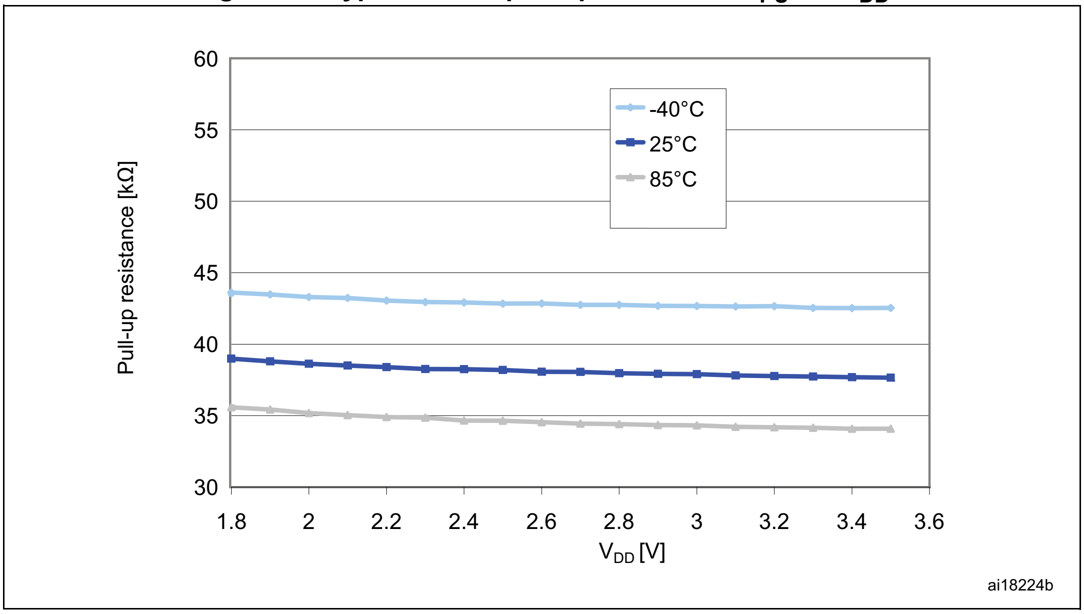
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 45. NRST pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage	-	V_{SS} (1)	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high-level voltage (1)	-	1.4(1)	-	V_{DD} (1)	
$V_{OL(NRST)}$	NRST output low-level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4(1)	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis	-	10%V_{DD} (2)(3)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor	-	30(1)	45	60(1)	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	50(3)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	300(3)	-	-	

1. Guaranteed by characterization results.
2. 200 mV min.
3. Guaranteed by design.

Figure 35. Typical NRST pull-up resistance R_{PU} vs. V_{DD}



I^2C - Inter IC control interface

Subject to general operating conditions for V_{DD}, f_{SYSCLK}, and T_A unless otherwise specified.

The STM8AL I^2C interface (I2C1) meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 47. I2C characteristics

Symbol	Parameter	Standard mode I^2C		Fast mode I^2C(1)		Unit
		Min.(2)	Max. (2)	Min. (2)	Max. (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	µs
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	ns
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SYSCLK} must be at least equal to 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.

Note: *For speeds around 200 kHz, the achieved speed has a ±5% tolerance.*
For other speed ranges, the achieved speed has a ±2% tolerance.
The above variations depend on the accuracy of the external components used.

9.3.9 LCD controller (STM8AL3L8x only)

In the following table, data are guaranteed by design, not tested in production.

Table 48. LCD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.7	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.8	-	
V_{LCD3}	LCD internal reference voltage 3	-	3.0	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.1	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.2	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.5	-	
C_{EXT}	V_{LCD} external capacitance	0.1	1	2	µF
I_{DD}	Supply current(1) at V_{DD} = 1.8 V	-	3	-	µA
	Supply current(1) at V_{DD} = 3 V	-	3	-	
R_{HN}(2)	High value resistive network (low drive)	-	6.6	-	MΩ
R_{LN}(3)	Low value resistive network (high drive)	-	240	-	kΩ
V_{33}	Segment/Common higher level voltage	-	-	V_{LCDx}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4V_{LCDx}$	-	
V_{23}	Segment/Common 2/3 level voltage	-	$2/3V_{LCDx}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2V_{LCDx}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3V_{LCDx}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4V_{LCDx}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. R_{HN} is the total high value resistive network.
3. R_{LN} is the total low value resistive network.

VLCD external capacitor (STM8AL3L8x only)

The application achieves a stabilized LCD reference voltage when connecting an external capacitor C_{EXT} to the V_{LCD} pin. C_{EXT} is specified in *Table 48*.

In the following table, data are based on characterization results, not tested in production.

Table 54. DAC accuracy

Symbol	Parameter	Conditions	Typ.	Max.(1)	Unit
DNL	Differential non linearity(2)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON(3)	1.5	3	12-bit LSB
		No load DACOUT buffer OFF	1.5	3	
INL	Integral non linearity(4)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON(3)	2	4	
		No load DACOUT buffer OFF	2	4	
Offset	Offset error(5)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON(3)	±10	±25	
		No load DACOUT buffer OFF	±5	±8	
Offset1	Offset error at Code 1 (6)	DACOUT buffer OFF	±1.5	±5	
Gain error	Gain error(7)	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON(3)	+0.1/-0.2	+0.2/-0.5	%
		No load DACOUT buffer OFF	+0/-0.2	+0/-0.4	
TUE	Total unadjusted error	$R_L \geq 5$ kΩ, $C_L \leq 50$ pF DACOUT buffer ON(3)	12	30	12-bit LSB
		No load -DACOUT buffer OFF	8	12	

1. Not tested in production.
2. Difference between two consecutive codes - 1 LSB.
3. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
5. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and (V_{DDA} -0.2) V when buffer is OFF.

Table 56. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA} ≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12000000 / f_{ADC} + t_S			
		16 MHz	1(3)	-	-	
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 49*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. In the RM0031, t_{IDLE} defines the time between 2 conversions, or between ADC ON and the first conversion. t_{IDLE} is not relevant for this device.

In the following three tables, data are guaranteed by characterization result, not tested in production.

Table 57. ADC1 accuracy with V_{DDA} = 3.3 V to 2.5 V

Symbol	Parameter	Conditions	Typ.	Max.(1)	Unit
DNL	Differential non linearity	f_{ADC} = 16 MHz	1	1.6	LSB
		f_{ADC} = 8 MHz	1	1.6	
		f_{ADC} = 4 MHz	1	1.5	
INL	Integral non linearity	f_{ADC} = 16 MHz	1.2	2	
		f_{ADC} = 8 MHz	1.2	1.8	
		f_{ADC} = 4 MHz	1.2	1.7	
TUE	Total unadjusted error	f_{ADC} = 16 MHz	2.2	3.0	
		f_{ADC} = 8 MHz	1.8	2.5	
		f_{ADC} = 4 MHz	1.8	2.3	
Offset	Offset error	f_{ADC} = 16 MHz	1.5	2	LSB
		f_{ADC} = 8 MHz	1	1.5	
		f_{ADC} = 4 MHz	0.7	1.2	
Gain	Gain error	f_{ADC} = 16 MHz	1	1.5	
		f_{ADC} = 8 MHz			
		f_{ADC} = 4 MHz			

1. Guaranteed by characterization results.

Table 58. ADC1 accuracy with V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Typ.	Max.(1)	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	1.7	3	LSB
TUE	Total unadjusted error	2	4	LSB
Offset	Offset error	1	2	LSB
Gain	Gain error	1.5	3	LSB

1. Guaranteed by characterization results.

Table 59. ADC1 accuracy with V_{DDA} = V_{REF}^{+} = 1.8 V to 2.4 V

Symbol	Parameter	Typ.	Max.(1)	Unit
DNL	Differential non linearity	1	2	LSB
INL	Integral non linearity	2	3	LSB
TUE	Total unadjusted error	3	5	LSB

Table 59. ADC1 accuracy with $V_{DDA} = V_{REF}^{+} = 1.8$ V to 2.4 V (continued)

Symbol	Parameter	Typ.	Max.(1)	Unit
Offset	Offset error	2	3	LSB
Gain	Gain error	2	3	LSB

1. Guaranteed by characterization results.

Figure 42. ADC1 accuracy characteristics

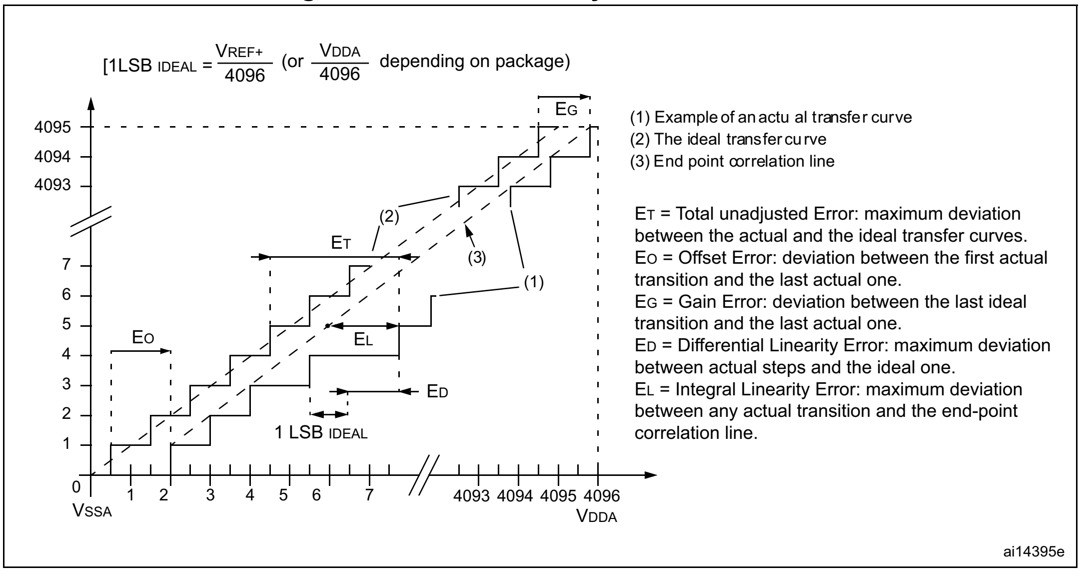
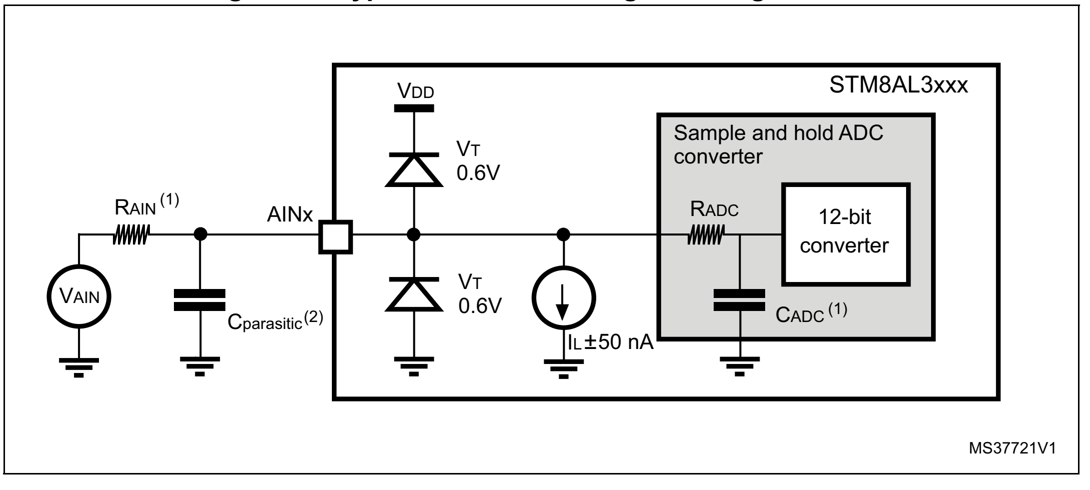


Figure 43. Typical connection diagram using the ADC



1. Refer to *Table 56* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 44* or *Figure 45*, depending on whether V_{REF+} is connected to V_{DDA} or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms to the ANSI/ESDA/JEDEC JS-001, JESD22-A115 and ANSI/ESD S5.3.1.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) are reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress is applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software is hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 60. EMS data

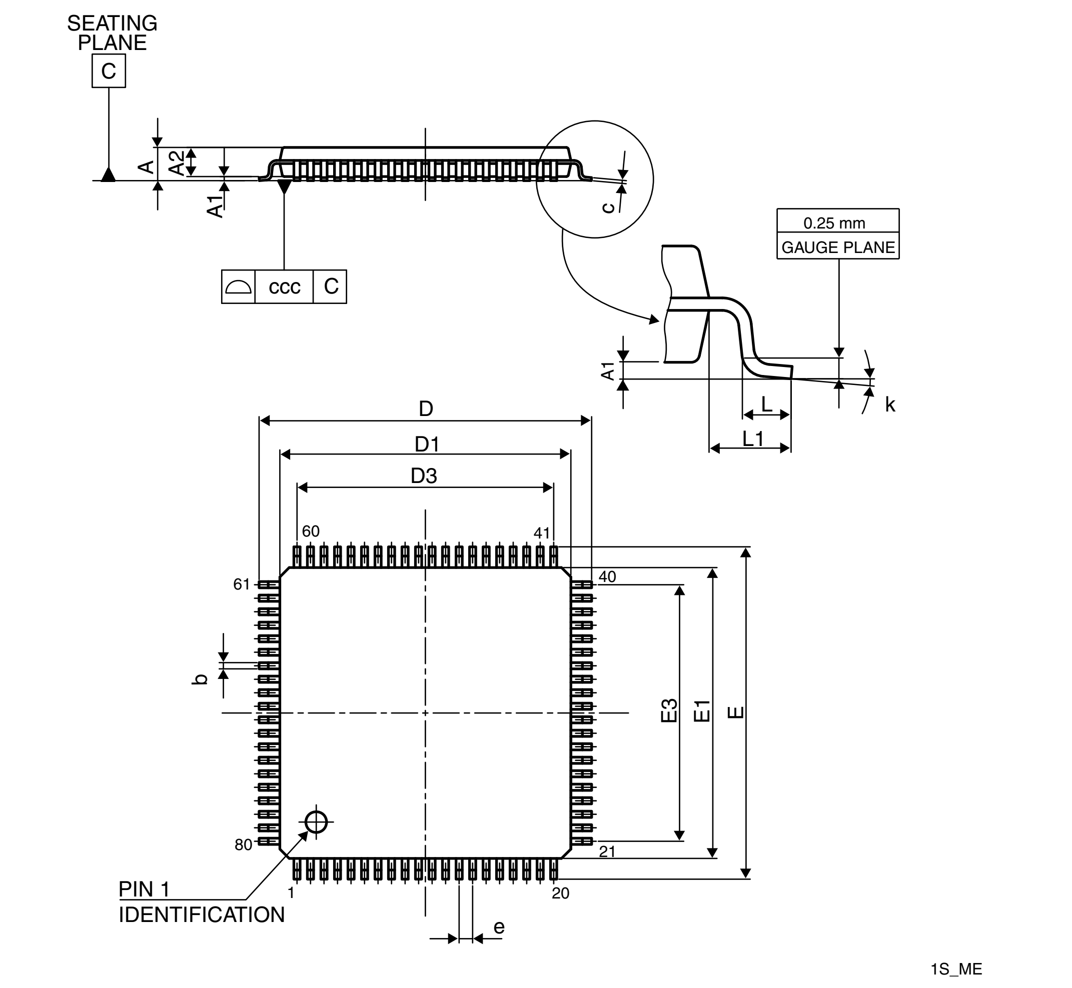
Symbol	Parameter	Conditions		Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU}= 16 MHz, conforms to IEC 61000		2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{CPU} = 16 MHz, conforms to IEC 61000	Using HSI	4A
			Using HSE	2B

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

10.1 LQFP80 package information

Figure 46. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

12 Revision history

Table 69. Document revision history

Date	Revision	Changes
03-Feb-2015	1	Initial release.
22-Apr-2015	2	Added: – *Figure 50: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, – *Figure 48: LQFP80 marking example (package top view)*, – *Figure 51: LQFP64 marking example (package top view)*, – *Figure 54: LQFP48 marking example (package top view)*. Corrected OPT0 default value in *Table 12: Option byte addresses*.
27-Jul-2015	3	Updated – the document confidentiality level to “Public”, – *Table 1: Device summary*, replacing STM8AL318AT with STM8AL318A.
19-Aug-2015	4	Datasheet status changed to “production data”.
1-Dec-2016	5	– Updated *Table 5: High-density STM8AL3x8x pin description*: two pin names changed from PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH3 to PI0/RTC_TAMP1/[SPI2_NSS]/[TIM3_CH1 and from PF2/ADC1_IN26/[SPI2_SCK]/[USART3_SCK] to PF2/ADC1_IN26/[SPI1_SCK]/[USART3_SCK] – Updated device marking part of *Section 10.1: LQFP80 package information*, *Section 10.2: LQFP64 package information* and *Section 10.3: LQFP48 package information* – Updated *Section 9.2: Absolute maximum ratings* – Updated table footnotes in *Chapter 9: Electrical parameters* – Updated *Figure 12: Power supply thresholds*
5-Dec-2016	6	– Updated *Table 5: High-density STM8AL3x8x pin description*: pin name changed from PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP _IN3M/COMP2_INM/COMP1_INP to PC3/USART1_TX/LCD_SEG23(3)/ADC1_IN5/COMP 2_INM/COMP1_INP.