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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8al3l8atcx

List of tables

STM8AL ultra-low-power microcontrollers operates either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8AL ultra-low-power microcontroller families suitable for a wide range of applications.

The devices are offered in three different packages from 48 to 80 pins. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8AL ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the high-density STM8AL3x8x families.

2.2 Device overview

Table 2. High-density STM8AL3x8x low-power device features and peripheral counts

Features		STM8AL3xx8	STM8AL3xx9	STM8AL3xxA
Flash (Kbyte)		64		
Data EEPROM (Kbyte)		2		
LCD		8x28 or 4x32(1)	8x36 or 4x40(1)	8x40 or 4x44(1)
Timers	Basic	1 (8-bit)	1 (8-bit)	1 (8-bit)
	General purpose	3 (16-bit)	3 (16-bit)	3 (16-bit)
	Advanced control	1 (16-bit)	1 (16-bit)	1 (16-bit)
Communication interfaces	SPI	2	2	2
	I2C	1	1	1
	USART	3	3	3
GPIOs		41(2)	54(2)	68(2)
12-bit synchronized ADC (number of channels)		1 (25)	1 (28)	1 (28)
12-Bit DAC Number of channels		2 2	2 2	2 2
Comparators (COMP1/COMP2)		2	2	2
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator		
CPU frequency		16 MHz		
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR		
Operating temperature		-40 to +85 °C / -40 to +125 °C		
Packages		LQFP48	LQFP64	LQFP80

1. STM8AL3L8x versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}, V_{DD1}, V_{SS2}, V_{DD2}, V_{SS3}, V_{DD3}, V_{SS4}, V_{DD4}= 1.65 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD} pins, the corresponding ground pin is V_{SS}. V_{SS1}/V_{SS2}/V_{SS3}/V_{SS4} and V_{DD1}/V_{DD2}/V_{DD3}/V_{DD4} must not be left unconnected.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{REF+}, V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC1/2): external voltage reference for DAC1 and DAC2 must be provided externally through V_{REF+}.

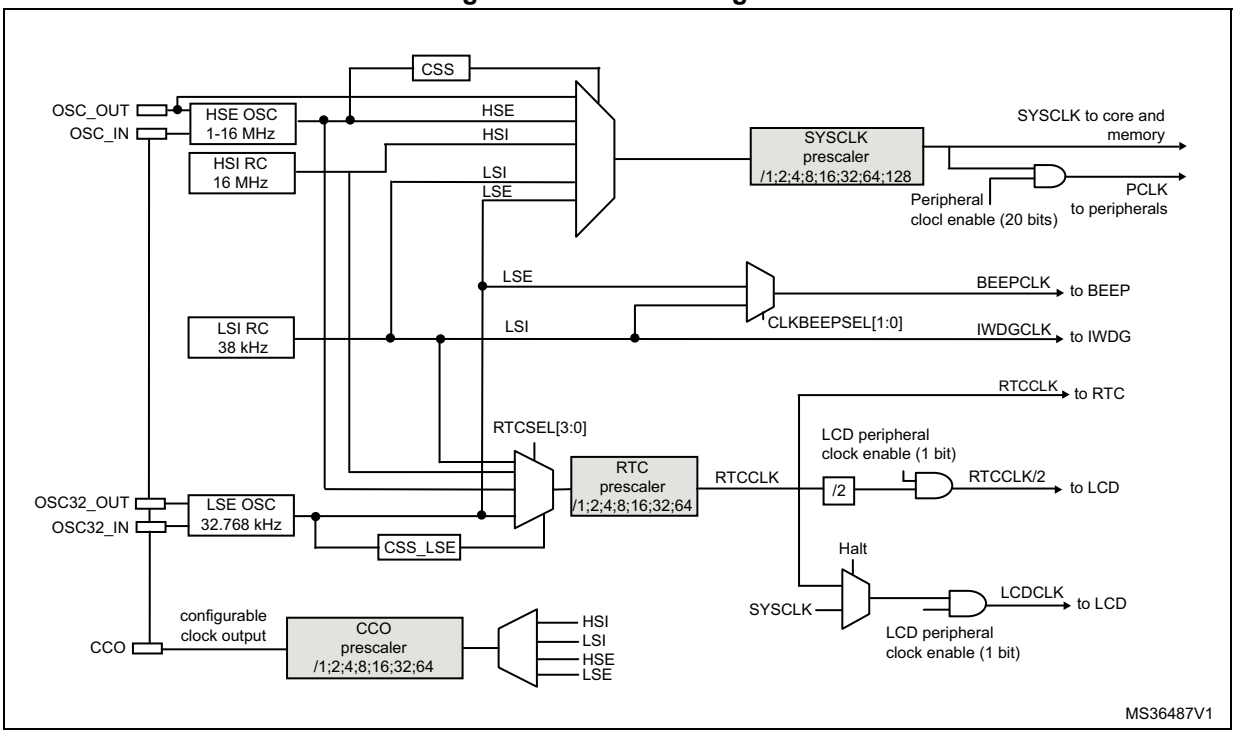
3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. As soon as the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify the default thresholds, or to disable BOR permanently. In this latter case, the V_{DD} min value at power down is 1.65 V.

Five BOR thresholds are available through option byte, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt is generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine generates then a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Figure 2. Clock tree diagram



1. The HSE clock source is either an external crystal/ceramic resonator or an external source (HSE bypass). Refer to Section HSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).
2. The LSE clock source is either an external crystal/ceramic resonator or a external source (LSE bypass). Refer to Section LSE clock in STM8L051/L052 Value Line, STM8L151/L152, STM8L162, STM8AL31, STM8AL3L MCU lines reference manual (RM0031).

3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field is also readable in binary format.

The calendar is adjustable from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time reaches 36 hours
- Periodic alarms based on the calendar are generated from LSE period to every year

A clock security system detects a failure on LSE, and provides an interrupt with wakeup capability. The RTC clock automatically switches to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and wakes-up the MCU.

3.6 LCD (Liquid crystal display)

The LCD is only available on STM8AL3L8x devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. This LCD is configurable to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels programmable to blink.
- The LCD controller operating in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8AL3x8x devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option byte.

The memory supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

Table 4. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	FT: Five-volt tolerant	
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 5. High-density STM8AL3x8x pin description

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	-	-	PH0/LCD SEG 36 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H0**	LCD segment 36
2	-	-	PH1/LCD SEG 37 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H1**	LCD segment 37
3	-	-	PH2/LCD SEG 38 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H2**	LCD segment 38
4	-	-	PH3/LCD SEG 39 (3)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port H3**	LCD segment 39
6	2	2	NRST/PA1(1)	I/O	-	-	**X**	-	HS	X	X	**Reset**	PA1
7	3	3	PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2)	I/O	-	**X**	X	X	HS	X	X	**Port A2**	HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /*
8	4	4	PA3/OSC_OUT/*[USART1 _RX](2)/[SPI1_MOSI](2)*	I/O	-	**X**	X	X	HS	X	X	**Port A3**	HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/*
9	5	5	PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input / */[Timer 2 - trigger] /* LCD COM 0 / ADC1 input 2/Comparator 1 positive input
10	6	6	PA5/TIM3_BKIN/ *[TIM3_ETR](2)*/ LCD_COM1(3)/ADC1_IN1/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input / *[Timer 3 - trigger] /* LCD_COM 1 / ADC1 input 1/Comparator 1 positive input
11	7	7	PA6/ADC1_TRIG/ LCD_COM2(3)/ADC1_IN0/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port A6**	ADC1 - trigger / LCD_COM2 / ADC1 input 0/Comparator 1 positive input

Table 5. High-density STM8AL3x8x pin description (continued)

Pin number			Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64	LQFP48				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
45	37	-	PB6/SPI1_MOSI/ LCD_SEG16(3)/ ADC1_IN12/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/Comparator 1 positive input
-	-	30	PB6/SPI1_MOSI/ LCD_SEG16(3)/ ADC1_IN12/DAC_OUT2/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B6**	SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/Comparator 1 positive input
46	38	31	PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port B7**	SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/Comparator 1 positive input
65	53	37	PC0/I2C1_SDA	I/O	FT(5)	**X**		X		T(6)	-	**Port C0**	I2C1 data
66	54	38	PC1/I2C1_SCL	I/O	FT(5)	**X**		X		T(6)	-	**Port C1**	I2C1 clock
69	57	41	PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ COMP1_INP/VREFINT	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C2**	USART1 receive / LCD segment 22 / ADC1_IN6/Comparator 1 positive input/Internal reference voltage output
-	-	42	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5
70	58	-	PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5/COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C3**	USART1 transmit / LCD segment 23 / ADC1_IN5 / Comparator 2 negative input /Comparator 1 input positive
71	59	43	PC4/USART1_CK/ I2C1_SMB/CCO/ LCD_SEG24(3)/ ADC1_IN4/COMP2_INM/ COMP1_INP	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C4**	USART1 synchronous clock / I2C1_SMB / Configurable clock output / LCD segment 24 / ADC1_IN4 / Comparator 2 negative input / Comparator 1 positive input
72	60	44	PC5/OSC32_IN /*[SPI1_NSS]*(2)/ *[USART1_TX]*(2)	I/O	FT(5)	**X**	X	X	HS	X	X	**Port C5**	LSE oscillator input / *[SPI1 master/slave select] / [USART1 transmit]*

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier are never altered by the user.

The unique device identifier is read in single byte and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 14. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

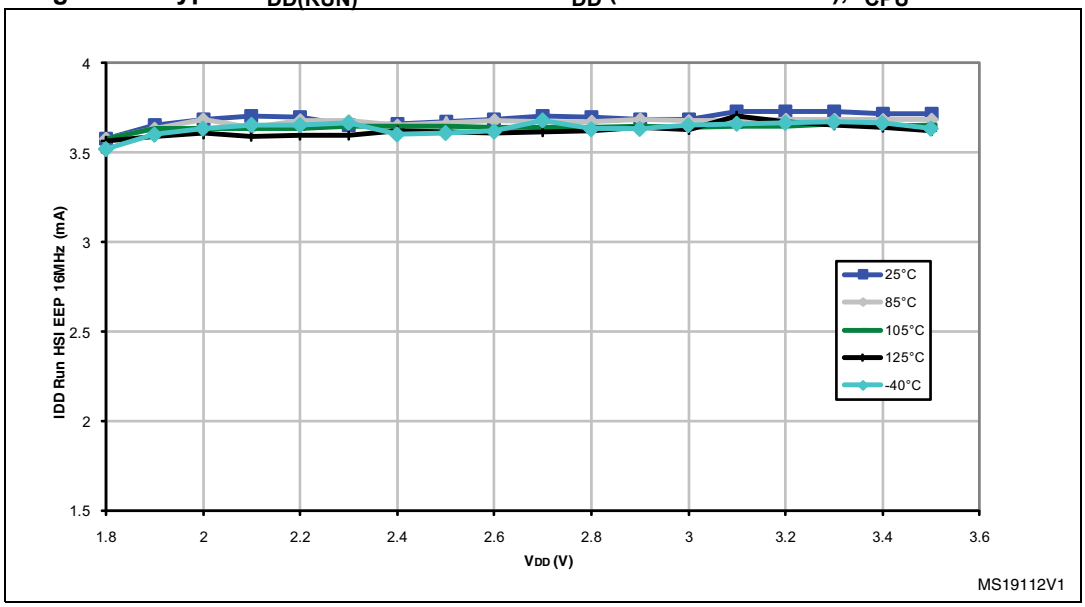
- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

General conditions for V_{DD} apply, TA = -40 °C to 125 °C.

Table 21. Total current consumption in Run mode

Symbol	Parameter	Conditions			Typ.	Max.	Unit
$I_{DD(RUN)}$	Supply current in run mode(1)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(2)	f_{CPU} = 125 kHz	0.40	0.55(3)	mA
				f_{CPU} = 1 MHz	0.50	0.65(3)	
				f_{CPU} = 4 MHz	0.75	1.00(3)	
				f_{CPU} = 8 MHz	1.10	1.40(3)	
				f_{CPU} = 16 MHz	1.85	2.35	
			HSE external clock (f_{CPU}=f_{HSE})(4)	f_{CPU} = 125 kHz	0.07	0.20(3)	
				f_{CPU} = 1 MHz	0.20	0.25(3)	
				f_{CPU} = 4 MHz	0.55	0.75(3)	
				f_{CPU} = 8 MHz	1.00	1.25(3)	
				f_{CPU} = 16 MHz	1.90	2.30(3)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	40	50(3)	µA
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	40	60(3)	
$I_{DD(RUN)}$	Supply current in Run mode	All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	HSI RC osc.(5)	f_{CPU} = 125 kHz	0.45	0.60(3)	mA
				f_{CPU} = 1 MHz	0.60	0.85(3)	
				f_{CPU} = 4 MHz	1.10	1.45(3)	
				f_{CPU} = 8 MHz	1.90	2.40(3)	
				f_{CPU} = 16 MHz	3.80	4.90	
			HSE external clock (f_{CPU}=f_{HSE}) (4)	f_{CPU} = 125 kHz	0.30	0.45(3)	
				f_{CPU} = 1 MHz	0.40	0.55(3)	
				f_{CPU} = 4 MHz	1.15	1.50(3)	
				f_{CPU} = 8 MHz	2.15	2.75(3)	
				f_{CPU} = 16 MHz	4.00	4.75(3)	
			LSI RC osc.	f_{CPU} = f_{LSI}	100	150(3)	µA
			LSE external clock (32.768 kHz)(6)	f_{CPU} = f_{LSE}	100	120(3)	

Figure 14. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz(1)



1. Typical current consumption measured with code executed from Flash.

LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8AL318x devices only.

Subject to general operating conditions for V_{DD} and T_A.

Table 31. LSE external clock characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high-level voltage	$0.7xV_{DD}$(1)	-	V_{DD}(1)	V
V_{LSEL}	OSC32_IN input pin low-level voltage	V_{SS}(1)		$0.3xV_{DD}$(1)	
$C_{in(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF
I_{LEAK_LSE}	OSC32_IN input leakage current	-	-	±500	nA

1. Guaranteed by characterization results.

HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 32. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE}	High speed external oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$C^{(1)(2)}$	Recommended load capacitance	-	-	20	-	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} =16 MHz	-	-	2.5 (startup) 0.46 (stabilized)(3)	
g_m	Oscillator transconductance	-	3.5(3)	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		1	-	ms

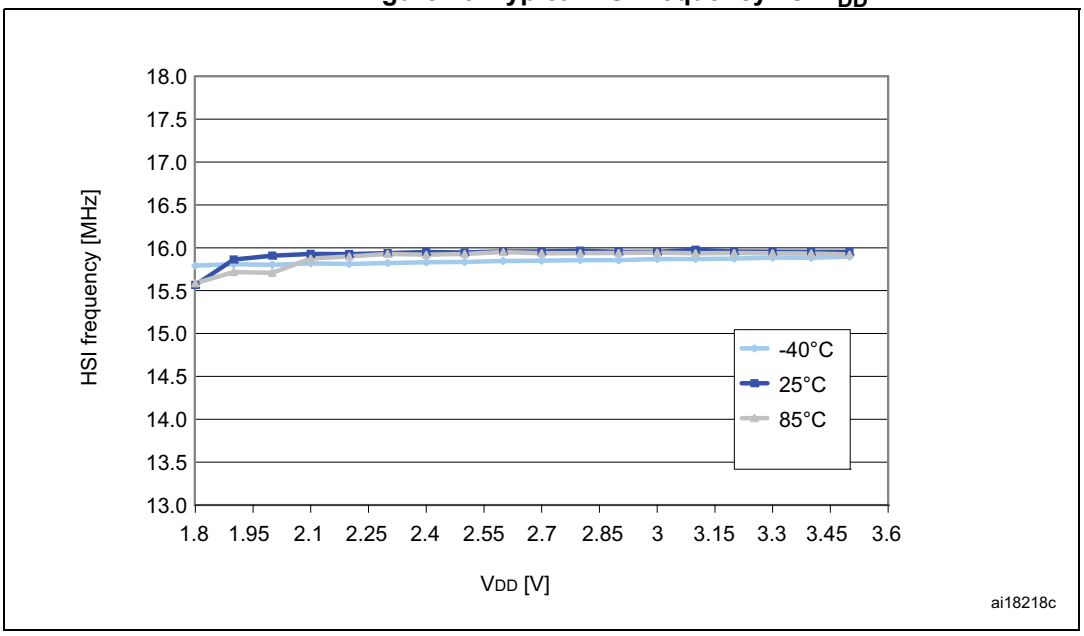
1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it varies significantly with the crystal manufacturer.

Table 34. HSI oscillator characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1	-	1	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} ≤1.8 V≤ V_{DD} ≤ 3.6 V -40 °C ≤T_A ≤ 125 °C	-5	-	5	
TRIM	HSI user trimming step(2)	Trimming code ≠ multiple of 16	-	0.4	0.7(2)	%
		Trimming code = multiple of 16	-	-	± 1.5(2)	
$t_{su(HSI)}$	HSI oscillator setup time (wakeup time)	-	-	3.7	6 (3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	100	140(3)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.
3. Guaranteed by design.

Figure 23. Typical HSI frequency vs. V_{DD}



NRST pin

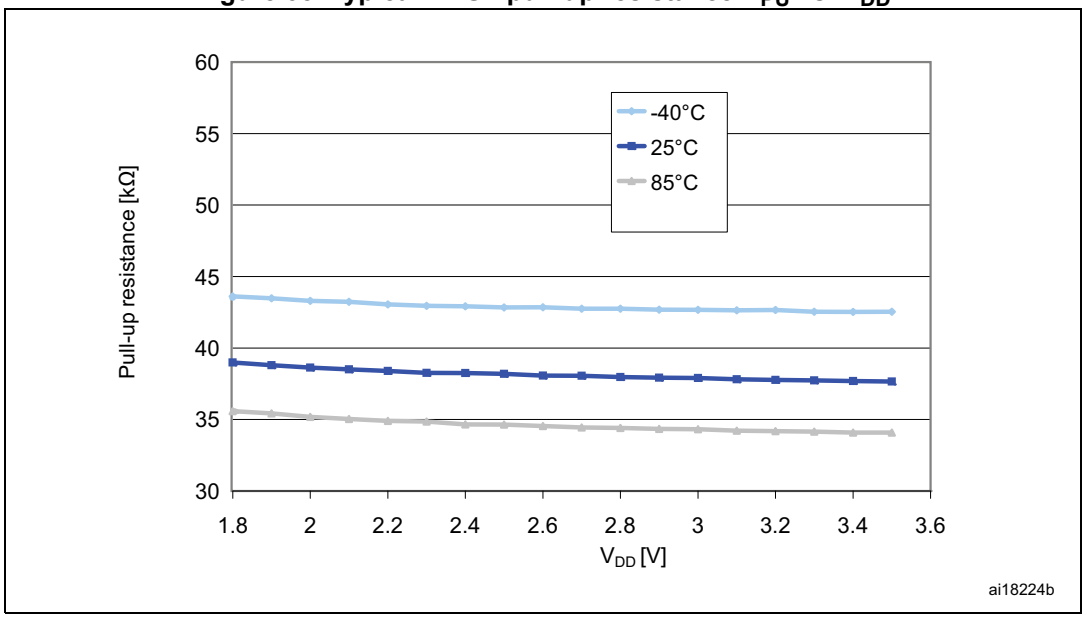
Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 45. $\overline{\text{NRST}}$ pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage	-	V_{SS}(1)	-	0.8(1)	V
$V_{IH(NRST)}$	NRST input high-level voltage (1)	-	1.4(1)	-	V_{DD}(1)	
$V_{OL(NRST)}$	NRST output low-level voltage (1)	I_{OL} = 2 mA for 2.7 V ≤V_{DD} ≤3.6 V	-	-	0.4(1)	
		I_{OL} = 1.5 mA for V_{DD} < 2.7 V	-	-		
V_{HYST}	NRST input hysteresis	-	10%V_{DD} (2)(3)	-	-	mV
$R_{PU(NRST)}$	NRST pull-up equivalent resistor	-	30(1)	45	60(1)	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	50(3)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	300(3)	-	-	

1. Guaranteed by characterization results.
2. 200 mV min.
3. Guaranteed by design.

Figure 35. Typical NRST pull-up resistance R_{PU} vs. V_{DD}



9.3.10 Embedded reference voltage

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 49. Reference voltage characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{REFINT}	Internal reference voltage consumption	-	-	1.4	-	µA
$T_{S\_VREFINT}$(1)(2)	ADC sampling time when reading the internal reference voltage	-	-	5	10	µs
I_{BUF}(1)	Internal reference voltage buffer consumption (used for ADC)	-	-	13.5	25	µA
$V_{REFINT\ out}$	Reference voltage output	-	1.202 (3)	1.224	1.242 (3)	V
I_{LPBUF}(1)	Internal reference voltage low-power buffer consumption (used for comparators or output)	-	-	730	1200	nA
I_{REFOUT}(1)(4)	Buffer output current	-	-	-	1	µA
C_{REFOUT}	Reference voltage output load	-	-	-	50	pF
$t_{VREFINT}$(1)	Internal reference voltage startup time	-	-	2	3	ms
t_{BUFEN}(1)(2)	Internal reference voltage buffer startup time once enabled	-	-	-	10	µs
$ACC_{VREFINT}$(5)	Accuracy of V_{REFINT} stored in the VREFINT_Factory_CONV byte	-	-	-	± 5	mV
$STAB_{VREFINT}$	Stability of V_{REFINT} over temperature	-40 °C ≤T_A ≤ 125 °C	-	20	50	ppm/°C
	Stability of V_{REFINT} over temperature	0 °C ≤T_A ≤ 50 °C	-	-	20	ppm/°C
$STAB_{VREFINT}$	Stability of V_{REFINT} after 1000 hours	-	-	-	TBD	ppm

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at V_{DD} = 3 V ±10 mV.
4. To guarantee less than 1% V_{REFOUT} deviation
5. Measured at V_{DD} = 3 V ±10 mV. This value takes into account V_{DD} accuracy and ADC conversion accuracy.

9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design, not tested in production.

Table 53. DAC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	-	1.8	-	V_{DDA}	
I_{VREF}	Current consumption on V_{REF+} supply	V_{REF+} = 3.3 V, no load, middle code (0x800)	-	130	220	µA
		V_{REF+} = 3.3 V, no load, worst code (0x000)	-	220	350	
I_{VDDA}	Current consumption on V_{DDA} supply	V_{DDA} = 3.3 V, no load, middle code (0x800)	-	210	320	
		V_{DDA} = 3.3 V, no load, worst code (0x000)	-	320	520	
T_A	Temperature range	-	-40	-	125	°C
R_L (1) (2)	Resistive load	DACOUT buffer ON	5	-		kΩ
R_O	Output impedance	DACOUT buffer OFF	-	8	10	kΩ
C_L (3)	Capacitive load	-	-	-	50	pF
DAC_OUT (4)	DAC_OUT voltage	DACOUT buffer ON	0.2	-	V_{DDA} - 0.2	V
		DACOUT buffer OFF	0	-	V_{REF+} -1 LSB	V
$t_{settling}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB)	R_L ≥5 kΩ, C_L≤ 50 pF	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB).	R_L ≥ 5 kΩ, C_L ≤50 pF	-	-	1	Msps
t_{WAKEUP}	Wakeup time from OFF state. Input code between lowest and highest possible codes.	R_L ≥5 kΩ, C_L≤50 pF	-	9	15	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	R_L≥ 5 kΩ, C_L≤50 pF	-	-60	-35	dB

1. Resistive load between DACOUT and GNDA
2. Output on PF0 or PF1
3. Capacitive load at DACOUT pin
4. It gives the output excursion of the DAC

In the following table, data are guaranteed by design, not tested in production.

Table 55. DAC output on PB4-PB5-PB6(1)

Symbol	Parameter	Conditions	Max	Unit
R_{int}	Internal resistance between DAC output and PB4-PB5-PB6 output	2.7 V < V_{DD} < 3.6 V	1.4	kΩ
		2.4 V < V_{DD} < 3.6 V	1.6	
		2.0 V < V_{DD} < 3.6 V	3.2	
		1.8 V < V_{DD} < 3.6 V	8.2	

1. 32 or 28-pin packages only. The DAC channel is routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

Table 67. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.