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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2926fbd144-551

Table 3. LQFP144 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
$V_{SS(CORE)}$	59	ground for digital core			
$V_{DD(CORE)}$	60	1.8 V power supply for digital core			
P3[13]/SDO1/ EI5/IDX0	61[1]	GPIO3, pin 13	SPI1 SDO	EXTINT5	QEI0 IDX
P2[4]/MAT1[0]/ EI0/D12	62[1]	GPIO2, pin 4	TIMER1 MAT0	EXTINT0	EXTBUS D12
P2[5]/MAT1[1]/ EI1/D13	63[1]	GPIO2, pin 5	TIMER1 MAT1	EXTINT1	EXTBUS D13
P1[9]/SDO1/ RXDL1/$\overline{CS1}$	64[1]	GPIO1, pin 9	SPI1 SDO	LIN1 RXD/UART RXD	EXTBUS $\overline{CS1}$
$V_{SS(IO)}$	65	ground for I/O			
P1[8]/SCS1[0]/ TXDL1/$\overline{CS0}$	66[1]	GPIO1, pin 8	SPI1 SCS0	LIN1 TXD/UART TXD	EXTBUS $\overline{CS0}$
P1[7]/SCS1[3]/RXD1/ A7	67[1]	GPIO1, pin 7	SPI1 SCS3	UART1 RXD	EXTBUS A7
P1[6]/SCS1[2]/ TXD1/A6	68[1]	GPIO1, pin 6	SPI1 SCS2	UART1 TXD	EXTBUS A6
P2[6]/MAT1[2]/ EI2/D14	69[1]	GPIO2, pin 6	TIMER1 MAT2	EXTINT2	EXTBUS D14
P1[5]/SCS1[1]/PMAT 3[5]/A5	70[1]	GPIO1, pin 5	SPI1 SCS1	PWM3 MAT5	EXTBUS A5
P1[4]/SCS2[2]/PMAT 3[4]/A4	71[1]	GPIO1, pin 4	SPI2 SCS2	PWM3 MAT4	EXTBUS A4
$\overline{TRST}$	72[1]	IEEE 1149.1 test reset NOT; active LOW; pulled up internally			
$\overline{RST}$	73[1]	asynchronous device reset; active LOW; pulled up internally			
$V_{SS(OSC)}$	74	ground for oscillator			
XOUT_OSC	75[3]	crystal out for oscillator			
XIN_OSC	76[3]	crystal in for oscillator			
$V_{DD(OSC\_PLL)}$	77	1.8 V supply for oscillator and PLL			
$V_{SS(PLL)}$	78	ground for PLL			
P2[7]/MAT1[3]/ EI3/D15	79[1]	GPIO2, pin 7	TIMER1 MAT3	EXTINT3	EXTBUS D15
P3[14]/SDI1/ EI6/TXDC0	80[1]	GPIO3, pin 14	SPI1 SDI	EXTINT6	CAN0 TXD
P3[15]/SCK1/ EI7/RXDC0	81[1]	GPIO3, pin 15	SPI1 SCK	EXTINT7	CAN0 RXD
$V_{DD(IO)}$	82	3.3 V power supply for I/O			
P2[8]/CLK_OUT/ PMAT0[0]/SCS0[2]	83[1]	GPIO2, pin 8	CLK_OUT	PWM0 MAT0	SPI0 SCS2
P2[9]/ $\overline{USB\_UP\_LED}$/ PMAT0[1]/ SCS0[1]	84[1]	GPIO2, pin 9	$\overline{USB\_UP\_LED}$	PWM0 MAT1	SPI0 SCS1

6.6 Reset, debug, test, and power description

6.6.1 Reset and power-up behavior

The LPC2926/2927/2929 contains external reset input and internal power-up reset circuits. This ensures that a reset is extended internally until the oscillators and flash have reached a stable state. See Section 8 for trip levels of the internal power-up reset circuit[1]. See Section 9 for characteristics of the several start-up and initialization times. Table 4 shows the reset pin.

Table 4. Reset pin

Symbol	Direction	Description
$\overline{\text{RST}}$	IN	external reset input, active LOW; pulled up internally

At activation of the $\overline{\text{RST}}$ pin the JTAGSEL pin is sensed as logic LOW. If this is the case the LPC2926/2927/2929 is assumed to be connected to debug hardware, and internal circuits re-program the source for the BASE_SYS_CLK to be the crystal oscillator instead of the Low-Power Ring Oscillator (LP_OSC). This is required because the clock rate when running at LP_OSC speed is too low for the external debugging environment.

6.6.2 Reset strategy

The LPC2926/2927/2929 contains a central module, the Reset Generator Unit (RGU) in the Power, Clock and Reset Subsystem (PCRSS), which controls all internal reset signals towards the peripheral modules. The RGU provides individual reset control as well as the monitoring functions needed for tracing a reset back to source.

6.6.3 IEEE 1149.1 interface pins (JTAG boundary scan test)

The LPC2926/2927/2929 contains boundary-scan test logic according to IEEE 1149.1, also referred to in this document as Joint Test Action Group (JTAG). The boundary-scan test pins can be used to connect a debugger probe for the embedded ARM processor. Pin JTAGSEL selects between boundary-scan mode and debug mode. Table 5 shows the boundary scan test pins.

Table 5. IEEE 1149.1 boundary-scan test and debug interface

Symbol	Description
JTAGSEL	TAP controller select input. LOW level selects ARM debug mode and HIGH level selects boundary scan and flash programming; pulled up internally
$\overline{\text{TRST}}$	test reset input; pulled up internally (active LOW)
TMS	test mode select input; pulled up internally
TDI	test data input, pulled up internally
TDO	test data output
TCK	test clock input

1. Only for 1.8 V power sources

Table 11. External memory-bank address bit description

32-bit system address bit field	Symbol	Description
31 to 29	BA[2:0]	external static-memory base address (three most significant bits); the base address can be found in the memory map; see Ref. 1. This field contains '010' when addressing an external memory bank.
28 to 26	CS[2:0]	chip select address space for eight memory banks; see Ref. 1.
25 and 24	-	always '00'; other values are 'mirrors' of the 16 MB bank address.
23 to 0	A[23:0]	16 MB memory banks address space

Table 12. External static-memory controller banks

CS[2:0]	Bank
000	bank 0
001	bank 1
010	bank 2
011	bank 3
100	bank 4
101	bank 5
110	bank 6
111	bank 7

6.9.2 Pin description

The external static-memory controller module in the LPC2926/2927/2929 has the following pins, which are combined with other functions on the port pins of the LPC2926/2927/2929. Table 13 shows the external memory controller pins.

Table 13. External memory controller pins

Symbol	Pin name	Direction	Description
EXTBUS $\overline{CSx}$	CSx	OUT	memory-bank x select, x runs from 0 to 7
EXTBUS $\overline{BLSy}$	$\overline{BLSy}$	OUT	byte-lane select input y, y runs from 0 to 3
EXTBUS $\overline{WE}$	$\overline{WE}$	OUT	write enable (active LOW)
EXTBUS $\overline{OE}$	OE	OUT	output enable (active LOW)
EXTBUS A[23:0]	A[23:0]	OUT	address bus
EXTBUS D[31:0]	D[31:0]	IN/OUT	data bus

6.9.3 Clock description

The External Static Memory Controller is clocked by CLK_SYS_SMC, see Section 6.7.2.

6.9.4 External memory timing diagrams

A timing diagram for reading from external memory is shown in Figure 5. The relationship between the wait-state settings is indicated with arrows.

Table 18. SPI pins *…continued*

Symbol	Pin name	Direction	Description
SPIx SCK	SCKx	IN/OUT	SPIx clock[1]
SPIx SDI	SDIx	IN	SPIx data input
SPIx SDO	SDOx	OUT	SPIx data output

[1] Direction of SPIx SCS and SPIx SCK pins depends on master or slave mode. These pins are output in master mode, input in slave mode.

[2] In slave mode there is only one chip select input pin, SPIx SCS0. The other chip selects have no function in slave mode.

6.13.5.3 Clock description

The SPI modules are clocked by two different clocks; CLK_SYS_PESS and CLK_SPIx (x = 0, 1, 2), see Section 6.7.2. Note that each SPI has its own CLK_SPIx branch clock for power management. The frequency of all clocks CLK_SPIx is identical as they are derived from the same base clock BASE_CLK_SPI. The register interface towards the system bus is clocked by CLK_SYS_PESS. The serial-clock rate divisor is clocked by CLK_SPIx.

The SPI clock frequency can be controlled by the CGU. In master mode the SPI clock frequency (CLK_SPIx) must be set to at least twice the SPI serial clock rate on the interface. In slave mode CLK_SPIx must be set to four times the SPI serial clock rate on the interface.

6.13.6 General-purpose I/O

The LPC2926/2927/2929 contains four general-purpose I/O ports located at different peripheral base addresses. In the 144-pin package all four ports are available. All I/O pins are bidirectional, and the direction can be programmed individually. The I/O pad behavior depends on the configuration programmed in the port function-select registers.

The key features are:

- General-purpose parallel inputs and outputs
- Direction control of individual bits
- Synchronized input sampling for stable input-data values
- All I/O defaults to input at reset to avoid any possible bus conflicts

6.13.6.1 Functional description

The general-purpose I/O provides individual control over each bidirectional port pin. There are two registers to control I/O direction and output level. The inputs are synchronized to achieve stable read-levels.

To generate an open-drain output, set the bit in the output register to the desired value. Use the direction register to control the signal. When set to output, the output driver actively drives the value on the output: when set to input the signal floats and can be pulled up internally or externally.

6.13.6.2 Pin description

The five GPIO ports in the LPC2926/2927/2929 have the pins listed below. The GPIO pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 19 shows the GPIO pins.

Figure 8 provides an overview of the MSCSS. An AHB-to-APB bus bridge takes care of communication with the AHB system bus. Two internal timers are dedicated to this subsystem. MSCSS timer 0 can be used to generate start pulses for the ADCs and the first PWM. The second timer (MSCSS timer 1) is used to generate ‘carrier’ signals for the PWMs. These carrier patterns can be used, for example, in applications requiring current control. Several other trigger possibilities are provided for the ADCs (external, cascaded or following a PWM). The capture inputs of both timers can also be used to capture the start pulse of the ADCs.

The PWMs can be used to generate waveforms in which the frequency, duty cycle and rising and falling edges can be controlled very precisely. Capture inputs are provided to measure event phases compared to the main counter. Depending on the applications, these inputs can be connected to digital sensor motor outputs or digital external signals. Interrupt signals are generated on several events to closely interact with the CPU.

The ADCs can be used for any application needing accurate digitized data from analog sources. To support applications like motor control, a mechanism to synchronize several PWMs and ADCs is available (sync_in and sync_out).

Note that the PWMs run on the PWM clock and the ADCs on the ADC clock, see Section 6.16.2.

Table 23. ADC pins

Symbol	Pin name	Direction	Description
ADC0 IN[7:0]	IN0[7:0]	IN	analog input for 5.0 V ADC0, channel 7 to channel 0.
ADC1/2 IN[7:0]	IN1/2[7:0]	IN	analog input for 3.3 V ADC1/2, channel 7 to channel 0.
ADC2_EXT_START	CAP1[2]	IN	ADC external start-trigger input.
VREFN	VREFN	IN	ADC LOW reference level.
VREFP	VREFP	IN	ADC HIGH reference level.
$V_{DDA(ADC5V0)}$	$V_{DDA(ADC5V0)}$[1]	IN	5 V high-power supply and HIGH reference for ADC0. Connect to clean 5 V as HIGH reference. May also be connected to 3.3 V if 3.3 V measurement range for ADC0 is needed.[2][3]
$V_{DDA(ADC3V3)}$	$V_{DDA(ADC3V3)}$	IN	ADC1 and ADC2 3.3 V supply (also used for ADC0).[3]

[1] VREFP, VREFN, $V_{DDA(ADC3V3)}$ must be connected for the 5 V ADC0 to operate properly.

[2] The analog inputs of ADC0 are internally multiplied by a factor of 3.3 / 5. If $V_{DDA(ADC5V0)}$ is connected to 3.3 V, the maximum digital result is 1024 × 3.3 / 5.

[3] $V_{DDA(ADC5V0)}$ and $V_{DDA(ADC3V3)}$ must be set as follows: $V_{DDA(ADC5V0)} = V_{DDA(ADC3V3)} \times 1.5$.

Remark: The following formula only applies to ADC0:

Voltage variations on VREFP (i.e. those that deviate from voltage variations on the $V_{DDA(ADC5V5)}$ pin) are visible as variations in the measurement result. The following formula is used to determine the conversion result of an input voltage V_I on ADC0:

$$\left(\frac{2}{3}\left(V_I - \frac{1}{2}V_{DDA(ADC5V0)}\right) + \frac{1}{2}V_{DDA(ADC3V3)}\right) \times \frac{1024}{V_{VREFP} - V_{VREFN}} \quad (3)$$

Remark: Note that the ADC1 and ADC2 accept an input voltage up to of 3.6 V (see Table 34) on the ADC1/2 IN pins. If the ADC is not used, the pins are 5 V tolerant. The ADC0 pins are 5 V tolerant.

6.15.4.3 Clock description

The ADC modules are clocked from two different sources; CLK_MSCSS_ADCx_APB and CLK_ADCx (x = 0, 1, or 2), see Section 6.7.2. Note that each ADC has its own CLK_ADCx and CLK_MSCSS_ADCx_APB branch clocks for power management. If an ADC is unused both its CLK_MSCSS_ADCx_APB and CLK_ADCx can be switched off.

The frequency of all the CLK_MSCSS_ADCx_APB clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK. Likewise the frequency of all the CLK_ADCx clocks is identical since they are derived from the same base clock BASE_ADC_CLK.

The register interface towards the system bus is clocked by CLK_MSCSS_ADCx_APB. Control logic for the analog section of the ADC is clocked by CLK_ADCx, see also Figure 9.

6.15.5 Pulse Width Modulator (PWM)

The MSCSS in the LPC2926/2927/2929 includes four PWM modules with the following features.

- Six pulse-width modulated output signals
- Double edge features (rising and falling edges programmed individually)
- Optional interrupt generation on match (each edge)
- Different operation modes: continuous or run-once
- 16-bit PWM counter and 16-bit prescale counter allow a large range of PWM periods
- A protective mode (TRAP) holding the output in a software-controllable state and with optional interrupt generation on a trap event
- Three capture registers and capture trigger pins with optional interrupt generation on a capture event
- Interrupt generation on match event, capture event, PWM counter overflow or trap event
- A burst mode mixing the external carrier signal with internally generated PWM
- Programmable sync-delay output to trigger other PWM modules (master/slave behavior)

6.15.5.1 Functional description

The ability to provide flexible waveforms allows PWM blocks to be used in multiple applications; e.g. dimmer/lamp control and fan control. Pulse-width modulation is the preferred method for regulating power since no additional heat is generated, and it is energy-efficient when compared with linear-regulating voltage control networks.

The PWM delivers the waveforms/pulses of the desired duty cycles and cycle periods. A very basic application of these pulses can be in controlling the amount of power transferred to a load. Since the duty cycle of the pulses can be controlled, the desired amount of power can be transferred for a controlled duration. Two examples of such applications are:

- Dimmer controller: The flexibility of providing waves of a desired duty cycle and cycle period allows the PWM to control the amount of power to be transferred to the load. The PWM functions as a dimmer controller in this application.
- Motor controller: The PWM provides multi-phase outputs, and these outputs can be controlled to have a certain pattern sequence. In this way the force/torque of the motor can be adjusted as desired. This makes the PWM function as a motor drive.

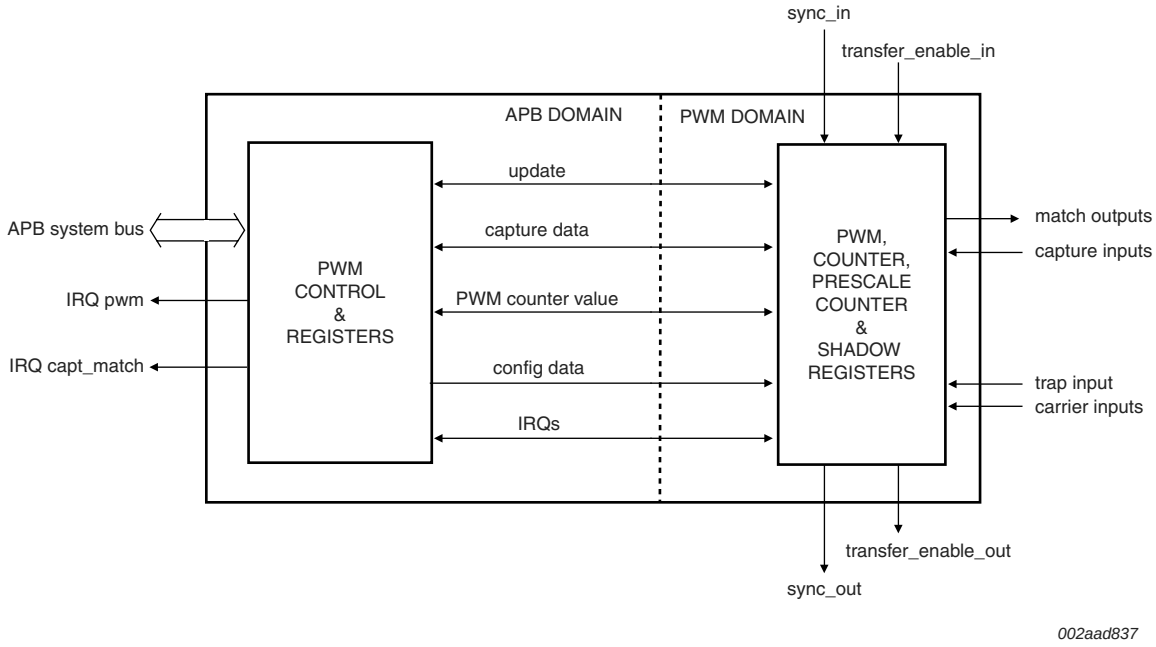


Fig 10. PWM block diagram

The PWM block diagram in Figure 10 shows the basic architecture of each PWM. PWM functionality is split into two major parts, a APB domain and a PWM domain, both of which run on clocks derived from the BASE_MSCSS_CLK. This split into two domains affects behavior from a system-level perspective. The actual PWM and prescale counters are located in the PWM domain but system control takes place in the APB domain.

The actual PWM consists of two counters; a 16-bit prescale counter and a 16-bit PWM counter. The position of the rising and falling edges of the PWM outputs can be programmed individually. The prescale counter allows high system bus frequencies to be scaled down to lower PWM periods. Registers are available to capture the PWM counter values on external events.

Note that in the Modulation and Sampling SubSystem, each PWM has its individual clock source CLK_MSCSS_PWMx (x runs from 0 to 3). Both the prescale and the timer counters within each PWM run on this clock CLK_MSCSS_PWMx, and all time references are related to the period of this clock. See Section 6.16 for information on generation of these clocks.

6.15.5.2 Synchronizing the PWM counters

A mechanism is included to synchronize the PWM period to other PWMs by providing a sync input and a sync output with programmable delay. Several PWMs can be synchronized using the trans_enable_in/trans_enable_out and sync_in/sync_out ports. See Figure 8 for details of the connections of the PWM modules within the MSCSS in the LPC2926/2927/2929. PWM 0 can be master over PWM 1; PWM 1 can be master over PWM 2, etc.

6.15.5.3 Master and slave mode

A PWM module can provide synchronization signals to other modules (also called Master mode). The signal sync_out is a pulse of one clock cycle generated when the internal PWM counter (re)starts. The signal trans_enable_out is a pulse synchronous to sync_out, generated if a transfer from system registers to PWM shadow registers occurred when the PWM counter restarted. A delay may be inserted between the counter start and generation of trans_enable_out and sync_out.

A PWM module can use input signals trans_enable_in and sync_in to synchronize its internal PWM counter and the transfer of shadow registers (Slave mode).

6.15.5.4 Pin description

Each of the four PWM modules in the MSCSS has the following pins. These are combined with other functions on the port pins of the LPC2926/2927/2929. Table 24 shows the PWM0 to PWM3 pins.

Table 24. PWM pins

Symbol	Pin name	Direction	Description
PWMn CAP[0]	PCAPn[0]	IN	PWM n capture input 0
PWMn CAP[1]	PCAPn[1]	IN	PWM n capture input 1
PWMn CAP[2]	PCAPn[2]	IN	PWM n capture input 2
PWMn MAT[0]	PMATn[0]	OUT	PWM n match output 0
PWMn MAT[1]	PMATn[1]	OUT	PWM n match output 1
PWMn MAT[2]	PMATn[2]	OUT	PWM n match output 2
PWMn MAT[3]	PMATn[3]	OUT	PWM n match output 3
PWMn MAT[4]	PMATn[4]	OUT	PWM n match output 4
PWMn MAT[5]	PMATn[5]	OUT	PWM n match output 5
PWMn TRAP	TRAPn	IN	PWM n trap input

6.15.5.5 Clock description

The PWM modules are clocked by CLK_MSCSS_PWMx (x = 0 to 3), see Section 6.7.2. Note that each PWM has its own CLK_MSCSS_PWMx branch clock for power management. The frequency of all these clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

Also note that unlike the timer modules in the Peripheral SubSystem, the actual timer counter registers of the PWM modules run at the same clock as the APB system interface CLK_MSCSS_APB. This clock is independent of the AHB system clock.

If a PWM module is not used its CLK_MSCSS_PWMx branch clock can be switched off.

6.15.6 Timers in the MSCSS

The two timers in the MSCSS are functionally identical to the timers in the peripheral subsystem, see Section 6.13.3. The features of the timers in the MSCSS are the same as the timers in the peripheral subsystem, but the capture inputs and match outputs are not available on the device pins. These signals are instead connected to the ADC and PWM modules as outlined in the description of the MSCSS, see Section 6.15.1.

See Section 6.13.3 for a functional description of the timers.

Table 33. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
ESD						
V_{ESD}	electrostatic discharge voltage	on all pins				
		human body model	[9]	−2000	+2000	V
		charged device model		−500	+500	V
		on corner pins				
		charged device model		−750	+750	V

[1] Based on package heat transfer, not device power consumption.

[2] Peak current must be limited at 25 times average current.

[3] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[4] Only when $V_{DD(IO)}$ is present.

[5] Note that pull-up should be off. With pull-up do not exceed 3.6 V.

[6] For these input pins a fixed amplification of $^{2}/_{3}$ is performed on the input voltage before feeding into the ADC0 itself. The maximum input voltage on ADC0 is $V_{DDA(ADC5V0)}$.

[7] Not exceeding 6 V.

[8] 112 mA per $V_{DD(IO)}$ or $V_{SS(IO)}$ should not be exceeded.

[9] Human-body model: discharging a 100 pF capacitor via a 10 kΩ series resistor.

Table 34. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-level input leakage current			-	-	1	μA
I_{LIL}	LOW-level input leakage current			-	-	1	μA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V		25	50	100	μA
$I_{I(pu)}$	pull-up input current	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed		−25	−50	−115	μA
C_i	input capacitance		[7]	-	3	8	pF
Output pins and I/O pins configured as output							
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
C_L	load capacitance			-	-	25	pF
USB pins USB_D+ and USB_D−							
Input characteristics							
V_{IH}	HIGH-level input voltage			1.5	-	-	V
V_{IL}	LOW-level input voltage			-	-	1.3	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Output characteristics							
Z_o	output impedance	with 33 Ω series resistor		36.0	-	44.1	Ω
V_{OH}	HIGH-level output voltage	(driven) for low-/full-speed; R_L of 15 kΩ to GND		2.9	-	3.5	V
V_{OL}	LOW-level output voltage	(driven) for low-/full-speed; with 1.5 kΩ resistor to 3.6 V external pull-up		-	-	0.18	V
I_{OH}	HIGH-level output current	at V_{OH} = $V_{DD(IO)}$ − 0.3 V; without 33 Ω external series resistor		20.8	-	41.7	mA
		at V_{OH} = $V_{DD(IO)}$ − 0.3 V; with 33 Ω external series resistor		4.8	-	5.3	mA

Table 34. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL}	LOW-level output current	at V_{OL} = 0.3 V; without 33 Ω external series resistor		26.7	-	57.2	mA
		at V_{OL} = 0.3 V; with 33 Ω external series resistor		5.0	-	5.5	mA
I_{OHS}	HIGH-level short-circuit output current	drive high; pad connected to ground		-	-	90.0	mA
I_{OLS}	LOW-level short-circuit output current	drive high; pad connected to $V_{DD(IO)}$		-	-	95.1	mA
Oscillator							
V_{XIN_OSC}	voltage on pin XIN_OSC			0	-	1.8	V
$R_{s(xtal)}$	crystal series resistance	f_{osc} = 10 MHz to 15 MHz	[8]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	160	Ω
		C_{xtal} = 20 pF; C_{ext} = 39 pF		-	-	60	Ω
		f_{osc} = 15 MHz to 20 MHz	[8]				
		C_{xtal} = 10 pF; C_{ext} = 18 pF		-	-	80	Ω
C_i	input capacitance	of XIN_OSC	[9]	-		2	pF
Power-up reset							
$V_{trip(high)}$	high trip level voltage		[10]	1.1	1.4	1.6	V
$V_{trip(low)}$	low trip level voltage		[10]	1.0	1.3	1.5	V
$V_{trip(dif)}$	difference between high and low trip level voltage		[10]	50	120	180	mV

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power-supply voltage range.

[2] Leakage current is exponential to temperature; worst-case value is at 85 °C T_{vj}. All clocks off. Analog modules and flash powered down.

[3] $V_{DDA(ADC3V3)}$ must correlate with $V_{DDA(ADC5V0)}$: $V_{DDA(ADC3V3)} = V_{DDA(ADC5V0)} / 1.5$.

[4] $V_{DDA(ADC5V0)}$ must correlate with $V_{DDA(ADC3V3)}$: $V_{DDA(ADC5V0)} = V_{DDA(ADC3V3)} \times 1.5$.

[5] Not 5 V-tolerant when pull-up is on.

[6] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[7] For Port 0, pin 0 to pin 15 add maximum 1.5 pF for input capacitance to ADC. For Port 0, pin 16 to pin 31 add maximum 1.0 pF for input capacitance to ADC.

[8] C_{xtal} is crystal load capacitance and C_{ext} are the two external load capacitors.

[9] This parameter is not part of production testing or final testing, hence only a typical value is stated. Maximum and minimum values are based on simulation results.

[10] The power-up reset has a time filter: $V_{DD(CORE)}$ must be above $V_{trip(high)}$ for 2 µs before reset is de-asserted; $V_{DD(CORE)}$ must be below $V_{trip(low)}$ for 11 µs before internal reset is asserted.

Table 35. ADC static characteristics

$V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{VREFN}	voltage on pin VREFN			0	-	V_{VREFP} − 2	V
V_{VREFP}	voltage on pin VREFP			V_{VREFN} + 2	-	$V_{DDA(ADC3V3)}$	V
V_{IA}	analog input voltage	for 3.3 V ADC1/2		V_{VREFN}	-	V_{VREFP}	V
Z_i	input impedance	between V_{VREFN} and V_{VREFP}		4.4	-	-	kΩ
		between V_{VREFN} and $V_{DDA(ADC5V0)}$		13.7	-	23.6	kΩ
C_{ia}	analog input capacitance	for ADC0/1/2		-	-	1	pF
E_D	differential linearity error	for ADC0/1/2	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	for ADC0/1/2	[1][4]	-	-	±2	LSB
E_O	offset error	for ADC0/1/2	[1][5]	-	-	±3	LSB
E_G	gain error	for ADC0/1/2	[1][6]	-	-	±0.5	%
E_T	absolute error	for ADC0/1/2	[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance	for ADC0/1/2	[8]	-	-	40	kΩ
FSR	full scale range	for ADC0/1/2		2	-	10	bit

[1] Conditions: $V_{SS(IO)}$ = 0 V, $V_{DDA(ADC3V3)}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 17.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 17.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 17.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 17.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 17.

[8] See Figure 16.

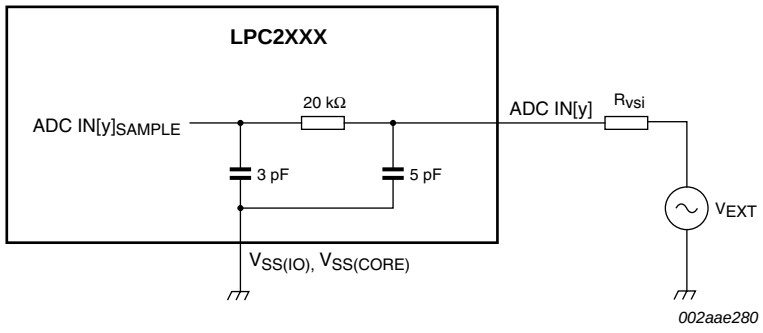
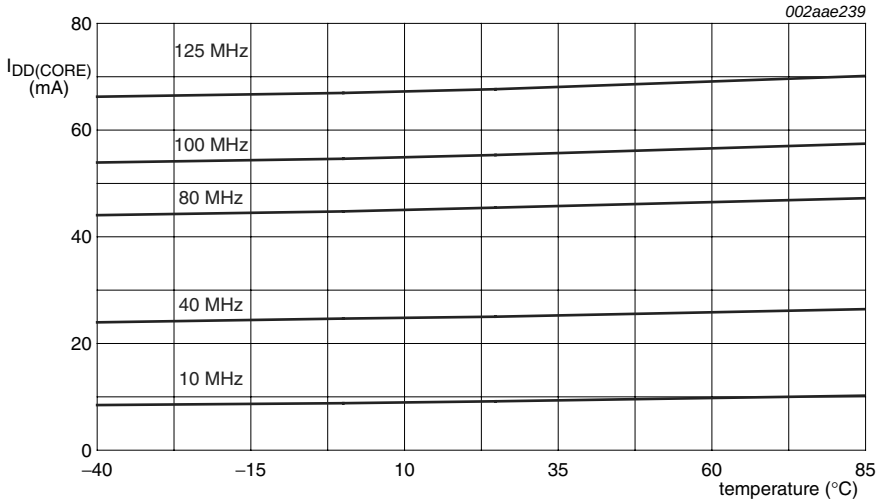


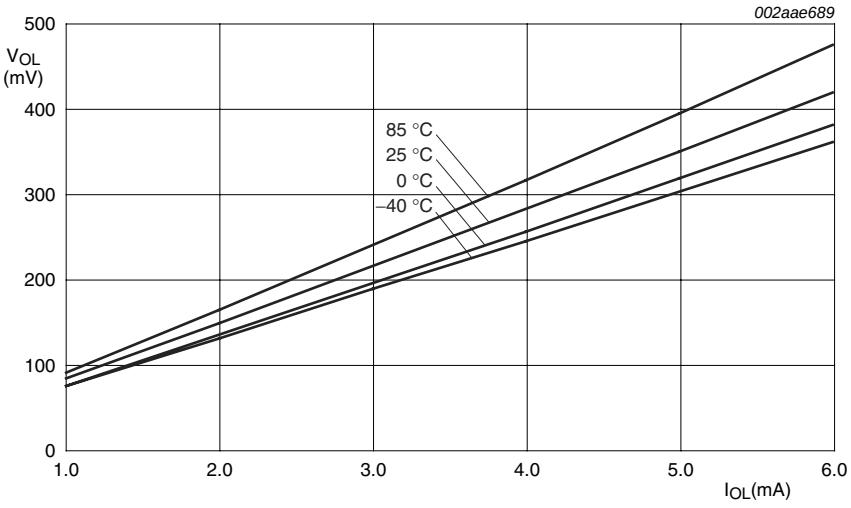
Fig 16. Suggested ADC interface - LPC2926/2927/2929 ADC1/2 IN[y] pin



Conditions: active mode entered executing code from flash; core voltage 1.8 V; all peripherals enabled but not configured to run.

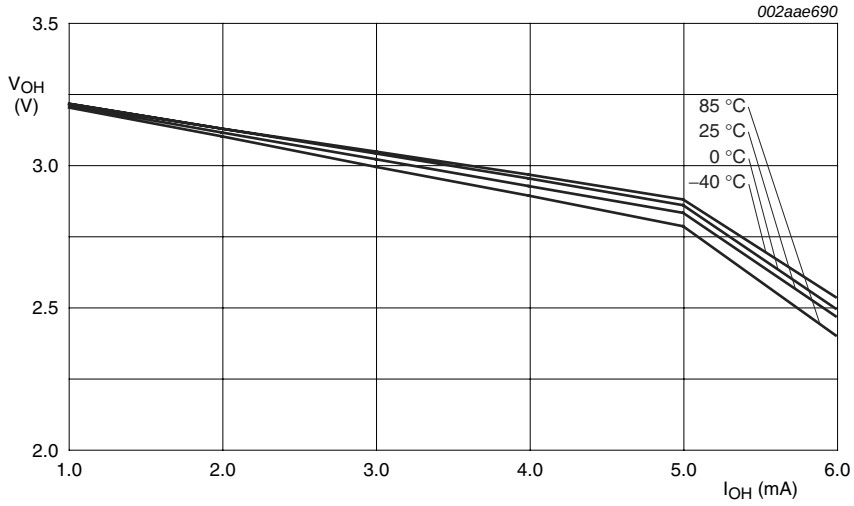
Fig 20. $I_{DD(CORE)}$ at different temperatures (active mode)

8.2 Electrical pin characteristics



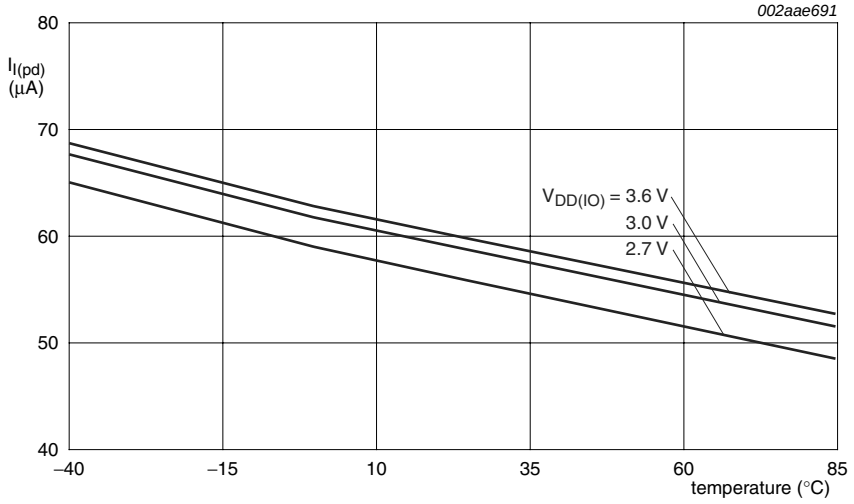
$V_{DD(IO)}$ = 3.3 V.

Fig 21. Typical LOW-level output voltage versus LOW-level output current



$V_{DD(IO)}$ = 3.3 V.

Fig 22. Typical HIGH-level output voltage versus HIGH-level output current



V_I = 3.3 V.

Fig 23. Typical pull-down current versus temperature

9.6 Dynamic characteristics: external static memory

Table 42. External static memory interface dynamic characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CLCL}	clock cycle time		8	-	100	ns
$t_{a(R)int}$	internal read access time		-	-	20.5	ns
$t_{a(W)int}$	internal write access time		-	-	24.9	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		–5	–2.5	-	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time		–5 – WSTOEN × T_{CLCL}	–2.5 – WSTOEN × T_{CLCL}	-	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		-	0 + WSTOEN × T_{CLCL}	-	ns
$t_{su(DQ)}$	data input/output set-up time		11	16	22	ns
$t_{h(D)}$	data input hold time		0	2.5	5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		-	0	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time		-	(WST1 – WSTOEN + 1) × T_{CLCL}	-	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		-	(WST1 – WSTOEN + 1) × T_{CLCL}	-	ns
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		-	0 + WSTOEN × T_{CLCL}	-	ns
Write cycle parameters						
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	[2]	-	0	-	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		-	(WSTWEN + 0.5) × T_{CLCL}	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[3]	-	WSTWEN × T_{CLCL}	-	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		-	(WSTWEN + 0.5) × T_{CLCL}	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–0.5	–0.1	0.3	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time		-	(WST2 – WSTWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4]	-	(WST2 – WSTWEN + 2) × T_{CLCL}	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] When the byte lane select signals are used to connect the write enable input (8 bit devices), $t_{CSHBLSH} = -0.5 \times T_{CLCL}$.

[3] When the byte lane select signals are used to connect the write enable input (8 bit devices), $t_{CSLBLSL} = t_{CSLWEL}$.

[4] For 16 and 32 bit devices.

10.2 Suggested USB interface solutions

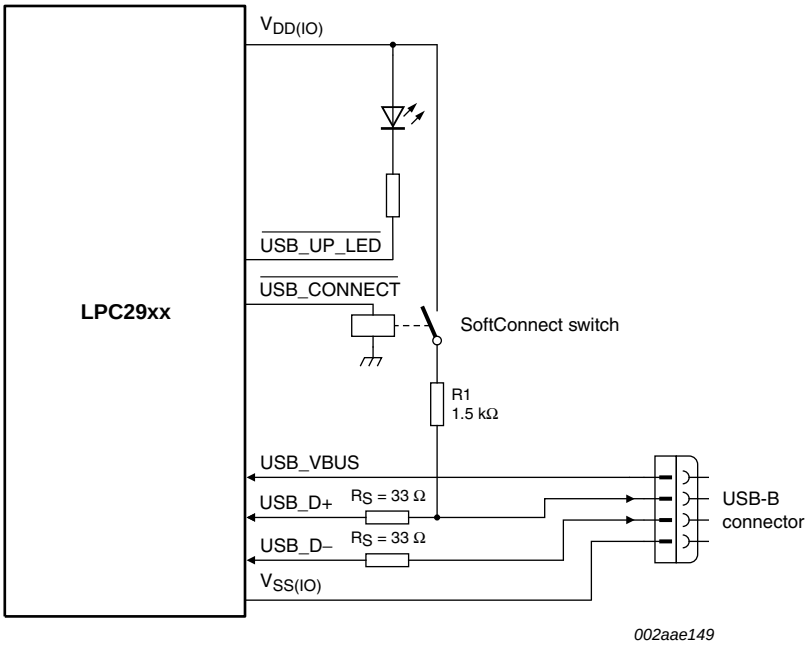


Fig 32. LPC2926/2927/2929 USB interface on a self-powered device

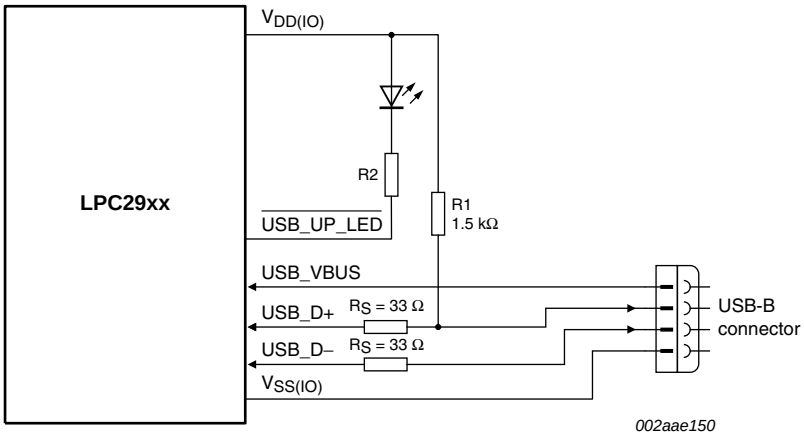


Fig 33. LPC2926/2927/2929 USB interface on a bus-powered device

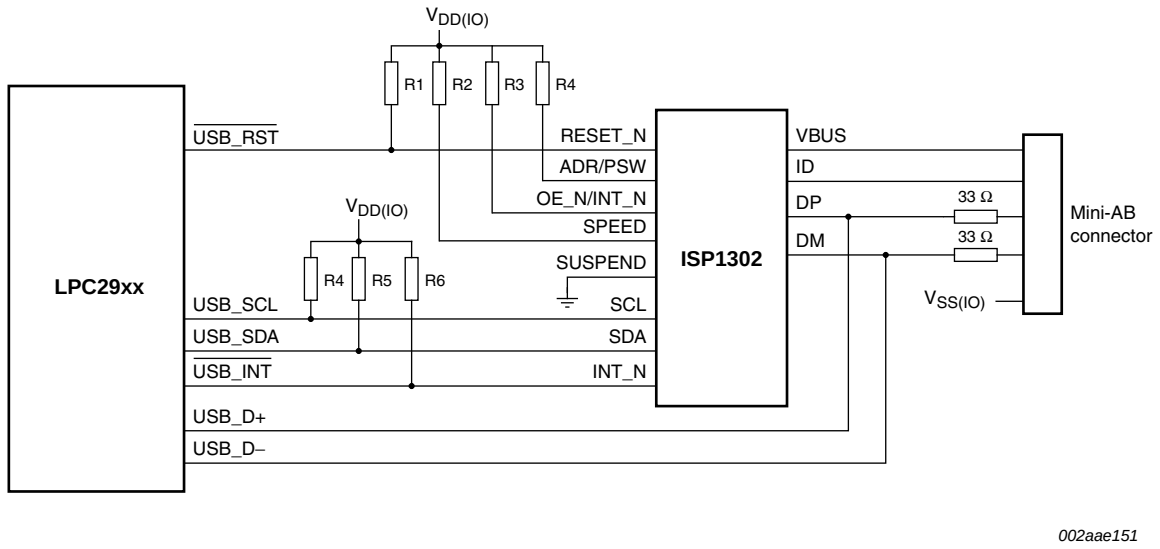


Fig 34. LPC2926/2927/2929 USB OTG port configuration

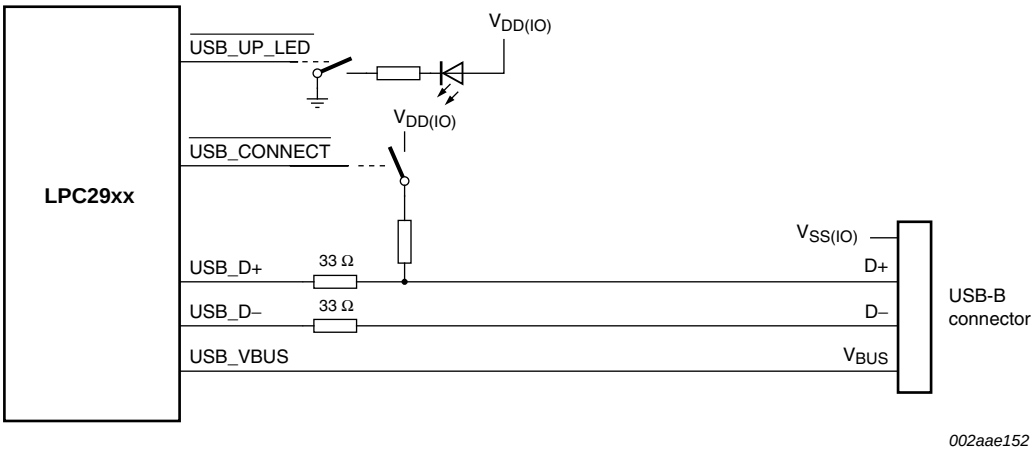


Fig 35. LPC2926/2927/2929 USB device port configuration

10.4 XIN_OSC input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed. For more details see the *LPC29xx User manual UM10316*.

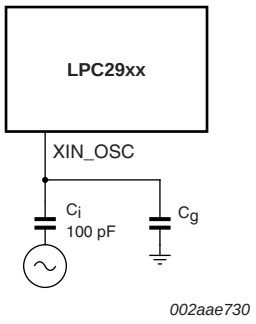


Fig 38. Slave mode operation of the on-chip oscillator

10.5 XIN_OSC Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1} and C_{x2}, and C_{x3} in case of third overtone crystal usage, have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible, in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13. Abbreviations

Table 46. Abbreviations list

Abbreviation	Description
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
BIST	Built-In Self Test
CCO	Current Controlled Oscillator
CISC	Complex Instruction Set Computers
DMA	Direct Memory Access
DSP	Digital Signal Processing
DTL	Device Transaction Level
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FIQ	Fast Interrupt reQuest
GPDMA	General Purpose DMA
IRQ	Interrupt ReQuest
LIN	Local Interconnect Network
LSB	Least Significant Bit
MAC	Media Access Control
MSB	Most Significant Bit
MSC	Modulation and Sampling Control
PHY	PHYsical layer
PLL	Phase-Locked Loop
Q-SPI	Queued SPI
RISC	Reduced Instruction Set Computer
SFSP	SCU Function Select Port x, y (use without the P if there are no x, y)
TAP	Test Access Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter

14. References

[1] **UM10316 —** *LPC29xx user manual*

[2] **ARM —** ARM web site

[3] **ARM-SSP —** ARM primecell synchronous serial port (PL022) technical reference manual

[4] **CAN —** ISO 11898-1: 2002 road vehicles - Controller Area Network (CAN) - part 1: data link layer and physical signalling

[5] **LIN —** LIN specification package, revision 2.0