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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2926fbd144-557

Table 3. LQFP144 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
$V_{DDA(ADC5V0)}$	109	5 V supply voltage for ADC0 and 5 V reference for ADC0.			
VREFP	110[3]	HIGH reference for ADC			
VREFN	111[3]	LOW reference for ADC			
P0[8]/IN1[0]/TXDL0/ A20	112[4]	GPIO0, pin 8	ADC1 IN0	LIN0 TXD/UART TXD	EXTBUS A20
P0[9]/IN1[1]/ RXDL0/A21	113[4]	GPIO0, pin 9	ADC1 IN1	LIN0 RXD/UART TXD	EXTBUS A21
P0[10]/IN1[2]/ PMAT1[0]/A8	114[4]	GPIO0, pin 10	ADC1 IN2	PWM1 MAT0	EXTBUS A8
P0[11]/IN1[3]/ PMAT1[1]/A9	115[4]	GPIO0, pin 11	ADC1 IN3	PWM1 MAT1	EXTBUS A9
P2[14]/SDA1/ PCAP0[0]/$\overline{\text{BLS0}}$	116[1]	GPIO2, pin 14	I2C1 SDA	PWM0 CAP0	EXTBUS $\overline{\text{BLS0}}$
P2[15]/SCL1/ PCAP0[1]/$\overline{\text{BLS1}}$	117[1]	GPIO2, pin 15	I2C1 SCL	PWM0 CAP1	EXTBUS $\overline{\text{BLS1}}$
P3[2]/MAT3[0]/ PMAT2[2]/ USB_SDA	118[1]	GPIO3, pin 2	TIMER3 MAT0	PWM2 MAT2	USB_SDA
$V_{SS(IO)}$	119	ground for I/O			
P3[3]/MAT3[1]/ PMAT2[3]/ USB_SCL	120[1]	GPIO3, pin 3	TIMER3 MAT1	PWM2 MAT3	USB_SCL
P0[12]/IN1[4]/ PMAT1[2]/A10	121[4]	GPIO0, pin 12	ADC1 IN4	PWM1 MAT2	EXTBUS A10
P0[13]/IN1[5]/ PMAT1[3]/A11	122[4]	GPIO0, pin 13	ADC1 IN5	PWM1 MAT3	EXTBUS A11
P0[14]/IN1[6]/ PMAT1[4]/A12	123[4]	GPIO0, pin 14	ADC1 IN6	PWM1 MAT4	EXTBUS A12
P0[15]/IN1[7]/ PMAT1[5]/A13	124[4]	GPIO0, pin 15	ADC1 IN7	PWM1 MAT5	EXTBUS A13
P0[16]IN2[0]/ TXD0/A22	125[4]	GPIO0, pin 16	ADC2 IN0	UART0 TXD	EXTBUS A22
P0[17]/IN2[1]/ RXD0/A23	126[4]	GPIO0, pin 17	ADC2 IN1	UART0 RXD	EXTBUS A23
$V_{DD(CORE)}$	127	1.8 V power supply for digital core			
$V_{SS(CORE)}$	128	ground for digital core			
P2[16]/TXD1/ PCAP0[2]/$\overline{\text{BLS2}}$	129[1]	GPIO2, pin 16	UART1 TXD	PWM0 CAP2	EXTBUS $\overline{\text{BLS2}}$
P2[17]/RXD1/ PCAP1[0]/$\overline{\text{BLS3}}$	130[1]	GPIO2, pin 17	UART1 RXD	PWM1 CAP0	EXTBUS $\overline{\text{BLS3}}$
$V_{DD(IO)}$	131	3.3 V power supply for I/O			
P0[18]/IN2[2]/ PMAT2[0]/A14	132[4]	GPIO0, pin 18	ADC2 IN2	PWM2 MAT0	EXTBUS A14

Two of the base clocks generated by the CGU0 are used as input into a second, dedicated CGU (CGU1). The CGU1 uses its own PLL and fractional dividers to generate two base clocks for the USB controller and one base clock for an independent clock output.

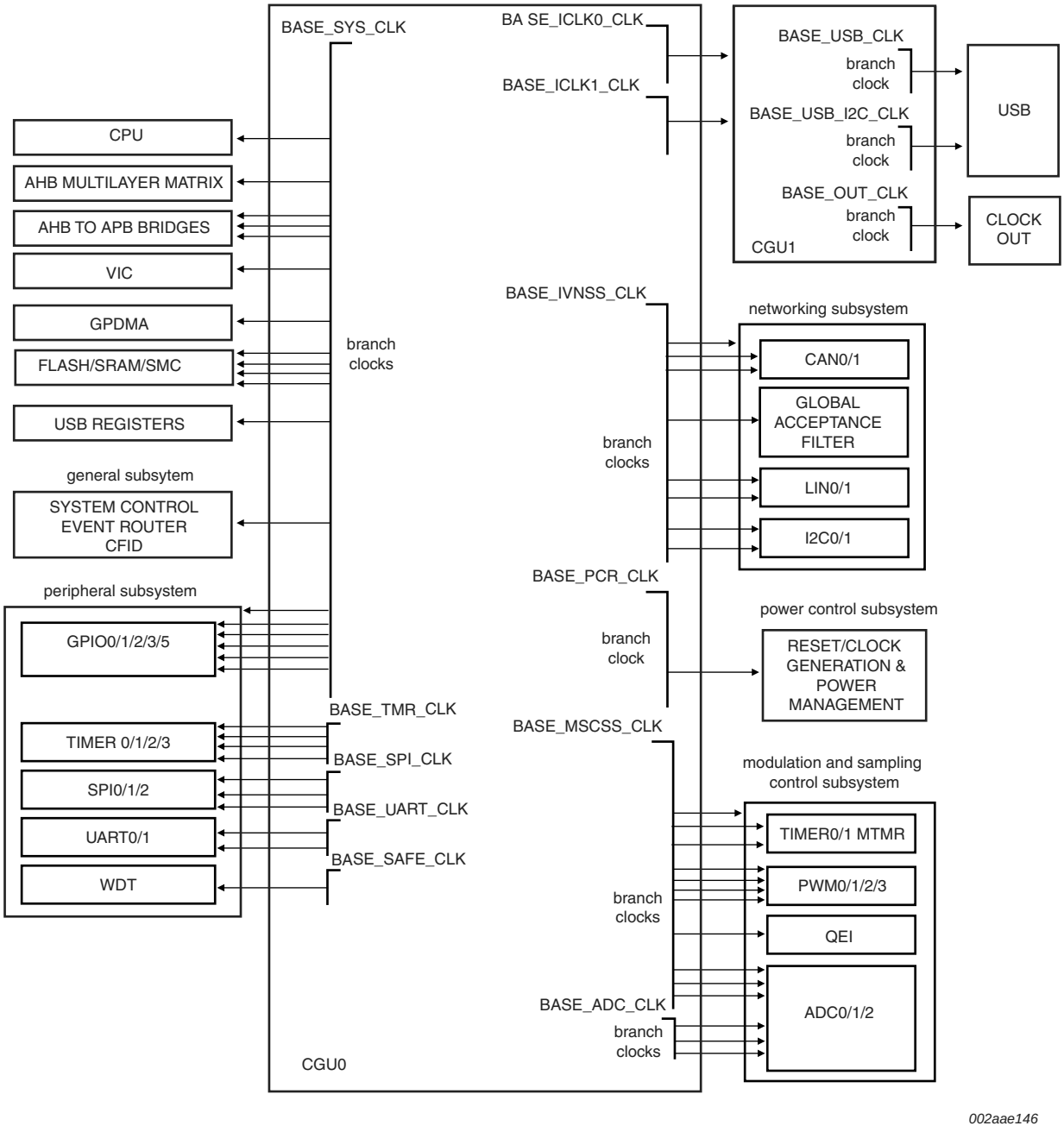


Fig 4. LPC2926/2927/2929 overview of clock areas

The USB OTG controller has the following features:

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

6.11.3 Pin description

Table 14. USB OTG port pins

Pin name	Direction	Description	Connection
USB_VBUS	I	V_{BUS} status input. When this function is not enabled via its corresponding PINSEL register, it is driven HIGH internally.	USB Connector
USB_D+	I/O	Positive differential data	USB Connector
USB_D−	I/O	Negative differential data	USB Connector
$\overline{\text{USB\_CONNECT}}$	O	SoftConnect control signal	Control
$\overline{\text{USB\_UP\_LED}}$	O	GoodLink LED control signal	Control
USB_SCL	I/O	I^2C serial clock	External OTG transceiver
USB_SDA	I/O	I^2C serial data	External OTG transceiver
USB_LS	O	Low speed status (applies to host functionality only)	External OTG transceiver
$\overline{\text{USB\_RST}}$	O	USB reset status	External OTG transceiver
$\overline{\text{USB\_INT}}$	O	USB transceiver interrupt	External OTG transceiver
USB_SSPND	O	Bus suspend status	External OTG transceiver

6.11.4 Clock description

Access to the USB registers is clocked by the CLK_SYS_USB, derived from BASE_SYS_CLK, see Section 6.7.2. The CGU1 provides two independent base clocks to the USB block, BASE_USB_CLK and BASE_USB_I2C_CLK (see Section 6.16.3).

6.13.4 UARTs

The LPC2926/2927/2929 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs.
- Register locations conform to 550 industry standard.
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes.
- Built-in baud rate generator.
- Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART is commonly used to implement a serial interface such as RS232. The LPC2926/2927/2929 contains two industry-standard 550 UARTs with 16-byte transmit and receive FIFOs, but they can also be put into 450 mode without FIFOs.

Remark: The LIN controller can be configured to provide two additional standard UART interfaces (see Section 6.14.2).

6.13.4.1 Pin description

The UART pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 17 shows the UART pins (x runs from 0 to 1).

Table 17. UART pins

Symbol	Pin name	Direction	Description
UARTx TXD	TXDx	OUT	UART channel x transmit data output
UARTx RXD	RXDx	IN	UART channel x receive data input

6.13.4.2 Clock description

The UART modules are clocked by two different clocks; CLK_SYS_PESS and CLK_UARTx (x = 0 to 1), see Section 6.7.2. Note that each UART has its own CLK_UARTx branch clock for power management. The frequency of all CLK_UARTx clocks is identical since they are derived from the same base clock BASE_CLK_UART. The register interface towards the system bus is clocked by CLK_SYS_PESS. The baud generator is clocked by the CLK_UARTx.

6.13.5 Serial Peripheral Interface (SPI)

The LPC2926/2927/2929 contains three Serial Peripheral Interface modules (SPIs) to allow synchronous serial communication with slave or master peripherals.

The key features are:

- Master or slave operation.
- Each SPI supports up to four slaves in sequential multi-slave operation.
- Supports timer-triggered operation.
- Programmable clock bit rate and prescale based on SPI source clock (BASE_SPI_CLK), independent of system clock.
- Separate transmit and receive FIFO memory buffers; 16 bits wide, 32 locations deep.

Table 19. GPIO pins

Symbol	Pin name	Direction	Description
GPIO0 pin[31:0]	P0[31:0]	IN/OUT	GPIO port x pins 31 to 0
GPIO1 pin[27:0]	P1[27:0]	IN/OUT	GPIO port x pins 27 to 0
GPIO2 pin[27:0]	P2[27:0]	IN/OUT	GPIO port x pins 27 to 0
GPIO3 pin[15:0]	P3[15:0]	IN/OUT	GPIO port x pins 15 to 0
GPIO5 pin[19:18]	P5[19:18]	IN/OUT	GPIO port x pins 19 and 18

6.13.6.3 Clock description

The GPIO modules are clocked by several clocks, all of which are derived from BASE_SYS_CLK; CLK_SYS_PESS and CLK_SYS_GPIOx (x = 0, 1, 2, 3, 5), see Section 6.7.2. Note that each GPIO has its own CLK_SYS_GPIOx branch clock for power management. The frequency of all clocks CLK_SYS_GPIOx is identical to CLK_SYS_PESS since they are derived from the same base clock BASE_SYS_CLK.

6.14 Networking subsystem

6.14.1 CAN gateway

Controller Area Network (CAN) is the definition of a high-performance communication protocol for serial data communication. The two CAN controllers in the LPC2926/2927/2929 provide a full implementation of the CAN protocol according to the *CAN specification version 2.0B*. The gateway concept is fully scalable with the number of CAN controllers, and always operates together with a separate powerful and flexible hardware acceptance filter.

The key features are:

- Supports 11-bit as well as 29-bit identifiers
- Double receive buffer and triple transmit buffer
- Programmable error-warning limit and error counters with read/write access
- Arbitration-lost capture and error-code capture with detailed bit position
- Single-shot transmission (i.e. no re-transmission)
- Listen-only mode (no acknowledge; no active error flags)
- Reception of ‘own’ messages (self-reception request)
- FullCAN mode for message reception

6.14.1.1 Global acceptance filter

The global acceptance filter provides look-up of received identifiers - called acceptance filtering in CAN terminology - for all the CAN controllers. It includes a CAN ID look-up table memory, in which software maintains one to five sections of identifiers. The CAN ID look-up table memory is 2 kB large (512 words, each of 32 bits). It can contain up to 1024 standard frame identifiers or 512 extended frame identifiers or a mixture of both types. It is also possible to define identifier groups for standard and extended message formats.

6.14.1.2 Pin description

The two CAN controllers in the LPC2926/2927/2929 have the pins listed below. The CAN pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 20 shows the CAN pins (x runs from 0 to 1).

Table 20. CAN pins

Symbol	Pin name	Direction	Description
CANx TXD	TXDC0/1	OUT	CAN channel x transmit data output
CANx RXD	RXDC0/1	IN	CAN channel x receive data input

6.14.2 LIN

The LPC2926/2927/2929 contain two LIN 2.0 master controllers. These can be used as dedicated LIN 2.0 master controllers with additional support for sync break generation and with hardware implementation of the LIN protocol according to spec 2.0.

Remark: Both LIN channels can be also configured as UART channels.

The key features are:

- Complete LIN 2.0 message handling and transfer
- One interrupt per LIN message
- Slave response time-out detection
- Programmable sync-break length
- Automatic sync-field and sync-break generation
- Programmable inter-byte space
- Hardware or software parity generation
- Automatic checksum generation
- Fault confinement
- Fractional baud rate generator

6.14.2.1 Pin description

The two LIN 2.0 master controllers in the LPC2926/2927/2929 have the pins listed below. The LIN pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 21 shows the LIN pins. For more information see Ref. 1 subsection 3.43, LIN master controller.

Table 21. LIN controller pins

Symbol	Pin name	Direction	Description
LIN0/1 TXD	TXDL0/1	OUT	LIN channel 0/1 transmit data output
LIN0/1 RXD	RXDL0/1	IN	LIN channel 0/1 receive data input

6.14.3 I^2C-bus serial I/O controllers

The LPC2926/2927/2929 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial CLock line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or as a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or

6.15.4.1 Functional description

The ADC block diagram, Figure 9, shows the basic architecture of each ADC. The ADC functionality is divided into two major parts; one part running on the MSCSS Subsystem clock, the other on the ADC clock. This split into two clock domains affects the behavior from a system-level perspective. The actual analog-to-digital conversions take place in the ADC clock domain, but system control takes place in the system clock domain.

A mechanism is provided to modify configuration of the ADC and control the moment at which the updated configuration is transferred to the ADC domain.

The ADC clock is limited to 4.5 MHz maximum frequency and should always be lower than or equal to the system clock frequency. To meet this constraint or to select the desired lower sampling frequency, the clock generation unit provides a programmable fractional system-clock divider dedicated to the ADC clock. Conversion rate is determined by the ADC clock frequency divided by the number of resolution bits plus one. Accessing ADC registers requires an enabled ADC clock, which is controllable via the clock generation unit, see Section 6.16.2.

Each ADC has four start inputs. Note that start 0 and start 2 are captured in the system clock domain while start 1 and start 3 are captured in the ADC domain. The start inputs are connected at MSCSS level, see Section 6.15 for details.

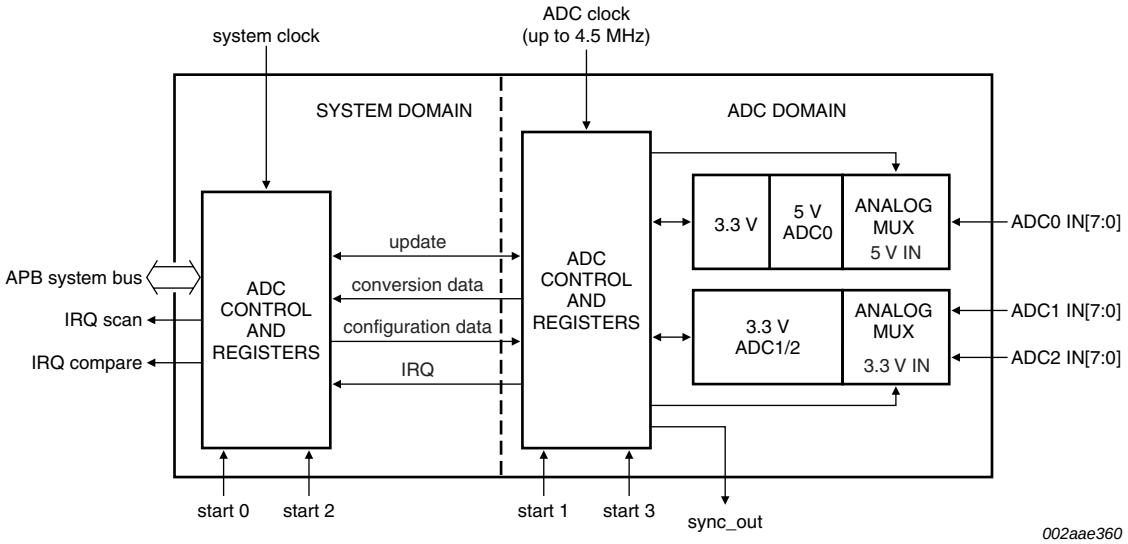


Fig 9. ADC block diagram

6.15.4.2 Pin description

The three ADC modules in the MSCSS have the pins described below. The ADCx input pins are combined with other functions on the port pins of the LPC2926/2927/2929. The VREFN and VREFP pins are common to all ADCs. Table 23 shows the ADC pins.

Table 23. ADC pins

Symbol	Pin name	Direction	Description
ADC0 IN[7:0]	IN0[7:0]	IN	analog input for 5.0 V ADC0, channel 7 to channel 0.
ADC1/2 IN[7:0]	IN1/2[7:0]	IN	analog input for 3.3 V ADC1/2, channel 7 to channel 0.
ADC2_EXT_START	CAP1[2]	IN	ADC external start-trigger input.
VREFN	VREFN	IN	ADC LOW reference level.
VREFP	VREFP	IN	ADC HIGH reference level.
$V_{DDA(ADC5V0)}$	$V_{DDA(ADC5V0)}$[1]	IN	5 V high-power supply and HIGH reference for ADC0. Connect to clean 5 V as HIGH reference. May also be connected to 3.3 V if 3.3 V measurement range for ADC0 is needed.[2][3]
$V_{DDA(ADC3V3)}$	$V_{DDA(ADC3V3)}$	IN	ADC1 and ADC2 3.3 V supply (also used for ADC0).[3]

[1] VREFP, VREFN, $V_{DDA(ADC3V3)}$ must be connected for the 5 V ADC0 to operate properly.

[2] The analog inputs of ADC0 are internally multiplied by a factor of 3.3 / 5. If $V_{DDA(ADC5V0)}$ is connected to 3.3 V, the maximum digital result is 1024 × 3.3 / 5.

[3] $V_{DDA(ADC5V0)}$ and $V_{DDA(ADC3V3)}$ must be set as follows: $V_{DDA(ADC5V0)} = V_{DDA(ADC3V3)} \times 1.5$.

Remark: The following formula only applies to ADC0:

Voltage variations on VREFP (i.e. those that deviate from voltage variations on the $V_{DDA(ADC5V5)}$ pin) are visible as variations in the measurement result. The following formula is used to determine the conversion result of an input voltage V_I on ADC0:

$$\left(\frac{2}{3}\left(V_I - \frac{1}{2}V_{DDA(ADC5V0)}\right) + \frac{1}{2}V_{DDA(ADC3V3)}\right) \times \frac{1024}{V_{VREFP} - V_{VREFN}} \quad (3)$$

Remark: Note that the ADC1 and ADC2 accept an input voltage up to of 3.6 V (see Table 34) on the ADC1/2 IN pins. If the ADC is not used, the pins are 5 V tolerant. The ADC0 pins are 5 V tolerant.

6.15.4.3 Clock description

The ADC modules are clocked from two different sources; CLK_MSCSS_ADCx_APB and CLK_ADCx (x = 0, 1, or 2), see Section 6.7.2. Note that each ADC has its own CLK_ADCx and CLK_MSCSS_ADCx_APB branch clocks for power management. If an ADC is unused both its CLK_MSCSS_ADCx_APB and CLK_ADCx can be switched off.

The frequency of all the CLK_MSCSS_ADCx_APB clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK. Likewise the frequency of all the CLK_ADCx clocks is identical since they are derived from the same base clock BASE_ADC_CLK.

The register interface towards the system bus is clocked by CLK_MSCSS_ADCx_APB. Control logic for the analog section of the ADC is clocked by CLK_ADCx, see also Figure 9.

Configuration of the CGU0: For every output generator generating the base clocks a choice can be made from the primary and secondary clock generators according to Figure 13.

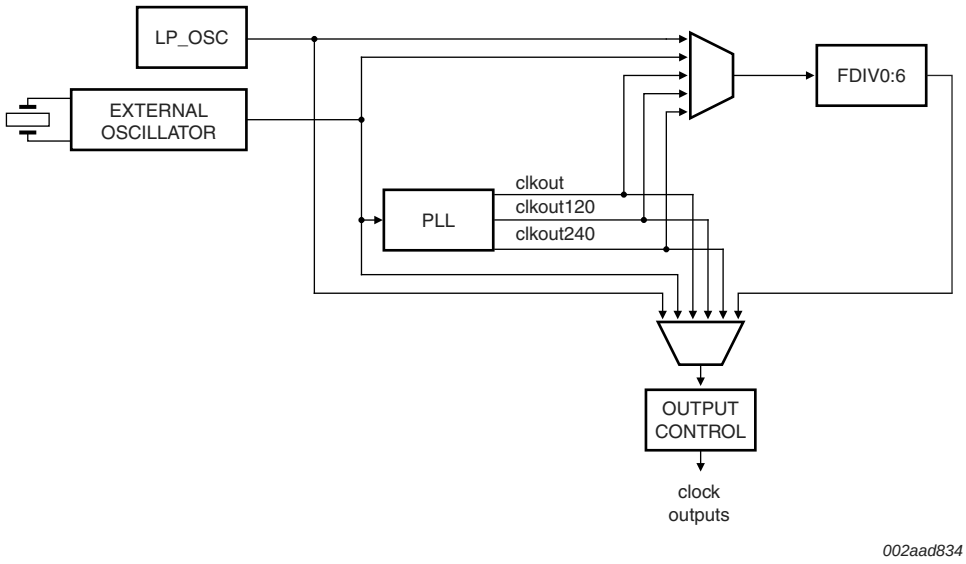


Fig 13. Structure of the clock generation scheme

Any output generator (except for BASE_SAFE_CLK and BASE_PCR_CLK) can be connected to either a fractional divider (FDIV[0:6]) or to one of the outputs of the PLL or to LP_OSC/crystal oscillator directly. BASE_SAFE_CLK and BASE_PCR_CLK can use only LP_OSC as source.

The fractional dividers can be connected to one of the outputs of the PLL or directly to LP_OSC/crystal Oscillator.

The PLL is connected to the crystal oscillator.

In this way every output generating the base clocks can be configured to get the required clock. Multiple output generators can be connected to the same primary or secondary clock source, and multiple secondary clock sources can be connected to the same PLL output or primary clock source.

Invalid selections/programming - connecting the PLL to an FDIV or to one of the PLL outputs itself for example - will be blocked by hardware. The control register will not be written, the previous value will be kept, although all other fields will be written with new data. This prevents clocks being blocked by incorrect programming.

Default Clock Sources: Every secondary clock generator or output generator is connected to LP_OSC at reset. In this way the device runs at a low frequency after reset. It is recommended to switch BASE_SYS_CLK to a high-frequency clock generator as one of the first steps in the boot code after verifying that the high-frequency clock generator is running.

Clock Activity Detection: Clocks that are inactive are automatically regarded as invalid, and values of ‘CLK_SEL’ that would select those clocks are masked and not written to the control registers. This is accomplished by adding a clock detector to every clock

6.16.4.2 Pin description

The RGU module in the LPC2926/2927/2929 has the following pins. Table 31 shows the RGU pins.

Table 31. RGU pins

Symbol	Direction	Description
$\overline{RST}$	IN	external reset input, Active LOW; pulled up internally

6.16.5 Power Management Unit (PMU)

This module enables software to actively control the system's power consumption by disabling clocks not required in a particular operating mode.

Using the base clocks from the CGU as input, the PMU generates branch clocks to the rest of the LPC2926/2927/2929. Output clocks branched from the same base clock are phase- and frequency-related. These branch clocks can be individually controlled by software programming.

The key features are:

- Individual clock control for all LPC2926/2927/2929 sub-modules.
- Activates sleeping clocks when a wake-up event is detected.
- Clocks can be individually disabled by software.
- Supports AHB master-disable protocol when AUTO mode is set.
- Disables wake-up of enabled clocks when Power-down mode is set.
- Activates wake-up of enabled clocks when a wake-up event is received.
- Status register is available to indicate if an input base clock can be safely switched off (i.e. all branch clocks are disabled).

6.16.5.1 Functional description

The PMU controls all internal clocks coming out of the CGU0 for power-mode management. With some exceptions, each branch clock can be switched on or off individually under control of software register bits located in its individual configuration register. Some branch clocks controlling vital parts of the device operate in a fixed mode. Table 32 shows which mode-control bits are supported by each branch clock.

By programming the configuration register the user can control which clocks are switched on or off, and which clocks are switched off when entering Power-down mode.

Note that the standby-wait-for-interrupt instructions of the ARM968E-S processor (putting the ARM CPU into a low-power state) are not supported. Instead putting the ARM CPU into power-down should be controlled by disabling the branch clock for the CPU.

Remark: For any disabled branch clocks to be re-activated their corresponding base clocks must be running (controlled by CGU0).

Table 32 shows the relation between branch and base clocks, see also Section 6.7.1. Every branch clock is related to one particular base clock: it is not possible to switch the source of a branch clock in the PMU.

6.17.1 Functional description

The Vectored Interrupt Controller routes incoming interrupt requests to the ARM processor. The interrupt target is configured for each interrupt request input of the VIC. The targets are defined as follows:

- Target 0 is ARM processor FIQ (fast interrupt service).
- Target 1 is ARM processor IRQ (standard interrupt service).

Interrupt-request masking is performed individually per interrupt target by comparing the priority level assigned to a specific interrupt request with a target-specific priority threshold. The priority levels are defined as follows:

- Priority level 0 corresponds to ‘masked’ (i.e. interrupt requests with priority 0 never lead to an interrupt).
- Priority 1 corresponds to the lowest priority.
- Priority 15 corresponds to the highest priority.

Software interrupt support is provided and can be supplied for:

- Testing RTOS (Real-Time Operating System) interrupt handling without using device-specific interrupt service routines.
- Software emulation of an interrupt-requesting device, including interrupts.

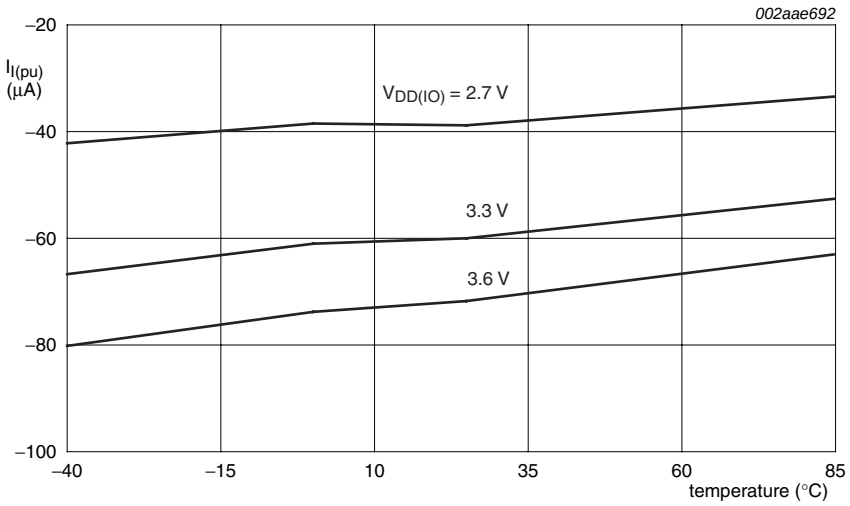
6.17.2 Clock description

The VIC is clocked by CLK_SYS_VIC, see Section 6.7.2.

Table 34. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS, TCK		-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
I_{LIH}	HIGH-level input leakage current			-	-	1	μA
I_{LIL}	LOW-level input leakage current			-	-	1	μA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V		25	50	100	μA
$I_{I(pu)}$	pull-up input current	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed		−25	−50	−115	μA
C_i	input capacitance		[7]	-	3	8	pF
Output pins and I/O pins configured as output							
V_O	output voltage			0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
C_L	load capacitance			-	-	25	pF
USB pins USB_D+ and USB_D−							
Input characteristics							
V_{IH}	HIGH-level input voltage			1.5	-	-	V
V_{IL}	LOW-level input voltage			-	-	1.3	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Output characteristics							
Z_o	output impedance	with 33 Ω series resistor		36.0	-	44.1	Ω
V_{OH}	HIGH-level output voltage	(driven) for low-/full-speed; R_L of 15 kΩ to GND		2.9	-	3.5	V
V_{OL}	LOW-level output voltage	(driven) for low-/full-speed; with 1.5 kΩ resistor to 3.6 V external pull-up		-	-	0.18	V
I_{OH}	HIGH-level output current	at V_{OH} = $V_{DD(IO)}$ − 0.3 V; without 33 Ω external series resistor		20.8	-	41.7	mA
		at V_{OH} = $V_{DD(IO)}$ − 0.3 V; with 33 Ω external series resistor		4.8	-	5.3	mA



V_I = 0 V.

Fig 24. Typical pull-up current versus temperature

9.2 USB interface

Table 37. Dynamic characteristics: USB pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 26		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 26		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 26	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 26	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

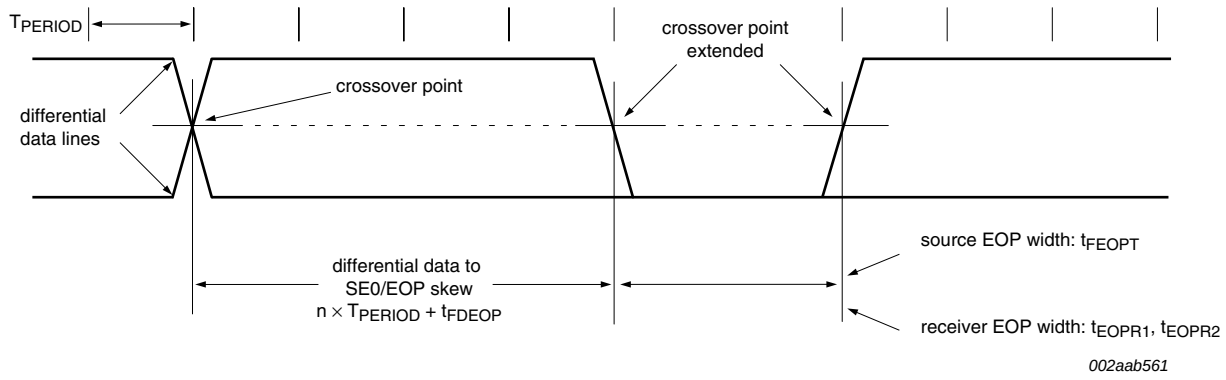


Fig 26. Differential data-to-EOP transition skew and EOP width

9.4 Dynamic characteristics: SPI

Table 39. Dynamic characteristics of SPI pins

$V_{DD(CORE)} = V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI}	SPI operating frequency	master operation	$1/65024 f_{clk(SPI)}$	-	$1/2 f_{clk(SPI)}$	MHz
		slave operation	$1/65024 f_{clk(SPI)}$	-	$1/4 f_{clk(SPI)}$	MHz
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 27	-	11	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

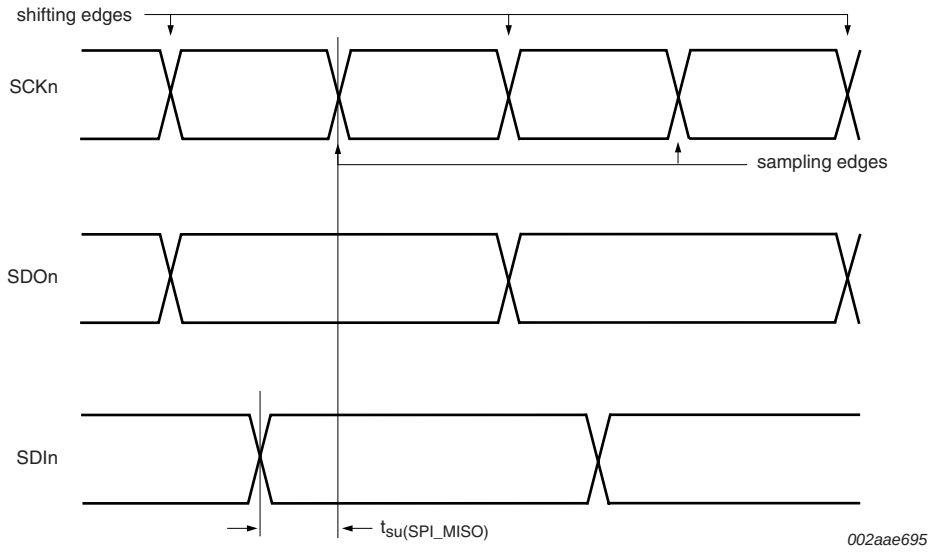


Fig 27. SPI data input set-up time in SSP Master mode

9.7 Dynamic characteristics: ADC

Table 43. ADC dynamic characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
5.0 V ADC0							
$f_{i(ADC)}$	ADC input frequency		[2]	4	-	4.5	MHz
$f_{s(max)}$	maximum sampling rate	$f_{i(ADC)}$ = 4.5 MHz; $f_s = f_{i(ADC)} / (n + 1)$ with n = resolution					
		resolution 2 bit		-	-	1500	ksample/s
		resolution 10 bit		-	-	400	ksample/s
t_{conv}	conversion time	In number of ADC clock cycles		3	-	11	cycles
		In number of bits		2	-	10	bits
3.3 V ADC1/2							
$f_{i(ADC)}$	ADC input frequency		[2]	4	-	4.5	MHz
$f_{s(max)}$	maximum sampling rate	$f_{i(ADC)}$ = 4.5 MHz; $f_s = f_{i(ADC)} / (n + 1)$ with n = resolution					
		resolution 2 bit		-	-	1500	ksample/s
		resolution 10 bit		-	-	400	ksample/s
t_{conv}	conversion time	In number of ADC clock cycles		3	-	11	cycles
		In number of bits		2	-	10	bits

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Duty cycle clock should be as close as possible to 50 %.

10. Application information

10.1 Operating frequency selection

The LPC2926/2927/2929 is specified to operate at a maximum frequency of 125 MHz, maximum temperature of 85 °C, and maximum core voltage of 1.89 V. Figure 30 and Figure 31 show that the user can achieve higher operating frequencies for the LPC2926/2927/2929 by controlling the temperature and the core voltage accordingly.

10.2 Suggested USB interface solutions

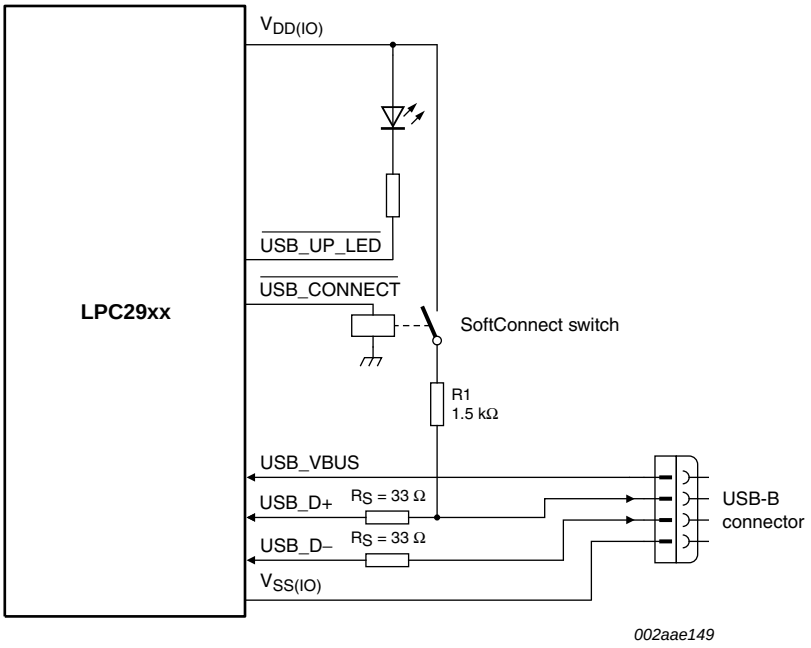


Fig 32. LPC2926/2927/2929 USB interface on a self-powered device

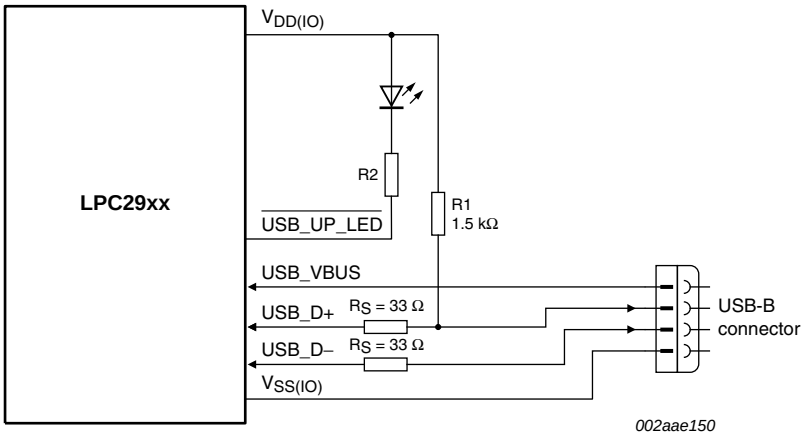


Fig 33. LPC2926/2927/2929 USB interface on a bus-powered device

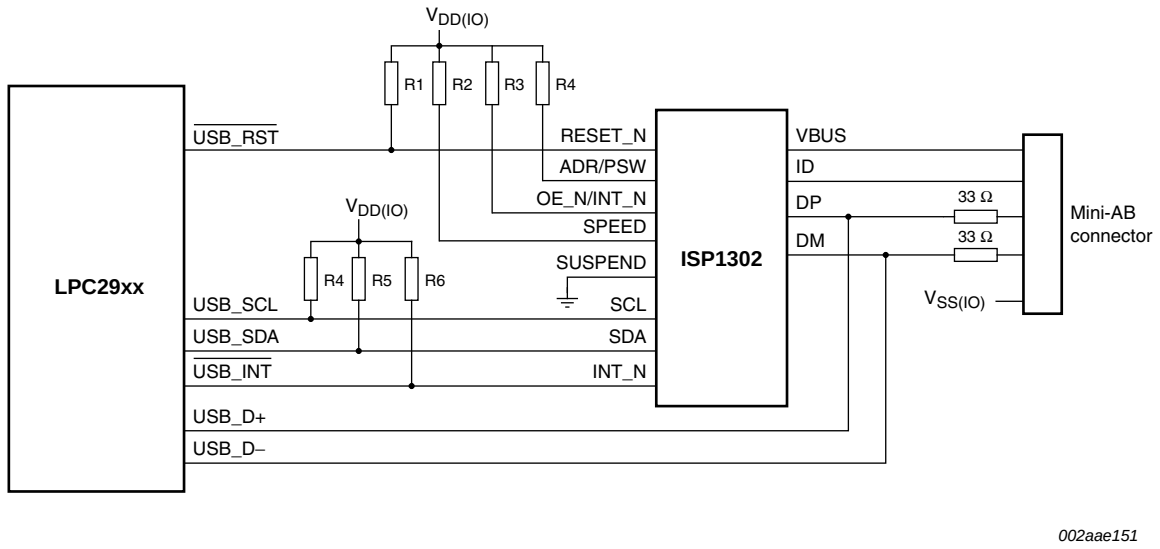


Fig 34. LPC2926/2927/2929 USB OTG port configuration

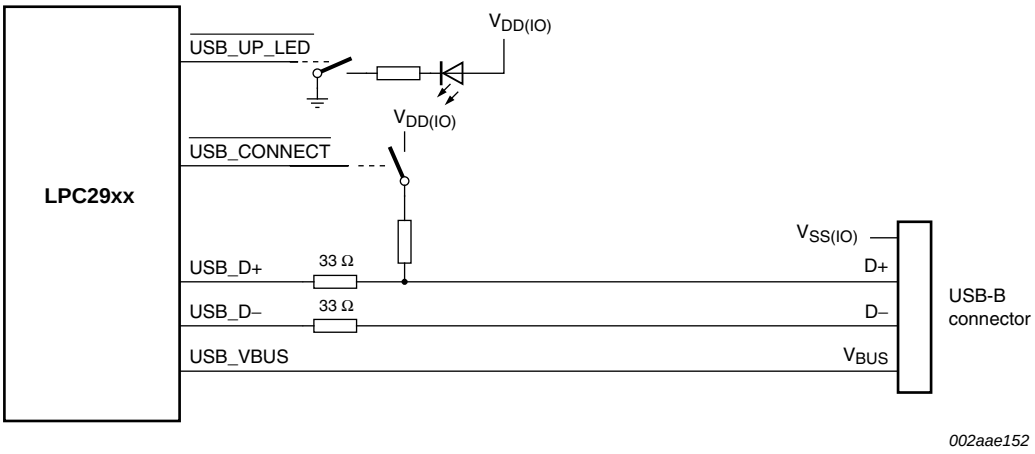
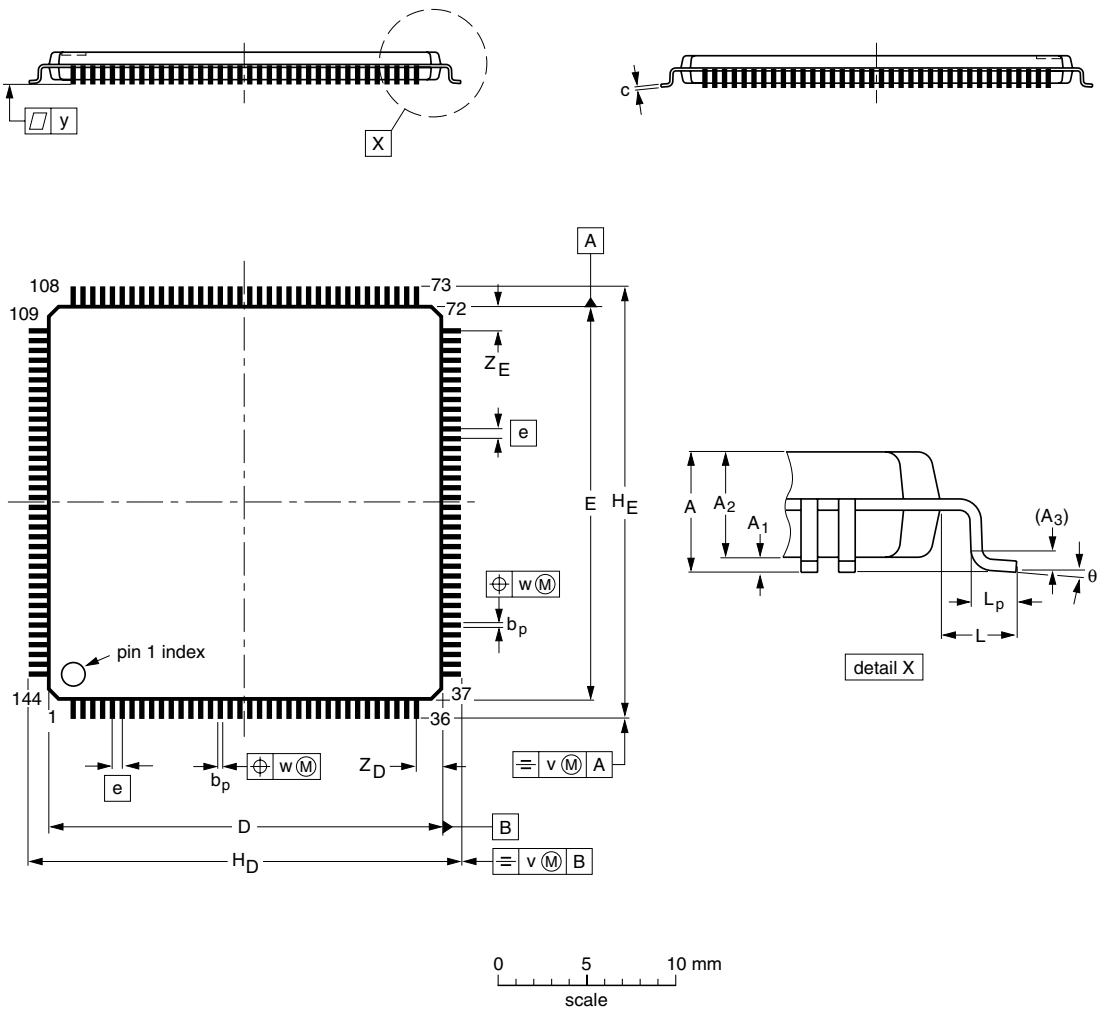


Fig 35. LPC2926/2927/2929 USB device port configuration

11. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 39. Package outline SOT486-1 (LQFP144)

13. Abbreviations

Table 46. Abbreviations list

Abbreviation	Description
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
BIST	Built-In Self Test
CCO	Current Controlled Oscillator
CISC	Complex Instruction Set Computers
DMA	Direct Memory Access
DSP	Digital Signal Processing
DTL	Device Transaction Level
EOP	End Of Packet
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FIQ	Fast Interrupt reQuest
GPDMA	General Purpose DMA
IRQ	Interrupt ReQuest
LIN	Local Interconnect Network
LSB	Least Significant Bit
MAC	Media Access Control
MSB	Most Significant Bit
MSC	Modulation and Sampling Control
PHY	PHYsical layer
PLL	Phase-Locked Loop
Q-SPI	Queued SPI
RISC	Reduced Instruction Set Computer
SFSP	SCU Function Select Port x, y (use without the P if there are no x, y)
TAP	Test Access Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver Transmitter

14. References

[1] **UM10316 —** *LPC29xx user manual*

[2] **ARM —** ARM web site

[3] **ARM-SSP —** ARM primecell synchronous serial port (PL022) technical reference manual

[4] **CAN —** ISO 11898-1: 2002 road vehicles - Controller Area Network (CAN) - part 1: data link layer and physical signalling

[5] **LIN —** LIN specification package, revision 2.0