NXP USA Inc. - LPC2927FBD144,551 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2927fbd144-551

Table 3. LQFP144 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P1[3]/SCS2[1]/ PMAT3[3]/A3	85[1]	GPIO1, pin 3	SPI2 SCS1	PWM3 MAT3	EXTBUS A3
P1[2]/SCS2[3]/ PMAT3[2]/A2	86[1]	GPIO1, pin 2	SPI2 SCS3	PWM3 MAT2	EXTBUS A2
P1[1]/EI1/ PMAT3[1]/A1	87[1]	GPIO1, pin 1	EXTINT1	PWM3 MAT1	EXTBUS A1
$V_{SS(CORE)}$	88	ground for digital core			
$V_{DD(CORE)}$	89	1.8 V power supply for digital core			
P1[0]/EI0/ PMAT3[0]/A0	90[1]	GPIO1, pin 0	EXTINT0	PWM3 MAT0	EXTBUS A0
P2[10]/ PMAT0[2]/ SCS0[0]	91[1]	GPIO2, pin 10	$\overline{\text{USB\_INT}}$	PWM0 MAT2	SPI0 SCS0
P2[11]/ PMAT0[3]/SCK0	92[1]	GPIO2, pin 11	$\overline{\text{USB\_RST}}$	PWM0 MAT3	SPI0 SCK
P0[0]/PHB0/ TXDC0/D24	93[1]	GPIO0, pin 0	QEI0 PHB	CAN0 TXD	EXTBUS D24
$V_{SS(IO)}$	94	ground for I/O			
P0[1]/PHA0/ RXDC0/D25	95[1]	GPIO0, pin 1	QEI 0 PHA	CAN0 RXD	EXTBUS D25
P0[2]/CLK_OUT/ PMAT0[0]/D26	96[1]	GPIO0, pin 2	CLK_OUT	PWM0 MAT0	EXTBUS D26
P0[3]/$\overline{\text{USB\_UP\_LED/}}$ PMAT0[1]/D27	97[1]	GPIO0, pin 3	$\overline{\text{USB\_UP\_LED}}$	PWM0 MAT1	EXTBUS D27
P3[0]/IN0[6]/ PMAT2[0]/$\overline{\text{CS6}}$	98[1]	GPIO3, pin 0	ADC0 IN6	PWM2 MAT0	EXTBUS $\overline{\text{CS6}}$
P3[1]/IN0[7/ PMAT2[1]/$\overline{\text{CS7}}$	99[1]	GPIO3, pin 1	ADC0 IN7	PWM2 MAT1	EXTBUS $\overline{\text{CS7}}$
P2[12]/IN0[4] PMAT0[4]/SDI0	100[1]	GPIO2, pin 12	ADC0 IN4	PWM0 MAT4	SPI0 SDI
P2[13]/IN0[5] PMAT0[5]/SDO0	101[1]	GPIO2, pin 13	ADC0 IN5	PWM0 MAT5	SPI0 SDO
P0[4]/IN0[0]/ PMAT0[2]/D28	102[1]	GPIO0, pin 4	ADC0 IN0	PWM0 MAT2	EXTBUS D28
P0[5]/IN0[1]/ PMAT0[3]/D29	103[1]	GPIO0, pin 5	ADC0 IN1	PWM0 MAT3	EXTBUS D29
$V_{DD(IO)}$	104	3.3 V power supply for I/O			
P0[6]/IN0[2]/ PMAT0[4]/D30	105[1]	GPIO0, pin 6	ADC0 IN2	PWM0 MAT4	EXTBUS D30
P0[7]/IN0[3]/ PMAT0[5]/D31	106[1]	GPIO0, pin 7	ADC0 IN3	PWM0 MAT5	EXTBUS D31
$V_{DDA(ADC3V3)}$	107	3.3 V power supply for ADC			
JTAGSEL	108[1]	TAP controller select input; LOW-level selects the ARM debug mode; HIGH-level selects boundary scan; pulled up internally.			

The LPC2926/2927/2929 configures the ARM968E-S processor in little-endian byte order. All peripherals run at their own clock frequency to optimize the total system power consumption. The AHB-to-APB bridge used in the subsystems contains a write-ahead buffer one transaction deep. This implies that when the ARM968E-S issues a buffered write action to a register located on the APB side of the bridge, it continues even though the actual write may not yet have taken place. Completion of a second write to the same subsystem will not be executed until the first write is finished.

6.2 ARM968E-S processor

The ARM968E-S is a general purpose 32-bit RISC processor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective controller core.

Amongst the most compelling features of the ARM968E-S are:

- Separate directly connected instruction and data Tightly Coupled Memory (TCM) interfaces
- Write buffers for the AHB and TCM buses
- Enhanced 16 × 32 multiplier capable of single-cycle MAC operations and 16-bit fixed-point DSP instructions to accelerate signal-processing algorithms and applications.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. The ARM968E-S is based on the ARMv5TE five-stage pipeline architecture. Typically, in a three-stage pipeline architecture, while one instruction is being executed its successor is being decoded and a third instruction is being fetched from memory. In the five-stage pipeline additional stages are added for memory access and write-back cycles.

The ARM968E-S processor also employs a unique architectural strategy known as THUMB, which makes it ideally suited to high-volume applications with memory restrictions or to applications where code density is an issue.

The key idea behind THUMB is that of a super-reduced instruction set. Essentially, the ARM968E-S processor has two instruction sets:

- Standard 32-bit ARMv5TE set
- 16-bit THUMB set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit controller using 16-bit registers. This is possible because THUMB code operates on the same 32-bit register set as ARM code.

THUMB code can provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM controller connected to a 16-bit memory system.

The ARM968E-S processor is described in detail in the ARM968E-S data sheet Ref. 2.

Two of the base clocks generated by the CGU0 are used as input into a second, dedicated CGU (CGU1). The CGU1 uses its own PLL and fractional dividers to generate two base clocks for the USB controller and one base clock for an independent clock output.

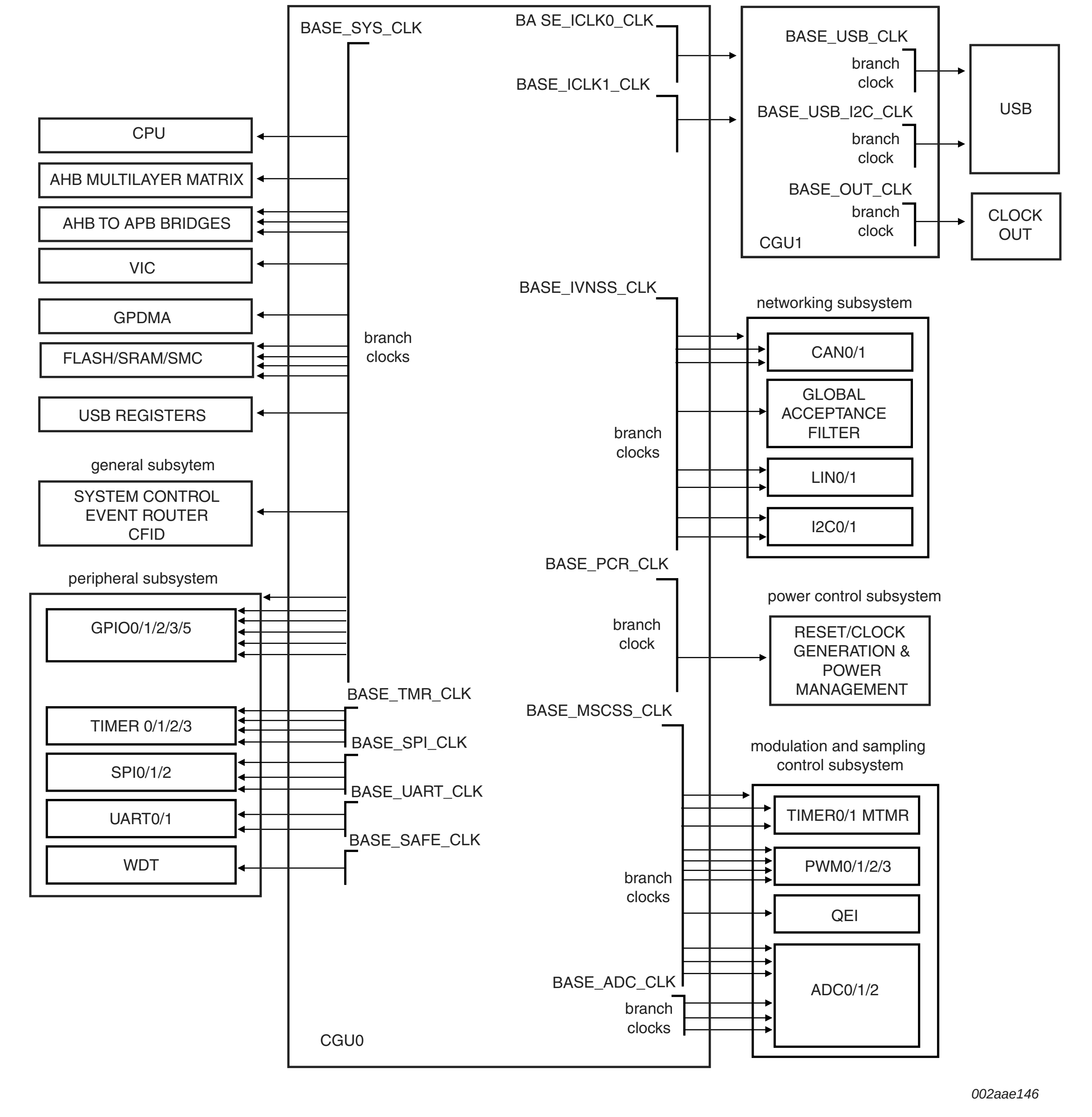
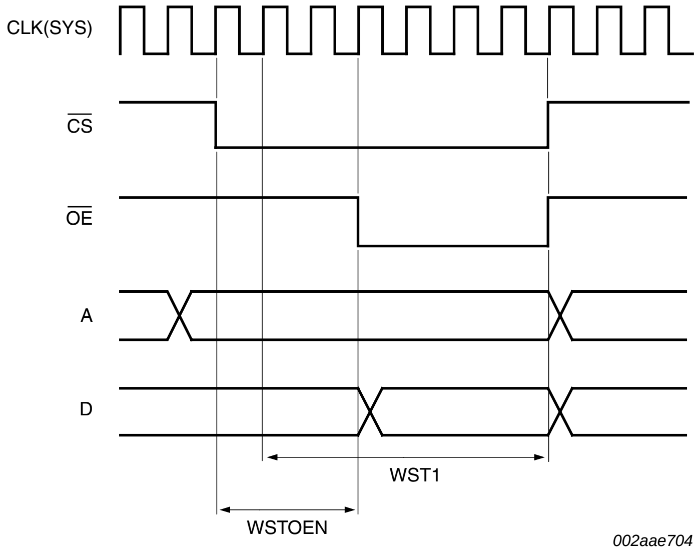


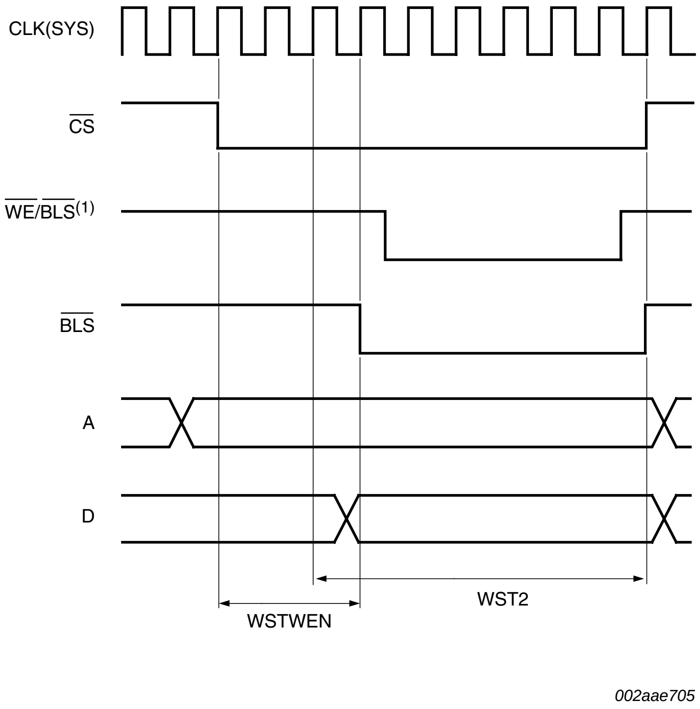
Fig 4. LPC2926/2927/2929 overview of clock areas



WSTOEN = 3, WST1 = 6

Fig 5. Reading from external memory

A timing diagram for writing to external memory is shown In Figure 6. The relationship between wait-state settings is indicated with arrows.



WSTWEN = 3, WST2 = 7

(1) $\overline{\text{BLS}}$ has the same timing as $\overline{\text{WE}}$ in configurations that use the byte lane enable signals to connect to write enable (8 bit devices).

Fig 6. Writing to external memory

The USB OTG controller has the following features:

- Fully compliant with *On-The-Go supplement to the USB 2.0 Specification, Revision 1.0a*.
- Hardware support for Host Negotiation Protocol (HNP).
- Includes a programmable timer required for HNP and Session Request Protocol (SRP).
- Supports any OTG transceiver compliant with the *OTG Transceiver Specification (CEA-2011), Rev. 1.0*.

6.11.3 Pin description

Table 14. USB OTG port pins

Pin name	Direction	Description	Connection
USB_VBUS	I	V_{BUS} status input. When this function is not enabled via its corresponding PINSEL register, it is driven HIGH internally.	USB Connector
USB_D+	I/O	Positive differential data	USB Connector
USB_D–	I/O	Negative differential data	USB Connector
$\overline{\text{USB\_CONNECT}}$	O	SoftConnect control signal	Control
$\overline{\text{USB\_UP\_LED}}$	O	GoodLink LED control signal	Control
USB_SCL	I/O	I^2C serial clock	External OTG transceiver
USB_SDA	I/O	I^2C serial data	External OTG transceiver
USB_LS	O	Low speed status (applies to host functionality only)	External OTG transceiver
$\overline{\text{USB\_RST}}$	O	USB reset status	External OTG transceiver
$\overline{\text{USB\_INT}}$	O	USB transceiver interrupt	External OTG transceiver
USB_SSPND	O	Bus suspend status	External OTG transceiver

6.11.4 Clock description

Access to the USB registers is clocked by the CLK_SYS_USB, derived from BASE_SYS_CLK, see Section 6.7.2. The CGU1 provides two independent base clocks to the USB block, BASE_USB_CLK and BASE_USB_I2C_CLK (see Section 6.16.3).

- Debug mode with disabling of reset
- Watchdog control register change-protected with key
- Programmable 32-bit watchdog timer period with programmable 32-bit prescaler.

6.13.2.1 Functional description

The watchdog timer consists of a 32-bit counter with a 32-bit prescaler.

The watchdog should be programmed with a time-out value and then periodically restarted. When the watchdog times out, it generates a reset through the RGU.

To generate watchdog interrupts in watchdog debug mode the interrupt has to be enabled via the interrupt enable register. A watchdog-overflow interrupt can be cleared by writing to the clear-interrupt register.

Another way to prevent resets during debug mode is via the Pause feature of the watchdog timer. The watchdog is stalled when the ARM9 is in debug mode and the PAUSE_ENABLE bit in the watchdog timer control register is set.

The Watchdog Reset output is fed to the Reset Generator Unit (RGU). The RGU contains a reset source register to identify the reset source when the device has gone through a reset. See Section 6.16.4.

6.13.2.2 Clock description

The watchdog timer is clocked by two different clocks; CLK_SYS_PESS and CLK_SAFE, see Section 6.7.2. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_SAFE which is always on.

6.13.3 Timer

The LPC2926/2927/2929 contains six identical timers: four in the peripheral subsystem and two in the Modulation and Sampling Control SubSystem (MSCSS) located at different peripheral base addresses. This section describes the four timers in the peripheral subsystem. Each timer has four capture inputs and/or match outputs. Connection to device pins depends on the configuration programmed into the port function-select registers. The two timers located in the MSCSS have no external capture or match pins, but the memory map is identical, see Section 6.15.6. One of these timers has an external input for a pause function.

The key features are:

- 32-bit timer/counter with programmable 32-bit prescaler
- Up to four 32-bit capture channels per timer. These take a snapshot of the timer value when an external signal connected to the TIMERx CAPn input changes state. A capture event may also optionally generate an interrupt
- Four 32-bit match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation

- Up to four external outputs per timer corresponding to match registers, with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Pause input pin (MSCSS timers only)

The timers are designed to count cycles of the clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. They also include capture inputs to trap the timer value when an input signal changes state, optionally generating an interrupt. The core function of the timers consists of a 32 bit prescale counter triggering the 32 bit timer counter. Both counters run on clock CLK_TMRx (x runs from 0 to 3) and all time references are related to the period of this clock. Note that each timer has its individual clock source within the Peripheral SubSystem. In the Modulation and Sampling SubSystem each timer also has its own individual clock source. See Section 6.16.5 for information on generation of these clocks.

6.13.3.1 Pin description

The four timers in the peripheral subsystem of the LPC2926/2927/2929 have the pins described below. The two timers in the modulation and sampling subsystem have no external pins except for the pause pin on MSCSS timer 1. See Section 6.15.6 for a description of these timers and their associated pins. The timer pins are combined with other functions on the port pins of the LPC2926/2927/2929, see Section 6.12.3. Table 16 shows the timer pins (x runs from 0 to 3).

Table 16. Timer pins

Note that CAP0 and CAP1 are not pinned out on Timer1.

Symbol	Pin name	Direction	Description
TIMERx CAP[0]	CAPx[0]	IN	TIMER x capture input 0
TIMERx CAP[1]	CAPx[1]	IN	TIMER x capture input 1
TIMERx CAP[2]	CAPx[2]	IN	TIMER x capture input 2
TIMERx CAP[3]	CAPx[3]	IN	TIMER x capture input 3
TIMERx MAT[0]	MATx[0]	OUT	TIMER x match output 0
TIMERx MAT[1]	MATx[1]	OUT	TIMER x match output 1
TIMERx MAT[2]	MATx[2]	OUT	TIMER x match output 2
TIMERx MAT[3]	MATx[3]	OUT	TIMER x match output 3

6.13.3.2 Clock description

The timer modules are clocked by two different clocks; CLK_SYS_PESS and CLK_TMRx (x = 0 to 3), see Section 6.7.2. Note that each timer has its own CLK_TMRx branch clock for power management. The frequency of all these clocks is identical as they are derived from the same base clock BASE_CLK_TMR. The register interface towards the system bus is clocked by CLK_SYS_PESS. The timer and prescale counters are clocked by CLK_TMRx.

6.13.4 UARTs

The LPC2926/2927/2929 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs.
- Register locations conform to 550 industry standard.
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes.
- Built-in baud rate generator.
- Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART is commonly used to implement a serial interface such as RS232. The LPC2926/2927/2929 contains two industry-standard 550 UARTs with 16-byte transmit and receive FIFOs, but they can also be put into 450 mode without FIFOs.

Remark: The LIN controller can be configured to provide two additional standard UART interfaces (see Section 6.14.2).

6.13.4.1 Pin description

The UART pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 17 shows the UART pins (x runs from 0 to 1).

Table 17. UART pins

Symbol	Pin name	Direction	Description
UARTx TXD	TXDx	OUT	UART channel x transmit data output
UARTx RXD	RXDx	IN	UART channel x receive data input

6.13.4.2 Clock description

The UART modules are clocked by two different clocks; CLK_SYS_PESS and CLK_UARTx (x = 0 to 1), see Section 6.7.2. Note that each UART has its own CLK_UARTx branch clock for power management. The frequency of all CLK_UARTx clocks is identical since they are derived from the same base clock BASE_CLK_UART. The register interface towards the system bus is clocked by CLK_SYS_PESS. The baud generator is clocked by the CLK_UARTx.

6.13.5 Serial Peripheral Interface (SPI)

The LPC2926/2927/2929 contains three Serial Peripheral Interface modules (SPIs) to allow synchronous serial communication with slave or master peripherals.

The key features are:

- Master or slave operation.
- Each SPI supports up to four slaves in sequential multi-slave operation.
- Supports timer-triggered operation.
- Programmable clock bit rate and prescale based on SPI source clock (BASE_SPI_CLK), independent of system clock.
- Separate transmit and receive FIFO memory buffers; 16 bits wide, 32 locations deep.

Table 23. ADC pins

Symbol	Pin name	Direction	Description
ADC0 IN[7:0]	IN0[7:0]	IN	analog input for 5.0 V ADC0, channel 7 to channel 0.
ADC1/2 IN[7:0]	IN1/2[7:0]	IN	analog input for 3.3 V ADC1/2, channel 7 to channel 0.
ADC2_EXT_START	CAP1[2]	IN	ADC external start-trigger input.
VREFN	VREFN	IN	ADC LOW reference level.
VREFP	VREFP	IN	ADC HIGH reference level.
$V_{DDA(ADC5V0)}$	$V_{DDA(ADC5V0)}$[1]	IN	5 V high-power supply and HIGH reference for ADC0. Connect to clean 5 V as HIGH reference. May also be connected to 3.3 V if 3.3 V measurement range for ADC0 is needed.[2][3]
$V_{DDA(ADC3V3)}$	$V_{DDA(ADC3V3)}$	IN	ADC1 and ADC2 3.3 V supply (also used for ADC0).[3]

[1] VREFP, VREFN, $V_{DDA(ADC3V3)}$ must be connected for the 5 V ADC0 to operate properly.

[2] The analog inputs of ADC0 are internally multiplied by a factor of 3.3 / 5. If $V_{DDA(ADC5V0)}$ is connected to 3.3 V, the maximum digital result is 1024 × 3.3 / 5.

[3] $V_{DDA(ADC5V0)}$ and $V_{DDA(ADC3V3)}$ must be set as follows: $V_{DDA(ADC5V0)} = V_{DDA(ADC3V3)} \times 1.5$.

Remark: The following formula only applies to ADC0:

Voltage variations on VREFP (i.e. those that deviate from voltage variations on the $V_{DDA(ADC5V5)}$ pin) are visible as variations in the measurement result. The following formula is used to determine the conversion result of an input voltage V_I on ADC0:

$$\left(\frac{2}{3}\left(V_I - \frac{1}{2}V_{DDA(ADC5V0)}\right) + \frac{1}{2}V_{DDA(ADC3V3)}\right) \times \frac{1024}{V_{VREFP} - V_{VREFN}} \tag{3}$$

Remark: Note that the ADC1 and ADC2 accept an input voltage up to of 3.6 V (see Table 34) on the ADC1/2 IN pins. If the ADC is not used, the pins are 5 V tolerant. The ADC0 pins are 5 V tolerant.

6.15.4.3 Clock description

The ADC modules are clocked from two different sources; CLK_MSCSS_ADCx_APB and CLK_ADCx (x = 0, 1, or 2), see Section 6.7.2. Note that each ADC has its own CLK_ADCx and CLK_MSCSS_ADCx_APB branch clocks for power management. If an ADC is unused both its CLK_MSCSS_ADCx_APB and CLK_ADCx can be switched off.

The frequency of all the CLK_MSCSS_ADCx_APB clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK. Likewise the frequency of all the CLK_ADCx clocks is identical since they are derived from the same base clock BASE_ADC_CLK.

The register interface towards the system bus is clocked by CLK_MSCSS_ADCx_APB. Control logic for the analog section of the ADC is clocked by CLK_ADCx, see also Figure 9.

6.15.5 Pulse Width Modulator (PWM)

The MSCSS in the LPC2926/2927/2929 includes four PWM modules with the following features.

- Six pulse-width modulated output signals
- Double edge features (rising and falling edges programmed individually)
- Optional interrupt generation on match (each edge)
- Different operation modes: continuous or run-once
- 16-bit PWM counter and 16-bit prescale counter allow a large range of PWM periods
- A protective mode (TRAP) holding the output in a software-controllable state and with optional interrupt generation on a trap event
- Three capture registers and capture trigger pins with optional interrupt generation on a capture event
- Interrupt generation on match event, capture event, PWM counter overflow or trap event
- A burst mode mixing the external carrier signal with internally generated PWM
- Programmable sync-delay output to trigger other PWM modules (master/slave behavior)

6.15.5.1 Functional description

The ability to provide flexible waveforms allows PWM blocks to be used in multiple applications; e.g. dimmer/lamp control and fan control. Pulse-width modulation is the preferred method for regulating power since no additional heat is generated, and it is energy-efficient when compared with linear-regulating voltage control networks.

The PWM delivers the waveforms/pulses of the desired duty cycles and cycle periods. A very basic application of these pulses can be in controlling the amount of power transferred to a load. Since the duty cycle of the pulses can be controlled, the desired amount of power can be transferred for a controlled duration. Two examples of such applications are:

- Dimmer controller: The flexibility of providing waves of a desired duty cycle and cycle period allows the PWM to control the amount of power to be transferred to the load. The PWM functions as a dimmer controller in this application.
- Motor controller: The PWM provides multi-phase outputs, and these outputs can be controlled to have a certain pattern sequence. In this way the force/torque of the motor can be adjusted as desired. This makes the PWM function as a motor drive.

6.15.5.3 Master and slave mode

A PWM module can provide synchronization signals to other modules (also called Master mode). The signal sync_out is a pulse of one clock cycle generated when the internal PWM counter (re)starts. The signal trans_enable_out is a pulse synchronous to sync_out, generated if a transfer from system registers to PWM shadow registers occurred when the PWM counter restarted. A delay may be inserted between the counter start and generation of trans_enable_out and sync_out.

A PWM module can use input signals trans_enable_in and sync_in to synchronize its internal PWM counter and the transfer of shadow registers (Slave mode).

6.15.5.4 Pin description

Each of the four PWM modules in the MSCSS has the following pins. These are combined with other functions on the port pins of the LPC2926/2927/2929. Table 24 shows the PWM0 to PWM3 pins.

Table 24. PWM pins

Symbol	Pin name	Direction	Description
PWMn CAP[0]	PCAPn[0]	IN	PWM n capture input 0
PWMn CAP[1]	PCAPn[1]	IN	PWM n capture input 1
PWMn CAP[2]	PCAPn[2]	IN	PWM n capture input 2
PWMn MAT[0]	PMATn[0]	OUT	PWM n match output 0
PWMn MAT[1]	PMATn[1]	OUT	PWM n match output 1
PWMn MAT[2]	PMATn[2]	OUT	PWM n match output 2
PWMn MAT[3]	PMATn[3]	OUT	PWM n match output 3
PWMn MAT[4]	PMATn[4]	OUT	PWM n match output 4
PWMn MAT[5]	PMATn[5]	OUT	PWM n match output 5
PWMn TRAP	TRAPn	IN	PWM n trap input

6.15.5.5 Clock description

The PWM modules are clocked by CLK_MSCSS_PWMx (x = 0 to 3), see Section 6.7.2. Note that each PWM has its own CLK_MSCSS_PWMx branch clock for power management. The frequency of all these clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

Also note that unlike the timer modules in the Peripheral SubSystem, the actual timer counter registers of the PWM modules run at the same clock as the APB system interface CLK_MSCSS_APB. This clock is independent of the AHB system clock.

If a PWM module is not used its CLK_MSCSS_PWMx branch clock can be switched off.

6.15.6 Timers in the MSCSS

The two timers in the MSCSS are functionally identical to the timers in the peripheral subsystem, see Section 6.13.3. The features of the timers in the MSCSS are the same as the timers in the peripheral subsystem, but the capture inputs and match outputs are not available on the device pins. These signals are instead connected to the ADC and PWM modules as outlined in the description of the MSCSS, see Section 6.15.1.

See Section 6.13.3 for a functional description of the timers.

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6.16.2 Clock Generation Unit (CGU0)

The key features are:

- Generation of 11 base clocks, selectable from several embedded clock sources.
- Crystal oscillator with power-down.
- Control PLL with power-down.
- Very low-power ring oscillator, always on to provide a safe clock.
- Individual source selector for each base clock, with glitch-free switching.
- Autonomous clock-activity detection on every clock source.
- Protection against switching to invalid or inactive clock sources.
- Embedded frequency counter.
- Register write-protection mechanism to prevent unintentional alteration of clocks.

Remark: Any clock-frequency adjustment has a direct impact on the timing of all on-board peripherals.

6.16.2.1 Functional description

The clock generation unit provides 11 internal clock sources as described in Table 27.

Table 27. CGU0 base clocks

Number	Name	Frequency (MHz) [1]	Description
0	BASE_SAFE_CLK	0.4	base safe clock (always on)
1	BASE_SYS_CLK	125	base system clock
2	BASE_PCR_CLK	0.4 [2]	base PCR subsystem clock
3	BASE_IVNSS_CLK	125	base IVNSS subsystem clock
4	BASE_MSCSS_CLK	125	base MSCSS subsystem clock
5	BASE_ICLK0_CLK	125	base internal clock 0, for CGU1
6	BASE_UART_CLK	125	base UART clock
7	BASE_SPI_CLK	50	base SPI clock
8	BASE_TMR_CLK	125	base timers clock
9	BASE_ADC_CLK	4.5	base ADCs clock
10	reserved	-	-
11	BASE_ICLK1_CLK	125	base internal clock 1, for CGU1

[1] Maximum frequency that guarantees stable operation of the LPC2926/2927/2929.

[2] Fixed to low-power oscillator.

For generation of these base clocks, the CGU consists of primary and secondary clock generators and one output generator for each base clock.

generator. The RDET register keeps track of which clocks are active and inactive, and the appropriate ‘CLK_SEL’ values are masked and unmasked accordingly. Each clock detector can also generate interrupts at clock activation and deactivation so that the system can be notified of a change in internal clock status.

Clock detection is done using a counter running at the *BASE_PCR_CLK* frequency. If no positive clock edge occurs before the counter has 32 cycles of BASE_PCR_CLK the clock is assumed to be inactive. As *BASE_PCR_CLK* is slower than any of the clocks to be detected, normally only one BASE_PCR_CLK cycle is needed to detect activity. After reset all clocks are assumed to be ‘non-present’, so the RDET status register will be correct only after 32 *BASE_PCR_CLK* cycles.

Note that this mechanism cannot protect against a currently-selected clock going from active to inactive state. Therefore an inactive clock may still be sent to the system under special circumstances, although an interrupt can still be generated to notify the system.

Glitch-Free Switching: Provisions are included in the CGU to allow clocks to be switched glitch-free, both at the output generator stage and also at secondary source generators.

In the case of the PLL the clock will be stopped and held low for long enough to allow the PLL to stabilize and lock before being re-enabled. For all non-PLL Generators the switch will occur as quickly as possible, although there will always be a period when the clock is held low due to synchronization requirements.

If the current clock is high and does not go low within 32 *cycles of BASE_PCR_CLK* it is assumed to be inactive and is asynchronously forced low. This prevents deadlocks on the interface.

6.16.2.2 PLL functional description

A block diagram of the PLL is shown in Figure 14. The input clock is fed directly to the analog section. This block compares the phase and frequency of the inputs and generates the main clock[2]. These clocks are either divided by 2 × P by the programmable post divider to create the output clock, or sent directly to the output. The main output clock is then divided by M by the programmable feedback divider to generate the feedback clock. The output signal of the analog section is also monitored by the lock detector to signal when the PLL has locked onto the input clock.

[2] Generation of the main clock is restricted by the frequency range of the PLL clock input. See Table 36, Dynamic characteristics.

Table 32. Branch clock overview *…continued*

Legend:

'1' Indicates that the related register bit is tied off to logic HIGH, all writes are ignored

'0' Indicates that the related register bit is tied off to logic LOW, all writes are ignored

'+' Indicates that the related register bit is readable and writable

Branch clock name	Base clock	Implemented switch on/off mechanism		
		WAKE-UP	AUTO	RUN
CLK_MSCSS_ADC2_APB	BASE_MSCSS_CLK	+	+	+
CLK_MSCSS_QEI	BASE_MSCSS_CLK	+	+	+
CLK_OUT_CLK	BASE_OUT_CLK	+	+	+
CLK_UART0	BASE_UART_CLK	+	+	+
CLK_UART1	BASE_UART_CLK	+	+	+
CLK_SPI0	BASE_SPI_CLK	+	+	+
CLK_SPI1	BASE_SPI_CLK	+	+	+
CLK_SPI2	BASE_SPI_CLK	+	+	+
CLK_TMR0	BASE_TMR_CLK	+	+	+
CLK_TMR1	BASE_TMR_CLK	+	+	+
CLK_TMR2	BASE_TMR_CLK	+	+	+
CLK_TMR3	BASE_TMR_CLK	+	+	+
CLK_ADC0	BASE_ADC_CLK	+	+	+
CLK_ADC1	BASE_ADC_CLK	+	+	+
CLK_ADC2	BASE_ADC_CLK	+	+	+
CLK_USB_I2C	BASE_USB_I2C_CLK	+	+	+
CLK_USB	BASE_USB_CLK	+	+	+

6.17 Vectored Interrupt Controller (VIC)

The LPC2926/2927/2929 contains a very flexible and powerful Vectored Interrupt Controller to interrupt the ARM processor on request.

The key features are:

- Level-active interrupt request with programmable polarity.
- 56 interrupt request inputs.
- Software interrupt request capability associated with each request input.
- Interrupt request state can be observed before masking.
- Software-programmable priority assignments to interrupt requests up to 15 levels.
- Software-programmable routing of interrupt requests towards the ARM-processor inputs IRQ and FIQ.
- Fast identification of interrupt requests through vector.
- Support for nesting of interrupt service routines.

Table 34. Static characteristics *…continued*

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(ADC5V0)}$ = 3.0 V to 5.5 V; T_{vj} = −40 °C to +85 °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS, TCK	-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
I_{LIH}	HIGH-level input leakage current		-	-	1	μA
I_{LIL}	LOW-level input leakage current		-	-	1	μA
$I_{I(pd)}$	pull-down input current	all port pins, V_I = 3.3 V; V_I = 5.5 V	25	50	100	μA
$I_{I(pu)}$	pull-up input current	all port pins, $\overline{RST}$, $\overline{TRST}$, TDI, JTAGSEL, TMS: V_I = 0 V; V_I > 3.6 V is not allowed	−25	−50	−115	μA
C_i	input capacitance	[7]	-	3	8	pF
Output pins and I/O pins configured as output						
V_O	output voltage		0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
C_L	load capacitance		-	-	25	pF
USB pins USB_D+ and USB_D−						
Input characteristics						
V_{IH}	HIGH-level input voltage		1.5	-	-	V
V_{IL}	LOW-level input voltage		-	-	1.3	V
V_{hys}	hysteresis voltage		0.4	-	-	V
Output characteristics						
Z_o	output impedance	with 33 Ω series resistor	36.0	-	44.1	Ω
V_{OH}	HIGH-level output voltage	(driven) for low-/full-speed; R_L of 15 kΩ to GND	2.9	-	3.5	V
V_{OL}	LOW-level output voltage	(driven) for low-/full-speed; with 1.5 kΩ resistor to 3.6 V external pull-up	-	-	0.18	V
I_{OH}	HIGH-level output current	at V_{OH} = $V_{DD(IO)}$ − 0.3 V; without 33 Ω external series resistor	20.8	-	41.7	mA
		at V_{OH} = $V_{DD(IO)}$ − 0.3 V; with 33 Ω external series resistor	4.8	-	5.3	mA

Table 35. ADC static characteristics

$V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{VREFN}	voltage on pin VREFN			0	-	V_{VREFP} − 2	V
V_{VREFP}	voltage on pin VREFP			V_{VREFN} + 2	-	$V_{DDA(ADC3V3)}$	V
V_{IA}	analog input voltage	for 3.3 V ADC1/2		V_{VREFN}	-	V_{VREFP}	V
Z_i	input impedance	between V_{VREFN} and V_{VREFP}		4.4	-	-	kΩ
		between V_{VREFN} and $V_{DDA(ADC5V0)}$		13.7	-	23.6	kΩ
C_{ia}	analog input capacitance	for ADC0/1/2		-	-	1	pF
E_D	differential linearity error	for ADC0/1/2	[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	for ADC0/1/2	[1][4]	-	-	±2	LSB
E_O	offset error	for ADC0/1/2	[1][5]	-	-	±3	LSB
E_G	gain error	for ADC0/1/2	[1][6]	-	-	±0.5	%
E_T	absolute error	for ADC0/1/2	[1][7]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance	for ADC0/1/2	[8]	-	-	40	kΩ
FSR	full scale range	for ADC0/1/2		2	-	10	bit

[1] Conditions: $V_{SS(IO)}$ = 0 V, $V_{DDA(ADC3V3)}$ = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 17.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 17.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 17.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 17.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 17.

[8] See Figure 16.

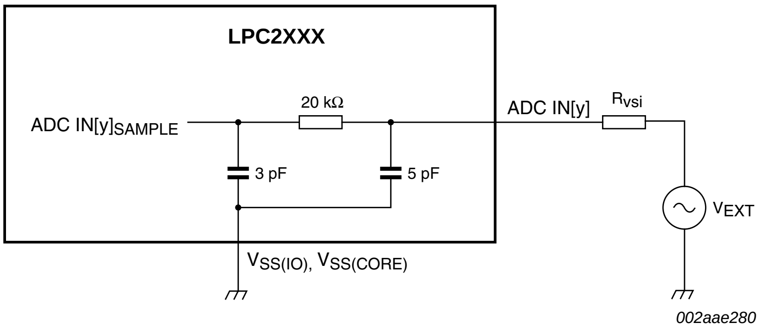
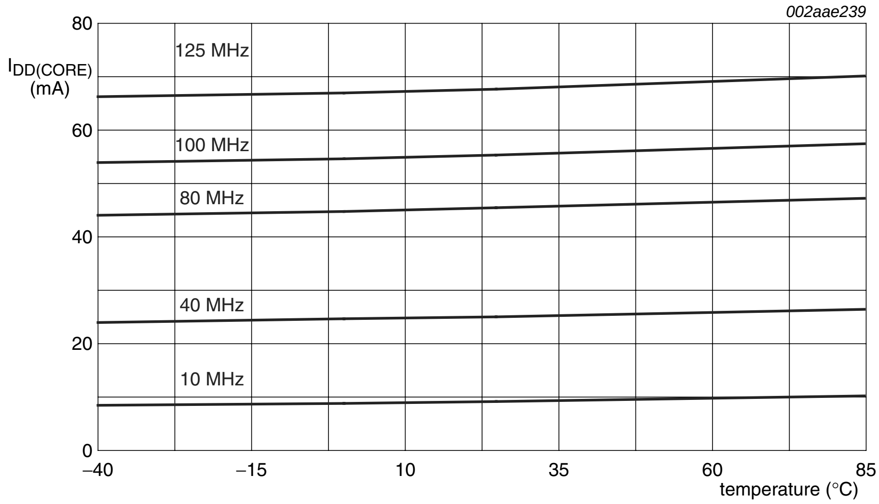


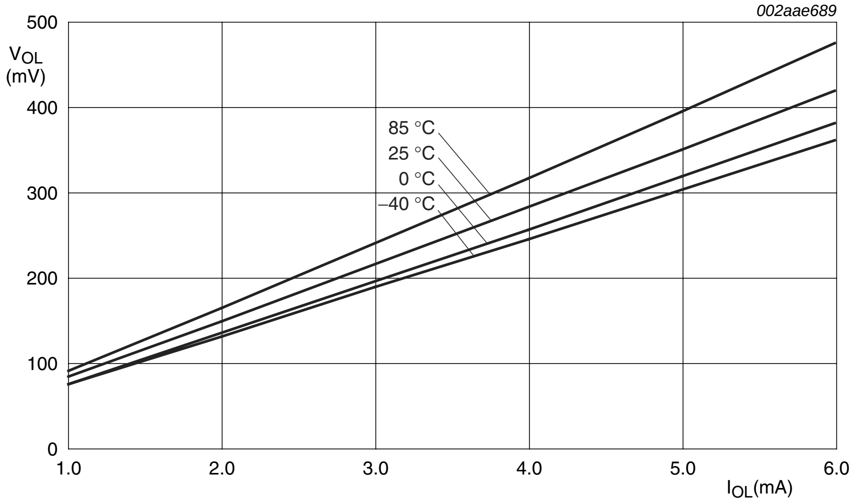
Fig 16. Suggested ADC interface - LPC2926/2927/2929 ADC1/2 IN[y] pin



Conditions: active mode entered executing code from flash; core voltage 1.8 V; all peripherals enabled but not configured to run.

Fig 20. $I_{DD(CORE)}$ at different temperatures (active mode)

8.2 Electrical pin characteristics



$V_{DD(IO)}$ = 3.3 V.

Fig 21. Typical LOW-level output voltage versus LOW-level output current

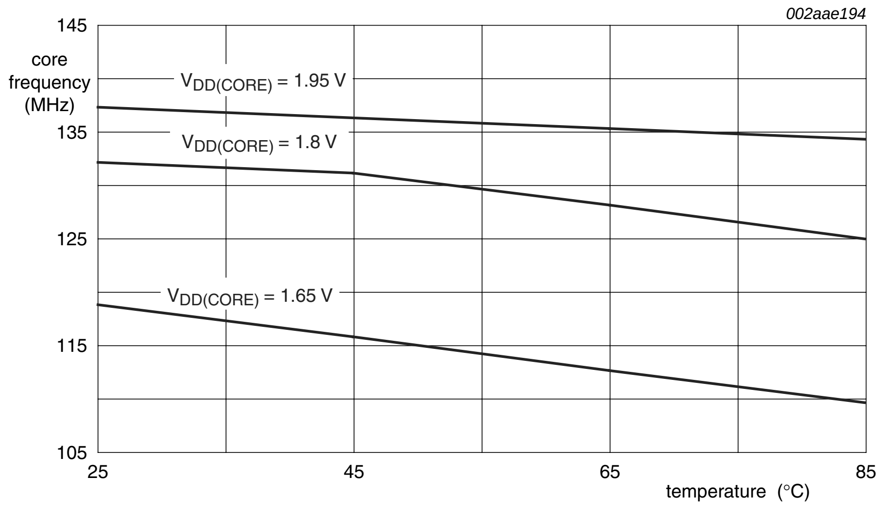


Fig 30. Core operating frequency versus temperature for different core voltages.

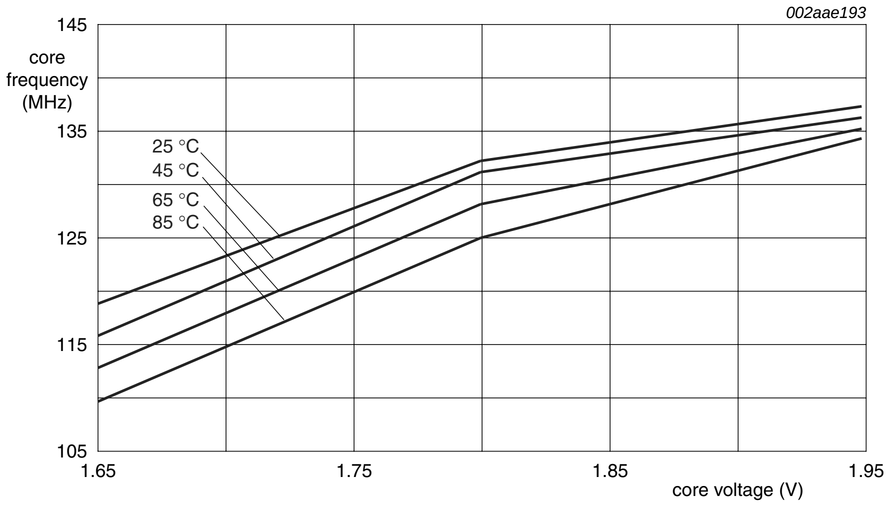
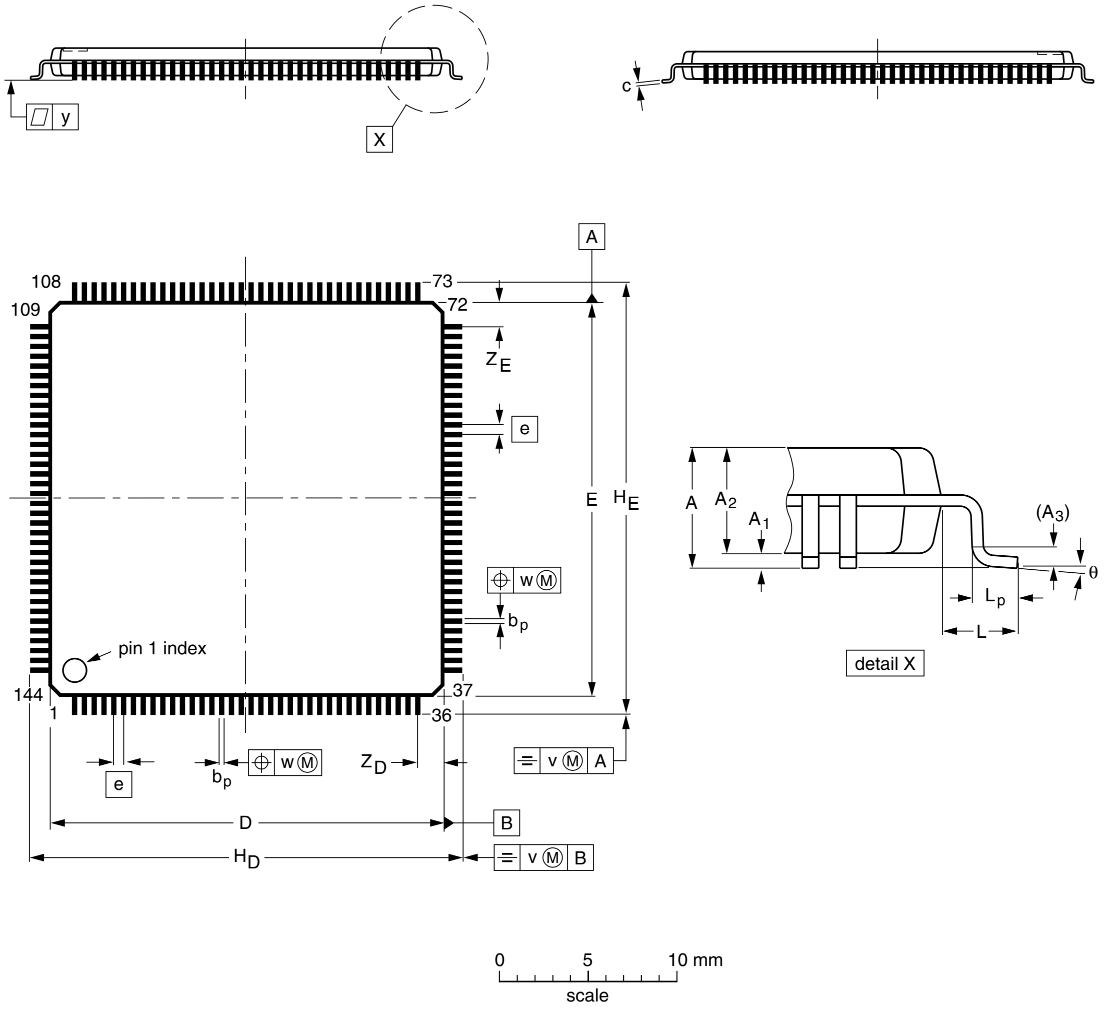


Fig 31. Core operating frequency versus core voltage for different temperatures

11. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 39. Package outline SOT486-1 (LQFP144)

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 40) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 44 and 45

Table 44. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 45. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 40.