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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM9®
Core Size	16/32-Bit
Speed	125MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2929fbd144-551

5. Pinning information

5.1 Pinning

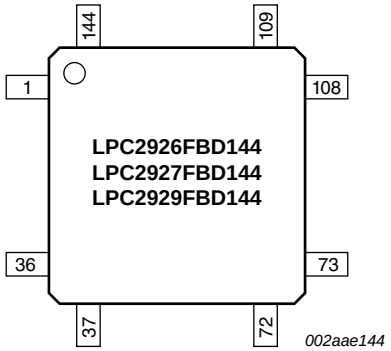


Fig 2. Pin configuration for SOT486-1 (LQFP144)

5.2 Pin description

5.2.1 General description

The LPC2926/2927/2929 uses five ports: port 0 with 32 pins, ports 1 and 2 with 28 pins each, port 3 with 16 pins, and port 5 with 2 pins. Port 4 is not used. The pin to which each function is assigned is controlled by the SFSP registers in the System Control Unit (SCU). The functions combined on each port pin are shown in the pin description tables in this section.

5.2.2 LQFP144 pin assignment

Table 3. LQFP144 pin assignment

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
TDO	1[1]	IEEE 1149.1 test data out			
P2[21]/SDI2/ PCAP2[1]/D19	2[1]	GPIO2, pin 21	SPI2 SDI	PWM2 CAP1	EXTBUS D19
P0[24]/TXD1/ TXDC1/SCS2[0]	3[1]	GPIO0, pin 24	UART1 TXD	CAN1 TXD	SPI2 SCS0
P0[25]/RXD1/ RXDC1/SDO2	4[1]	GPIO0, pin 25	UART1 RXD	CAN1 RXD	SPI2 SDO
P0[26]/TXD1/SDI2	5[1]	GPIO0, pin 26	-	UART1 TXD	SPI2 SDI
P0[27]/RXD1/SCK2	6[1]	GPIO0, pin 27	-	UART1 RXD	SPI2 SCK
P0[28]/CAP0[0]/ MAT0[0]	7[1]	GPIO0, pin 28	-	TIMER0 CAP0	TIMER0 MAT0
P0[29]/CAP0[1]/ MAT0[1]	8[1]	GPIO0, pin 29	-	TIMER0 CAP1	TIMER0 MAT1
$V_{DD(IO)}$	9	3.3 V power supply for I/O			

Table 3. LQFP144 pin assignment *…continued*

Pin name	Pin	Description			
		Function 0 (default)	Function 1	Function 2	Function 3
P2[22]/SCK2/ PCAP2[2]/D20	10[1]	GPIO2, pin 22	SPI2 SCK	PWM2 CAP2	EXTBUS D20
P2[23]/SCS1[0]/ PCAP3[0]/D21	11[1]	GPIO2, pin 23	SPI1 SCS0	PWM3 CAP0	EXTBUS D21
P3[6]/SCS0[3]/ PMAT1[0]/TXDL1	12[1]	GPIO3, pin 6	SPI0 SCS3	PWM1 MAT0	LIN1/UART TXD
P3[7]/SCS2[1]/ PMAT1[1]/RXDL1	13[1]	GPIO3, pin 7	SPI2 SCS1	PWM1 MAT1	LIN1/UART RXD
P0[30]/CAP0[2]/ MAT0[2]	14[1]	GPIO0, pin 30	-	TIMER0 CAP2	TIMER0 MAT2
P0[31]/CAP0[3]/ MAT0[3]	15[1]	GPIO0, pin 31	-	TIMER0 CAP3	TIMER0 MAT3
P2[24]/SCS1[1]/ PCAP3[1]/D22	16[1]	GPIO2, pin 24	SPI1 SCS1	PWM3 CAP1	EXTBUS D22
P2[25]/SCS1[2]/ PCAP3[2]/D23	17[1]	GPIO2, pin 25	SPI1 SCS2	PWM3 CAP2	EXTBUS D23
$V_{SS(IO)}$	18	ground for I/O			
P5[19]/USB_D+	19[2]	GPIO5, pin 19	USB_D+	-	-
P5[18]/USB_D–	20[2]	GPIO5, pin 18	USB_D–	-	-
$V_{DD(IO)}$	21	3.3 V power supply for I/O			
$V_{DD(CORE)}$	22	1.8 V power supply for digital core			
$V_{SS(CORE)}$	23	ground for core			
$V_{SS(IO)}$	24	ground for I/O			
P3[8]/SCS2[0]/ PMAT1[2]	25[1]	GPIO3, pin 8	SPI2 SCS0	PWM1 MAT2	-
P3[9]/SDO2/ PMAT1[3]	26[1]	GPIO3, pin 9	SPI2 SDO	PWM1 MAT3	-
P2[26]/CAP0[2]/ MAT0[2]/EI6	27[1]	GPIO2, pin 26	TIMER0 CAP2	TIMER0 MAT2	EXTINT6
P2[27]/CAP0[3]/ MAT0[3]/EI7	28[1]	GPIO2, pin 27	TIMER0 CAP3	TIMER0 MAT3	EXTINT7
P1[27]/CAP1[2]/ TRAP2/PMAT3[3]	29[1]	GPIO1, pin 27	TIMER1 CAP2, ADC2 EXT START	PWM TRAP2	PWM3 MAT3
P1[26]/PMAT2[0]/ TRAP3/PMAT3[2]	30[1]	GPIO1, pin 26	PWM2 MAT0	PWM TRAP3	PWM3 MAT2
$V_{DD(IO)}$	31	3.3 V power supply for I/O			
P1[25]/PMAT1[0]/ USB_VBUS/ PMAT3[1]	32[1]	GPIO1, pin 25	PWM1 MAT0	USB_VBUS	PWM3 MAT1
P1[24]/PMAT0[0]/ $\overline{\text{USB\_CONNECT}}$/ PMAT3[0]	33[1]	GPIO1, pin 24	PWM0 MAT0	$\overline{\text{USB\_CONNECT}}$	PWM3 MAT0
P1[23]/RXD0/ USB_SSPND/$\overline{\text{CS5}}$	34[1]	GPIO1, pin 23	UART0 RXD	USB_SSPND	EXTBUS $\overline{\text{CS5}}$

6.5 Memory map

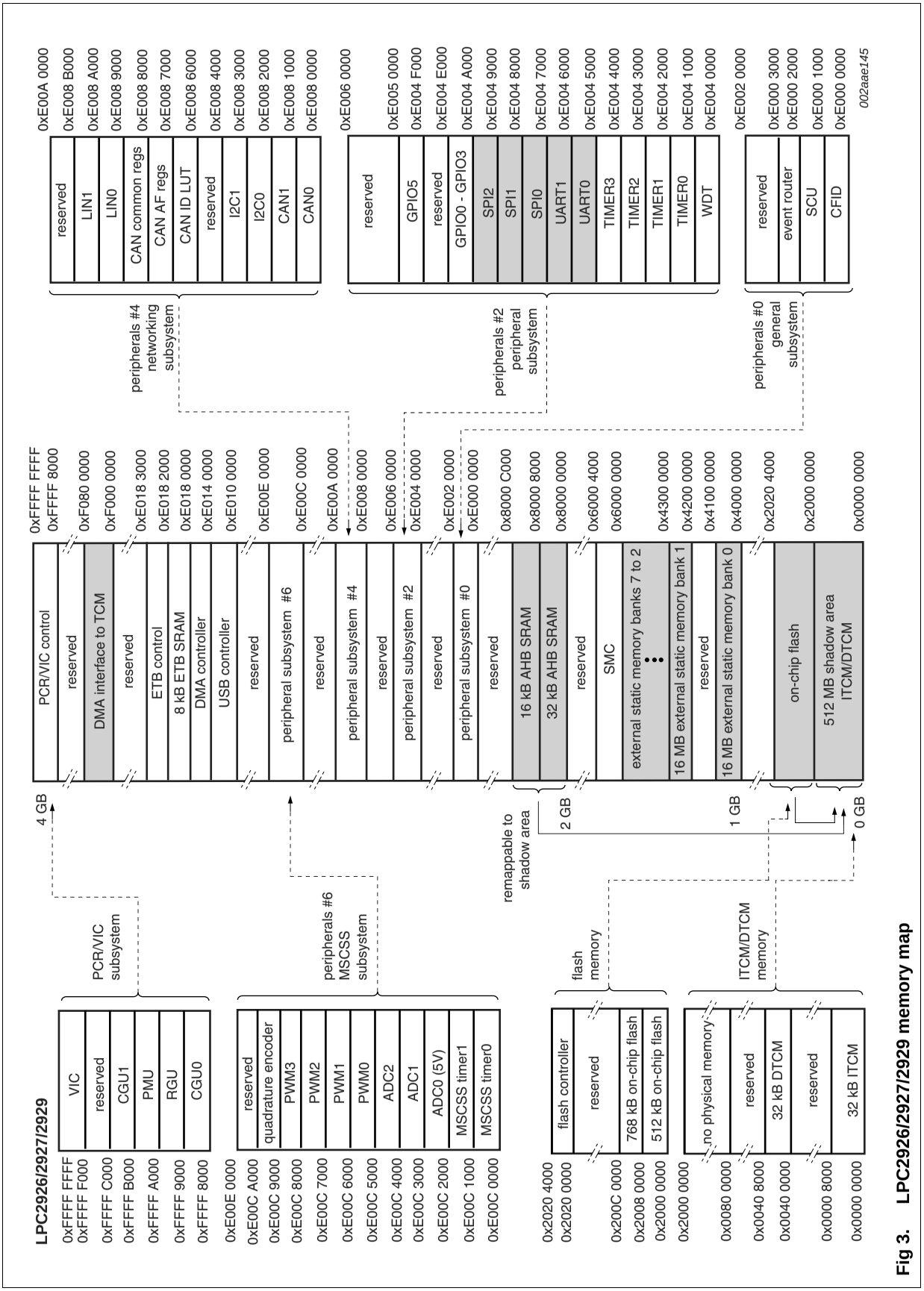


Fig 3. LPC2926/2927/2929 memory map

6.6 Reset, debug, test, and power description

6.6.1 Reset and power-up behavior

The LPC2926/2927/2929 contains external reset input and internal power-up reset circuits. This ensures that a reset is extended internally until the oscillators and flash have reached a stable state. See Section 8 for trip levels of the internal power-up reset circuit[1]. See Section 9 for characteristics of the several start-up and initialization times. Table 4 shows the reset pin.

Table 4. Reset pin

Symbol	Direction	Description
$\overline{\text{RST}}$	IN	external reset input, active LOW; pulled up internally

At activation of the $\overline{\text{RST}}$ pin the JTAGSEL pin is sensed as logic LOW. If this is the case the LPC2926/2927/2929 is assumed to be connected to debug hardware, and internal circuits re-program the source for the BASE_SYS_CLK to be the crystal oscillator instead of the Low-Power Ring Oscillator (LP_OSC). This is required because the clock rate when running at LP_OSC speed is too low for the external debugging environment.

6.6.2 Reset strategy

The LPC2926/2927/2929 contains a central module, the Reset Generator Unit (RGU) in the Power, Clock and Reset Subsystem (PCRSS), which controls all internal reset signals towards the peripheral modules. The RGU provides individual reset control as well as the monitoring functions needed for tracing a reset back to source.

6.6.3 IEEE 1149.1 interface pins (JTAG boundary scan test)

The LPC2926/2927/2929 contains boundary-scan test logic according to IEEE 1149.1, also referred to in this document as Joint Test Action Group (JTAG). The boundary-scan test pins can be used to connect a debugger probe for the embedded ARM processor. Pin JTAGSEL selects between boundary-scan mode and debug mode. Table 5 shows the boundary scan test pins.

Table 5. IEEE 1149.1 boundary-scan test and debug interface

Symbol	Description
JTAGSEL	TAP controller select input. LOW level selects ARM debug mode and HIGH level selects boundary scan and flash programming; pulled up internally
$\overline{\text{TRST}}$	test reset input; pulled up internally (active LOW)
TMS	test mode select input; pulled up internally
TDI	test data input, pulled up internally
TDO	test data output
TCK	test clock input

1. Only for 1.8 V power sources

6.6.3.1 ETM/ETB

The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to a trace buffer. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured in a format that a user can easily understand. The ETB stores trace data produced by the ETM.

The ETM/ETB module has the following features:

- Closely tracks the instructions that the ARM core is executing.
- On-chip trace data storage (ETB).
- All registers are programmed through JTAG interface.
- Does not consume power when trace is not being used.
- THUMB/Java instruction set support.

6.6.4 Power supply pins

Table 6 shows the power supply pins.

Table 6. Power supply pins

Symbol	Description
$V_{DD(CORE)}$	digital core supply 1.8 V
$V_{SS(CORE)}$	digital core ground (digital core, ADC0/1/2)
$V_{DD(IO)}$	I/O pins supply 3.3 V
$V_{SS(IO)}$	I/O pins ground
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply
$V_{SS(OSC)}$	oscillator ground
$V_{SS(PLL)}$	PLL ground
$V_{DDA(ADC3V3)}$	ADC1 and ADC2 3.3 V supply
$V_{DDA(ADC5V0)}$	ADC0 5.0 V supply

6.7 Clocking strategy

6.7.1 Clock architecture

The LPC2926/2927/2929 contains several different internal clock areas. Peripherals like Timers, SPI, UART, CAN and LIN have their own individual clock sources called base clocks. All base clocks are generated by the Clock Generator Unit (CGU0). They may be unrelated in frequency and phase and can have different clock sources within the CGU.

The system clock for the CPU and AHB Bus infrastructure has its own base clock. This means most peripherals are clocked independently from the system clock. See Figure 4 for an overview of the clock areas within the device.

Within each clock area there may be multiple branch clocks, which offers very flexible control for power-management purposes. All branch clocks are outputs of the Power Management Unit (PMU) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase. See Section 6.16 for more details of clock and power control within the device.

Two of the base clocks generated by the CGU0 are used as input into a second, dedicated CGU (CGU1). The CGU1 uses its own PLL and fractional dividers to generate two base clocks for the USB controller and one base clock for an independent clock output.

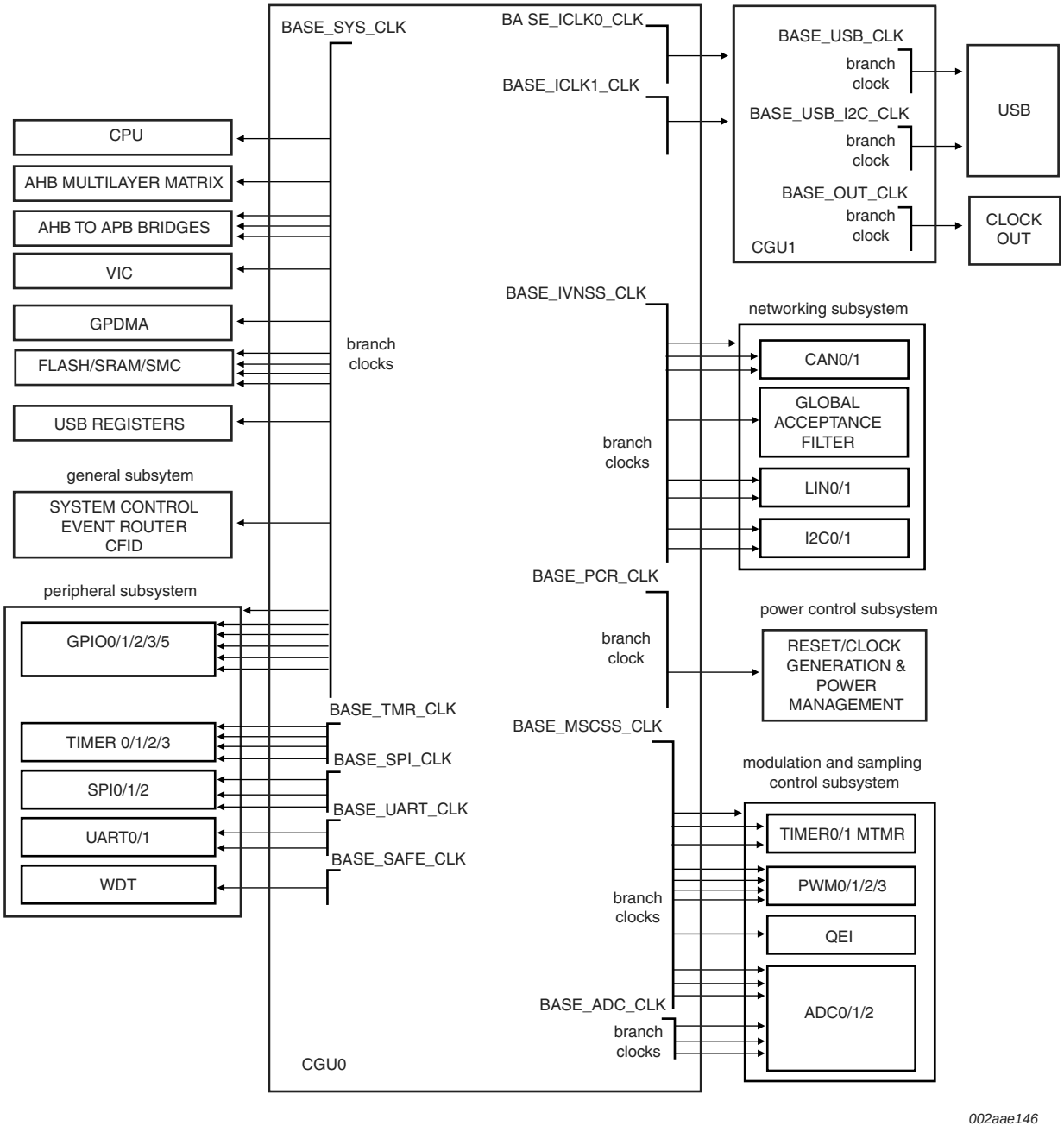


Fig 4. LPC2926/2927/2929 overview of clock areas

6.7.2 Base clock and branch clock relationship

Table 7 contains an overview of all the base blocks in the LPC2926/2927/2929 and their derived branch clocks. A short description is given of the hardware parts that are clocked with the individual branch clocks. In relevant cases more detailed information can be found in the specific subsystem description. Some branch clocks have special protection since they clock vital system parts of the device and should not be switched off. See Section 6.16.5 for more details of how to control the individual branch clocks.

Table 7. CGU0 base clock and branch clock overview

Base clock	Branch clock name	Parts of the device clocked by this branch clock	Remark
BASE_SAFE_CLK	CLK_SAFE	watchdog timer	[1]
BASE_SYS_CLK	CLK_SYS_CPU	ARM968E-S and TCMs	
	CLK_SYS_SYS	AHB bus infrastructure	
	CLK_SYS_PCRSS	AHB side of bridge in PCRSS	
	CLK_SYS_FMC	Flash Memory Controller	
	CLK_SYS_RAM0	Embedded SRAM Controller 0 (32 kB)	
	CLK_SYS_RAM1	Embedded SRAM Controller 1 (16 kB)	
	CLK_SYS_SMC	External Static Memory Controller	
	CLK_SYS_GESS	General Subsystem	
	CLK_SYS_VIC	Vectored Interrupt Controller	
	CLK_SYS_PESS	Peripheral Subsystem	[2][3]
	CLK_SYS_GPIO0	GPIO bank 0	
	CLK_SYS_GPIO1	GPIO bank 1	
	CLK_SYS_GPIO2	GPIO bank 2	
	CLK_SYS_GPIO3	GPIO bank 3	
	CLK_SYS_GPIO5	GPIO bank 5	
	CLK_SYS_IVNSS_A	AHB side of bridge of IVNSS	
	CLK_SYS_MSCSS_A	AHB side of bridge of MSCSS	
	CLK_SYS_DMA	GPDMA	
	CLK_SYS_USB	USB registers	
BASE_PCR_CLK	CLK_PCR_SLOW	PCRSS, CGU, RGU and PMU logic clock	[1][4]
BASE_IVNSS_CLK	CLK_IVNSS_APB	APB side of the IVNSS	
	CLK_IVNSS_CANCA	CAN controller Acceptance Filter	
	CLK_IVNSS_CANC0	CAN channel 0	
	CLK_IVNSS_CANC1	CAN channel 1	
	CLK_IVNSS_I2C0	I2C0	
	CLK_IVNSS_I2C1	I2C1	
	CLK_IVNSS_LIN0	LIN channel 0	
	CLK_IVNSS_LIN1	LIN channel 1	

Table 10 gives an overview of the flash-sector base addresses.

Table 10. Flash sector overview

Sector number	Sector size (kB)	Sector base address
11	8	0x2000 0000
12	8	0x2000 2000
13	8	0x2000 4000
14	8	0x2000 6000
15	8	0x2000 8000
16	8	0x2000 A000
17	8	0x2000 C000
18	8	0x2000 E000
0	64	0x2001 0000
1	64	0x2002 0000
2	64	0x2003 0000
3[1]	64	0x2004 0000
4[1]	64	0x2005 0000
5[1]	64	0x2006 0000
6[1]	64	0x2007 0000
7[1]	64	0x2008 0000
8[1]	64	0x2009 0000
9[1]	64	0x200A 0000
10[1]	64	0x200B 0000

[1] Availability of sector 3 to sector 10 depends on device type, see Section 3 “Ordering information”.

The index sector is a special sector in which the JTAG access protection and sector security are located. The address space becomes visible by setting the FS_ISS bit and overlaps the regular flash sector’s address space.

Note that the index sector, once programmed, cannot be erased. Any flash operation must be executed out of SRAM (internal or external).

6.8.5 Flash bridge wait-states

To eliminate the delay associated with synchronizing flash-read data, a predefined number of wait-states must be programmed. These depend on flash memory response time and system clock period. The minimum wait-states value can be calculated with the following formulas:

Synchronous reading:

$$WST > \frac{t_{acc(clk)}}{t_{t_{tclk(sys)}}} - 1 \quad (1)$$

Asynchronous reading:

$$WST > \frac{t_{acc(addr)}}{t_{tclk(sys)}} - 1 \quad (2)$$

6.13.4 UARTs

The LPC2926/2927/2929 contains two identical UARTs located at different peripheral base addresses. The key features are:

- 16-byte receive and transmit FIFOs.
- Register locations conform to 550 industry standard.
- Receiver FIFO trigger points at 1 byte, 4 bytes, 8 bytes and 14 bytes.
- Built-in baud rate generator.
- Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART is commonly used to implement a serial interface such as RS232. The LPC2926/2927/2929 contains two industry-standard 550 UARTs with 16-byte transmit and receive FIFOs, but they can also be put into 450 mode without FIFOs.

Remark: The LIN controller can be configured to provide two additional standard UART interfaces (see Section 6.14.2).

6.13.4.1 Pin description

The UART pins are combined with other functions on the port pins of the LPC2926/2927/2929. Table 17 shows the UART pins (x runs from 0 to 1).

Table 17. UART pins

Symbol	Pin name	Direction	Description
UARTx TXD	TXDx	OUT	UART channel x transmit data output
UARTx RXD	RXDx	IN	UART channel x receive data input

6.13.4.2 Clock description

The UART modules are clocked by two different clocks; CLK_SYS_PESS and CLK_UARTx (x = 0 to 1), see Section 6.7.2. Note that each UART has its own CLK_UARTx branch clock for power management. The frequency of all CLK_UARTx clocks is identical since they are derived from the same base clock BASE_CLK_UART. The register interface towards the system bus is clocked by CLK_SYS_PESS. The baud generator is clocked by the CLK_UARTx.

6.13.5 Serial Peripheral Interface (SPI)

The LPC2926/2927/2929 contains three Serial Peripheral Interface modules (SPIs) to allow synchronous serial communication with slave or master peripherals.

The key features are:

- Master or slave operation.
- Each SPI supports up to four slaves in sequential multi-slave operation.
- Supports timer-triggered operation.
- Programmable clock bit rate and prescale based on SPI source clock (BASE_SPI_CLK), independent of system clock.
- Separate transmit and receive FIFO memory buffers; 16 bits wide, 32 locations deep.

Figure 8 provides an overview of the MSCSS. An AHB-to-APB bus bridge takes care of communication with the AHB system bus. Two internal timers are dedicated to this subsystem. MSCSS timer 0 can be used to generate start pulses for the ADCs and the first PWM. The second timer (MSCSS timer 1) is used to generate ‘carrier’ signals for the PWMs. These carrier patterns can be used, for example, in applications requiring current control. Several other trigger possibilities are provided for the ADCs (external, cascaded or following a PWM). The capture inputs of both timers can also be used to capture the start pulse of the ADCs.

The PWMs can be used to generate waveforms in which the frequency, duty cycle and rising and falling edges can be controlled very precisely. Capture inputs are provided to measure event phases compared to the main counter. Depending on the applications, these inputs can be connected to digital sensor motor outputs or digital external signals. Interrupt signals are generated on several events to closely interact with the CPU.

The ADCs can be used for any application needing accurate digitized data from analog sources. To support applications like motor control, a mechanism to synchronize several PWMs and ADCs is available (sync_in and sync_out).

Note that the PWMs run on the PWM clock and the ADCs on the ADC clock, see Section 6.16.2.

6.15.2 Pin description

The pins of the LPC2926/2927/2929 MSCSS associated with the three ADC modules are described in Section 6.15.4.2. Pins connected to the four PWM modules are described in Section 6.15.5.4, pins directly connected to the MSCSS timer 1 module are described in Section 6.15.6.1, and pins connected to the quadrature encoder interface are described in Section 6.15.7.1.

6.15.3 Clock description

The MSCSS is clocked from a number of different sources:

- CLK_SYS_MSCSS_A clocks the AHB side of the AHB-to-APB bus bridge
- CLK_MSCSS_APB clocks the subsystem APB bus
- CLK_MSCSS_MTMR0/1 clocks the timers
- CLK_MSCSS_PWM[0:3] clocks the PWMs.

Each ADC has two clock areas; a APB part clocked by CLK_MSCSS_ADCx_APB (x = 0, 1, or 2) and a control part for the analog section clocked by CLK_ADCx = 0, 1, or 2), see Section 6.7.2.

All clocks are derived from the BASE_MSCSS_CLK, except for CLK_SYS_MSCSS_A which is derived form BASE_SYS_CLK, and the CLK_ADCx clocks which are derived from BASE_CLK_ADC. If specific PWM or ADC modules are not used their corresponding clocks can be switched off.

6.15.4 Analog-to-digital converter

The MSCSS in the LPC2926/2927/2929 includes three 10-bit successive-approximation analog-to-digital converters.

The key features of the ADC interface module are:

- ADC0: Eight analog inputs; time-multiplexed; measurement range up to 5.0 V.
- ADC1 and ADC2: Eight analog inputs; time-multiplexed; measurement range up to 3.3 V.
- External reference-level inputs.
- 400 ksamples per second at 10-bit resolution up to 1500 ksamples per second at 2-bit resolution.
- Programmable resolution from 2-bit to 10-bit.
- Single analog-to-digital conversion scan mode and continuous analog-to-digital conversion scan mode.
- Optional conversion on transition on external start input, timer capture/match signal, PWM_sync or ‘previous’ ADC.
- Converted digital values are stored in a register for each channel.
- Optional compare condition to generate a ‘less than’ or an ‘equal to or greater than’ compare-value indication for each channel.
- Power-down mode.

6.15.5.3 Master and slave mode

A PWM module can provide synchronization signals to other modules (also called Master mode). The signal sync_out is a pulse of one clock cycle generated when the internal PWM counter (re)starts. The signal trans_enable_out is a pulse synchronous to sync_out, generated if a transfer from system registers to PWM shadow registers occurred when the PWM counter restarted. A delay may be inserted between the counter start and generation of trans_enable_out and sync_out.

A PWM module can use input signals trans_enable_in and sync_in to synchronize its internal PWM counter and the transfer of shadow registers (Slave mode).

6.15.5.4 Pin description

Each of the four PWM modules in the MSCSS has the following pins. These are combined with other functions on the port pins of the LPC2926/2927/2929. Table 24 shows the PWM0 to PWM3 pins.

Table 24. PWM pins

Symbol	Pin name	Direction	Description
PWMn CAP[0]	PCAPn[0]	IN	PWM n capture input 0
PWMn CAP[1]	PCAPn[1]	IN	PWM n capture input 1
PWMn CAP[2]	PCAPn[2]	IN	PWM n capture input 2
PWMn MAT[0]	PMATn[0]	OUT	PWM n match output 0
PWMn MAT[1]	PMATn[1]	OUT	PWM n match output 1
PWMn MAT[2]	PMATn[2]	OUT	PWM n match output 2
PWMn MAT[3]	PMATn[3]	OUT	PWM n match output 3
PWMn MAT[4]	PMATn[4]	OUT	PWM n match output 4
PWMn MAT[5]	PMATn[5]	OUT	PWM n match output 5
PWMn TRAP	TRAPn	IN	PWM n trap input

6.15.5.5 Clock description

The PWM modules are clocked by CLK_MSCSS_PWMx (x = 0 to 3), see Section 6.7.2. Note that each PWM has its own CLK_MSCSS_PWMx branch clock for power management. The frequency of all these clocks is identical to CLK_MSCSS_APB since they are derived from the same base clock BASE_MSCSS_CLK.

Also note that unlike the timer modules in the Peripheral SubSystem, the actual timer counter registers of the PWM modules run at the same clock as the APB system interface CLK_MSCSS_APB. This clock is independent of the AHB system clock.

If a PWM module is not used its CLK_MSCSS_PWMx branch clock can be switched off.

6.15.6 Timers in the MSCSS

The two timers in the MSCSS are functionally identical to the timers in the peripheral subsystem, see Section 6.13.3. The features of the timers in the MSCSS are the same as the timers in the peripheral subsystem, but the capture inputs and match outputs are not available on the device pins. These signals are instead connected to the ADC and PWM modules as outlined in the description of the MSCSS, see Section 6.15.1.

See Section 6.13.3 for a functional description of the timers.

6.16.4.2 Pin description

The RGU module in the LPC2926/2927/2929 has the following pins. Table 31 shows the RGU pins.

Table 31. RGU pins

Symbol	Direction	Description
$\overline{RST}$	IN	external reset input, Active LOW; pulled up internally

6.16.5 Power Management Unit (PMU)

This module enables software to actively control the system's power consumption by disabling clocks not required in a particular operating mode.

Using the base clocks from the CGU as input, the PMU generates branch clocks to the rest of the LPC2926/2927/2929. Output clocks branched from the same base clock are phase- and frequency-related. These branch clocks can be individually controlled by software programming.

The key features are:

- Individual clock control for all LPC2926/2927/2929 sub-modules.
- Activates sleeping clocks when a wake-up event is detected.
- Clocks can be individually disabled by software.
- Supports AHB master-disable protocol when AUTO mode is set.
- Disables wake-up of enabled clocks when Power-down mode is set.
- Activates wake-up of enabled clocks when a wake-up event is received.
- Status register is available to indicate if an input base clock can be safely switched off (i.e. all branch clocks are disabled).

6.16.5.1 Functional description

The PMU controls all internal clocks coming out of the CGU0 for power-mode management. With some exceptions, each branch clock can be switched on or off individually under control of software register bits located in its individual configuration register. Some branch clocks controlling vital parts of the device operate in a fixed mode. Table 32 shows which mode-control bits are supported by each branch clock.

By programming the configuration register the user can control which clocks are switched on or off, and which clocks are switched off when entering Power-down mode.

Note that the standby-wait-for-interrupt instructions of the ARM968E-S processor (putting the ARM CPU into a low-power state) are not supported. Instead putting the ARM CPU into power-down should be controlled by disabling the branch clock for the CPU.

Remark: For any disabled branch clocks to be re-activated their corresponding base clocks must be running (controlled by CGU0).

Table 32 shows the relation between branch and base clocks, see also Section 6.7.1. Every branch clock is related to one particular base clock: it is not possible to switch the source of a branch clock in the PMU.

7. Limiting values

Table 33. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Supply pins						
P_{tot}	total power dissipation		[1]	-	1.5	W
$V_{DD(CORE)}$	core supply voltage			−0.5	+2.0	V
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage			−0.5	+2.0	V
$V_{DDA(ADC3V3)}$	3.3 V ADC analog supply voltage			−0.5	+4.6	V
$V_{DDA(ADC5V0)}$	5.0 V ADC analog supply voltage			−0.5	+6.0	V
$V_{DD(IO)}$	input/output supply voltage			−0.5	+4.6	V
I_{DD}	supply current	average value per supply pin	[2]	-	98	mA
I_{SS}	ground current	average value per ground pin	[2]	-	98	mA
Input pins and I/O pins						
V_{XIN_OSC}	voltage on pin XIN_OSC			−0.5	+2.0	V
$V_{I(IO)}$	I/O input voltage		[3][4][5]	−0.5	$V_{DD(IO)}$ + 3.0	V
$V_{I(ADC)}$	ADC input voltage	for ADC1/2: I/O port 0 pin 8 to pin 23.	[4][5]	−0.5	$V_{DDA(ADC3V3)}$ + 0.5	V
		for ADC0: I/O port 0 pin 5 to pin 7; I/O port 2 pins 12 and 13; I/O port 3 pins 0 and 1.	[4][5][6][7]	−0.5	$V_{DDA(ADC5V0)}$ + 0.5	V
V_{VREFP}	voltage on pin VREFP			−0.5	+3.6	V
V_{VREFN}	voltage on pin VREFN			−0.5	+3.6	V
$I_{I(ADC)}$	ADC input current	average value per input pin	[2]	-	35	mA
Output pins and I/O pins configured as output						
I_{OHS}	HIGH-level short-circuit output current	drive HIGH, output shorted to $V_{SS(IO)}$	[8]	-	−33	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW, output shorted to $V_{DD(IO)}$	[8]	-	+38	mA
General						
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

Table 33. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
ESD						
V_{ESD}	electrostatic discharge voltage	on all pins				
		human body model	[9]	−2000	+2000	V
		charged device model		−500	+500	V
		on corner pins				
		charged device model		−750	+750	V

[1] Based on package heat transfer, not device power consumption.

[2] Peak current must be limited at 25 times average current.

[3] For I/O Port 0, the maximum input voltage is defined by $V_{I(ADC)}$.

[4] Only when $V_{DD(IO)}$ is present.

[5] Note that pull-up should be off. With pull-up do not exceed 3.6 V.

[6] For these input pins a fixed amplification of $^{2}/_{3}$ is performed on the input voltage before feeding into the ADC0 itself. The maximum input voltage on ADC0 is $V_{DDA(ADC5V0)}$.

[7] Not exceeding 6 V.

[8] 112 mA per $V_{DD(IO)}$ or $V_{SS(IO)}$ should not be exceeded.

[9] Human-body model: discharging a 100 pF capacitor via a 10 kΩ series resistor.

9.6 Dynamic characteristics: external static memory

Table 42. External static memory interface dynamic characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{CLCL}	clock cycle time		8	-	100	ns
$t_{a(R)int}$	internal read access time		-	-	20.5	ns
$t_{a(W)int}$	internal write access time		-	-	24.9	ns
Read cycle parameters						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		–5	–2.5	-	ns
t_{OELAV}	$\overline{OE}$ LOW to address valid time		–5 – WSTOEN × T_{CLCL}	–2.5 – WSTOEN × T_{CLCL}	-	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		-	0 + WSTOEN × T_{CLCL}	-	ns
$t_{su(DQ)}$	data input/output set-up time		11	16	22	ns
$t_{h(D)}$	data input hold time		0	2.5	5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		-	0	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time		-	(WST1 – WSTOEN + 1) × T_{CLCL}	-	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		-	(WST1 – WSTOEN + 1) × T_{CLCL}	-	ns
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		-	0 + WSTOEN × T_{CLCL}	-	ns
Write cycle parameters						
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	[2]	-	0	-	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		-	(WSTWEN + 0.5) × T_{CLCL}	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[3]	-	WSTWEN × T_{CLCL}	-	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time		-	(WSTWEN + 0.5) × T_{CLCL}	-	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		–0.5	–0.1	0.3	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time		-	(WST2 – WSTWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4]	-	(WST2 – WSTWEN + 2) × T_{CLCL}	-	ns

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] When the byte lane select signals are used to connect the write enable input (8 bit devices), $t_{CSHBLSH} = -0.5 \times T_{CLCL}$.

[3] When the byte lane select signals are used to connect the write enable input (8 bit devices), $t_{CSLBLSL} = t_{CSLWEL}$.

[4] For 16 and 32 bit devices.

9.7 Dynamic characteristics: ADC

Table 43. ADC dynamic characteristics

$V_{DD(CORE)}$ = $V_{DD(OSC\_PLL)}$; $V_{DD(IO)}$ = 2.7 V to 3.6 V; $V_{DDA(ADC3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
5.0 V ADC0							
$f_{i(ADC)}$	ADC input frequency		[2]	4	-	4.5	MHz
$f_{s(max)}$	maximum sampling rate	$f_{i(ADC)}$ = 4.5 MHz; $f_s = f_{i(ADC)} / (n + 1)$ with n = resolution					
		resolution 2 bit		-	-	1500	ksample/s
		resolution 10 bit		-	-	400	ksample/s
t_{conv}	conversion time	In number of ADC clock cycles		3	-	11	cycles
		In number of bits		2	-	10	bits
3.3 V ADC1/2							
$f_{i(ADC)}$	ADC input frequency		[2]	4	-	4.5	MHz
$f_{s(max)}$	maximum sampling rate	$f_{i(ADC)}$ = 4.5 MHz; $f_s = f_{i(ADC)} / (n + 1)$ with n = resolution					
		resolution 2 bit		-	-	1500	ksample/s
		resolution 10 bit		-	-	400	ksample/s
t_{conv}	conversion time	In number of ADC clock cycles		3	-	11	cycles
		In number of bits		2	-	10	bits

[1] All parameters are guaranteed over the virtual junction temperature range by design. Pre-testing is performed at T_{amb} = 85 °C ambient temperature on wafer level. Cased products are tested at T_{amb} = 25 °C (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Duty cycle clock should be as close as possible to 50 %.

10. Application information

10.1 Operating frequency selection

The LPC2926/2927/2929 is specified to operate at a maximum frequency of 125 MHz, maximum temperature of 85 °C, and maximum core voltage of 1.89 V. Figure 30 and Figure 31 show that the user can achieve higher operating frequencies for the LPC2926/2927/2929 by controlling the temperature and the core voltage accordingly.

10.3 SPI signal forms

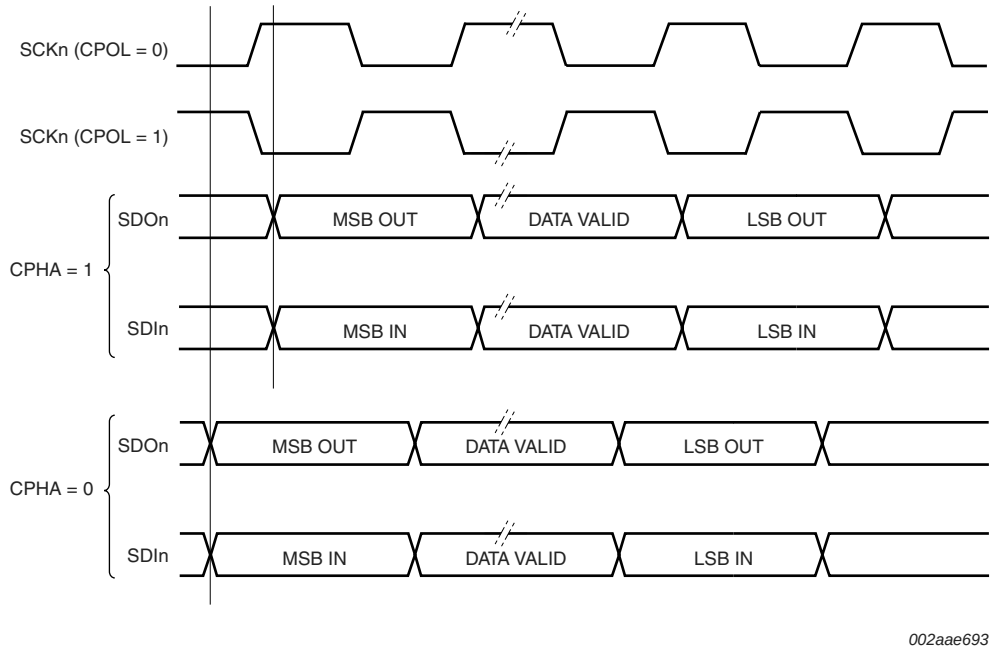


Fig 36. SPI timing in master mode

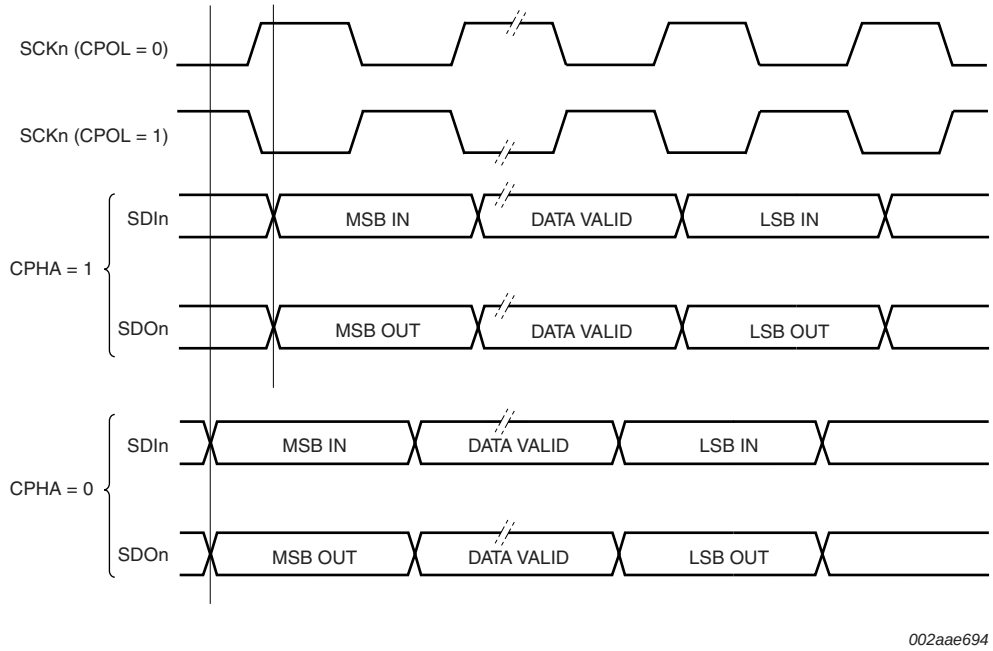
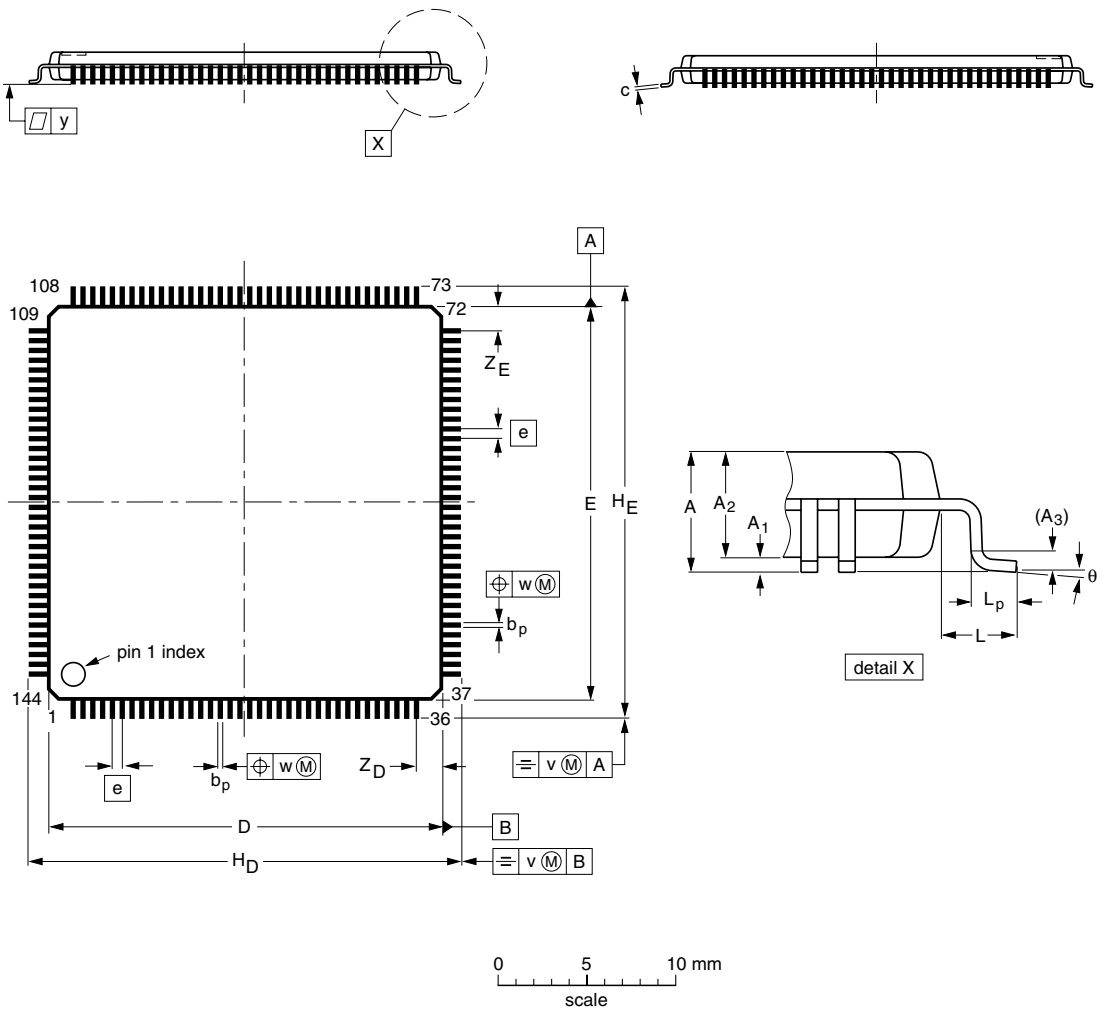


Fig 37. SPI timing in slave mode

11. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

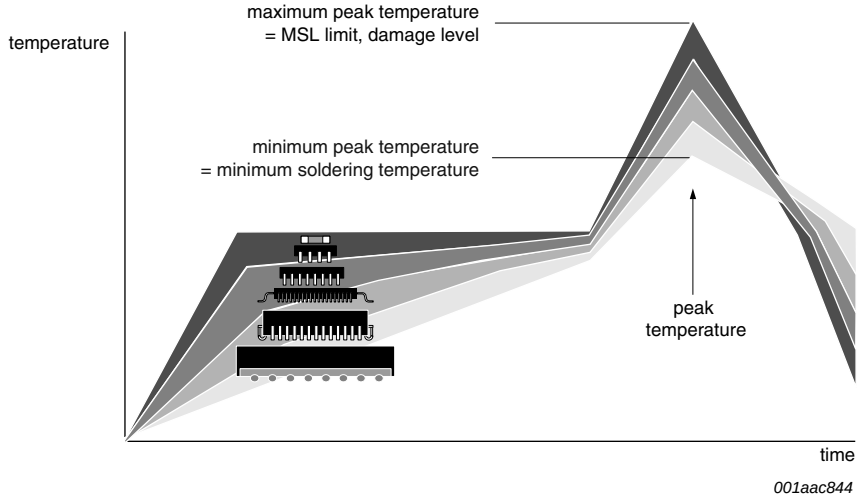
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 39. Package outline SOT486-1 (LQFP144)



MSL: Moisture Sensitivity Level

Fig 40. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.