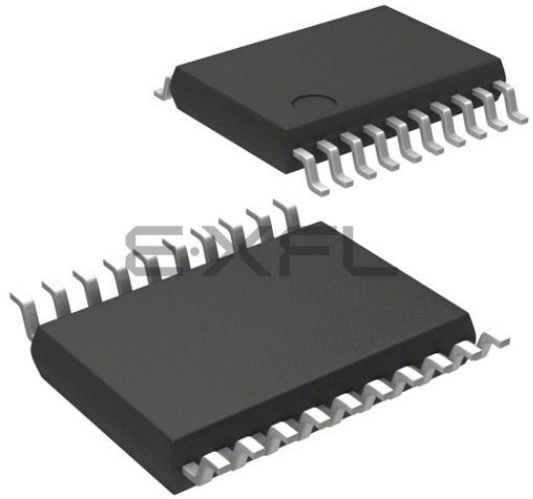

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s003f3p6

Contents

List of tables

2 Description

The STM8S003F3/K3 value line 8-bit microcontrollers offer 8 Kbytes of Flash program memory, plus integrated true data EEPROM. They are referred to as low-density devices in the STM8S microcontroller family reference manual (RM0016).

TheSTM8S003F3/K3 value line devices provide the following benefits: performance, robustness and reduced system cost.

Device performance and robustness are ensured by true data EEPROM supporting up to 100000 write/erase cycles, advanced core and peripherals made in a state-of-the-art technology at 16 MHz clock frequency, robust I/Os, independent watchdogs with separate clock source, and a clock security system.

The system cost is reduced thanks to a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Full documentation is offered as well as a wide choice of development tools.

Table 1. STM8S003F3/K3 value line features

Features	STM8S003K3	STM8S003F3
Pin count	32	20
Max. number of GPIOs (I/O)	28	16
External interrupt pins	27	16
Timer CAPCOM channels	7	7
Timer complementary outputs	3	2
A/D converter channels	4	5
High-sink I/Os	21	12
Low-density Flash program memory (byte)	8 K	8 K
RAM (byte)	1 K	1 K
True data EEPROM (byte)	128(1)	128(1)
Peripheral set	Multi purpose timer (TIM1), SPI, I2C, UART, Window WDG, independent WDG, ADC, PWM timer (TIM2), 8-bit timer (TIM4)	

1. Without read-while-write capability.

4 Product overview

The following section intends to give an overview of the basic features of the STM8S003F3/K3 value line functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains six internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler***: To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching***: Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management***: To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources***: Four different clock sources can be used to drive the master clock:
  - 1-16 MHz high-speed external crystal (HSE)
  - Up to 16 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock***: After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)***: This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)***: This outputs an external clock for use by the application.

Table 2. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART1	PCKEN27	Reserved	PCKEN23	ADC
PCKEN16	Reserved	PCKEN12	Reserved	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 3. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC1)

STM8S003F3/K3 value line products contain a 10-bit successive approximation A/D converter (ADC1) with up to 5 external multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Conversion time: 14 clock cycles
- Single and continuous, buffered continuous conversion modes
- Buffer size (10 x 10 bits)
- Scan mode for single and continuous conversion of a sequence of channels
- Analog watchdog capability with programmable upper and lower thresholds
- Analog watchdog interrupt
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

Note: Additional AIN12 analog input is not selectable in ADC scan mode or with analog watchdog. Values converted from AIN12 are stored only into the ADC_DRH/ADC_DRL registers.

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: full feature UART, synchronous mode, SPI master mode, SmartCard mode, IrDA mode, LIN2.1 master capability
- SPI: full and half-duplex, 8 Mbit/s
- I²C: up to 400 Kbit/s

Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
7	PA3/TIM2_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 2 channel 3	SPI master/ slave select [AFR1]
8	PF4	I/O	**X**	X	-	-	O1	X	X	**Port F4**	-	-
9	PB7	I/O	**X**	X	-	-	O1	X	X	**Port B7**	-	-
10	PB6	I/O	**X**	X	-	-	O1	X	X	**Port B6**	-	-
11	PB5/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port B5**	I^2C data	-
12	PB4/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port B4**	I^2C clock	-
13	PB3/AIN3 [TIM1_ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port B3**	Analog input 3/Timer 1 external trigger	-
14	PB2/AIN2 [TIM1_CH3N]	I/O	**X**	X	X	HS	O3	X	X	**Port B2**	Analog input 2/Timer 1 - inverted channel 3	-
15	PB1/AIN1 [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	**Port B1**	Analog input 1/Timer 1 - inverted channel 2	-
16	PB0/AIN0 [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	**Port B0**	Analog input 0/Timer 1 - inverted channel 1	-
17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	**Port E5**	SPI master/slave select	-
18	PC1/TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1 UART1 clock	-
19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-

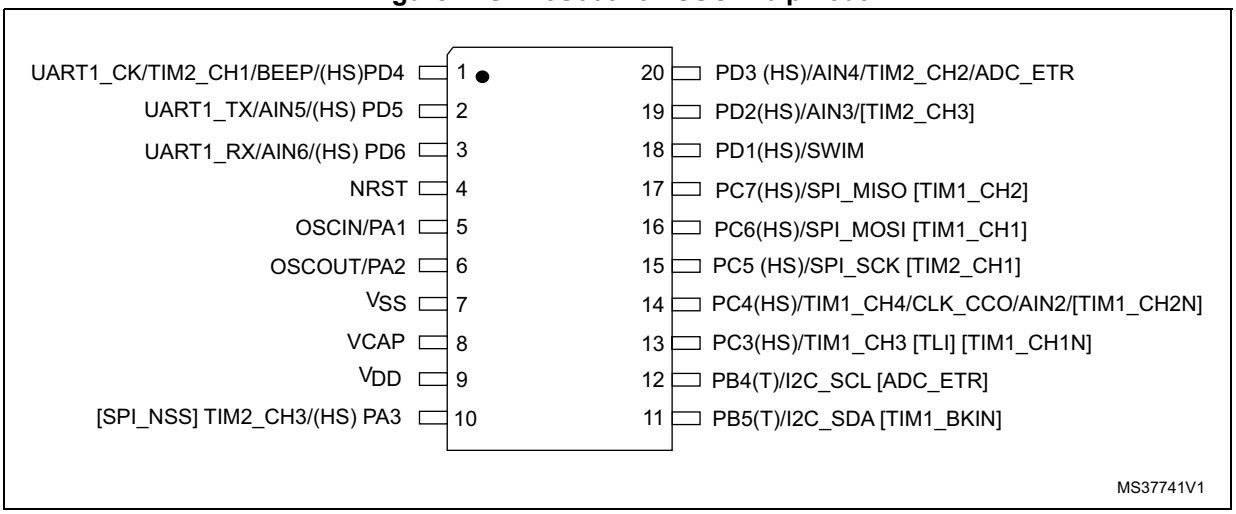
Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
21	PC4/TIM1_CH4/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4/configurable clock output	-
22	PC5/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	-
23	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/slave in	-
24	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	-
25	PD0/[TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 1 - break input	Configurable clock output [AFR5]
26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
27	PD2 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	-	Timer 2 - channel 3 [AFR1]
28	PD3/TIM2_CH2 [ADC_ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2/ADC external trigger	-
29	PD4/BEEP/ TIM2_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1/BEEP output	-
30	PD5/ UART1_TX	I/O	**X**	X	X	HS	O3	X	X	**Port D5**	UART1 data transmit	-
31	PD6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	**Port D6**	UART1 data receive	-
32	PD7/TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	**Port D7**	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high-current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings given in *Section 9: Electrical characteristics*.
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.

5.2 STM8S003F3 TSSOP20/UFQFPN20 pinout and pin description

Figure 4. STM8S003F3 TSSOP20 pinout



1. HS high sink capability.
2. (T) True open drain (P-buffer and protection diode to VDD not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6. STM8S003F3 pin description (continued)

Pin no.		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
TSSOP20	UFQFPN20			floating	wpu	Ext. interr.	High sink(1)	Speed	OD	PP			
14	11	PC4/ CLK_CCO/ TIM1_ CH4/AIN2/ [TIM1_ CH2N]	I/O	**X**	X	X	HS	O3	X	X	Port C4	Configurable clock output/Timer 1 - channel 4/Analog input 2	Timer 1 - inverted channel 2 [AFR7]
15	12	PC5/ SPI_SCK [TIM2_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C5	SPI clock	Timer 2 - channel 1 [AFR0]
16	13	PC6/ SPI_MOSI [TIM1_ CH1]	I/O	**X**	X	X	HS	O3	X	X	Port C6	SPI master out/slave in	Timer 1 - channel 1 [AFR0]
17	14	PC7/ SPI_MISO [TIM1_ CH2]	I/O	**X**	X	X	HS	O3	X	X	Port C7	SPI master in/ slave out	Timer 1 - channel 2 [AFR0]
18	15	PD1/ SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	Port D1	SWIM data interface	-
19	16	PD2/AIN3/ [TIM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	Port D2	Analog input 3	Timer 2 - channel 3 [AFR1]
20	17	PD3/ AIN4/ TIM2_ CH2/ ADC_ ETR	I/O	**X**	X	X	HS	O3	X	X	Port D3	Analog input 4/ Timer 2 - channel 2/ADC external trigger	-

1. I/O pins used simultaneously for high current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings.
2. When the MCU is in halt/active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended d to use PA1 only in input mode if halt/active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to VDD are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after internal reset release.

Table 17. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(3)(4)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
$\Sigma I_{INJ(PIN)}$(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

Total current consumption in halt mode

Table 27. Total current consumption in halt mode at V_{DD} = 5 V

Symbol	Parameter	Conditions	Typ	Max at 85°C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	63	75	µA
		Flash in power-down mode, HSI clock after wakeup	6.0	20	

1. Data based on characterization results, not tested in production.

Table 28. Total current consumption in halt mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max at 85° C(1)	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash in operating mode, HSI clock after wakeup	60	75	µA
		Flash in power-down mode, HSI clock after wakeup	4.5	17	

1. Data based on characterization results, not tested in production.

Low-power mode wakeup times

Table 29. Wakeup times

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$t_{WU(WFI)}$	Wakeup time from wait mode to run mode(3)	0 to 16 MHz			-	-(2)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz.			0.56	-	
$t_{WU(AH)}$	Wakeup time active halt mode to run mode.(3)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wakeup)	1(6)	2(6)	
			Flash in power-down mode(5)		3(6)	-	
		MVR voltage regulator off(4)	Flash in operating mode(5)		48(6)	-	
			Flash in power-down mode(5)		50(6)	-	
$t_{WU(H)}$	Wakeup time from halt mode to run mode(3)	Flash in operating mode(5)			52	-	
		Flash in power-down mode(5)			54	-	

1. Data guaranteed by design, not tested in production.
2. $t_{WU(WFI)} = 2 \times 1/f_{master} + 7 \times 1/f_{CPU}$
3. Measured from interrupt event to interrupt vector fetch.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization.

9.3.3 External clock sources and timing characteristics

HSE user external clock

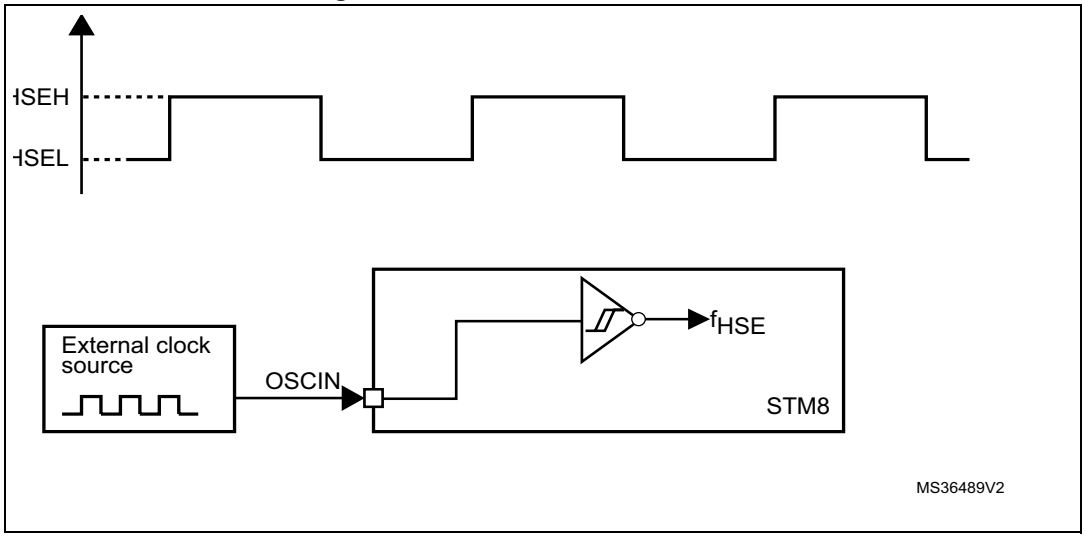
Subject to general operating conditions for V_{DD} and T_A.

Table 32. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	0	-	16	MHz
V_{HSEH}(1)	OSCIN input pin high level voltage		0.7 x V_{DD}	-	V_{DD} + 0.3 V	V
V_{HSEL}(1)	OSCIN input pin low level voltage		V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. Data based on characterization results, not tested in production.

Figure 17. HSE external clock source



HSE crystal/ceramic resonator oscillator

The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 41. Output driving current (high sink ports)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level with 8 pins sunk	I_{IO} = 10 mA, V_{DD} = 5 V	-	0.8	V
	Output low level with 4 pins sunk	I_{IO} = 10 mA, V_{DD} = 3.3 V	-	1.0(1)	
	Output low level with 4 pins sunk	I_{IO} = 20 mA, V_{DD} = 5 V	-	1.5(1)	
V_{OH}	Output high level with 8 pins sourced	I_{IO} = 10 mA, V_{DD} = 5 V	4.0	-	
	Output high level with 4 pins sourced	I_{IO} = 10 mA, V_{DD} = 3.3 V	2.1(1)	-	
	Output high level with 4 pins sourced	I_{IO} = 20 mA, V_{DD} = 5 V	3.3(1)	-	

1. Data based on characterization results, not tested in production

Typical output level curves

Figure 25 to *Figure 32* show typical output level curves measured with output on a single pin.

Figure 24. Typ. V_{OL} @ V_{DD} = 5 V (standard ports)

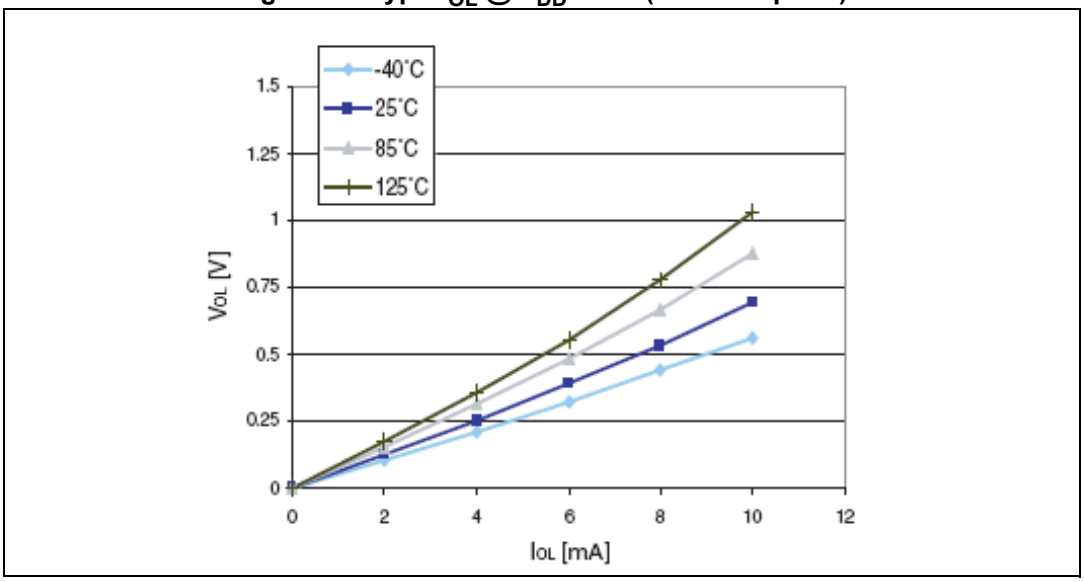


Figure 29. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

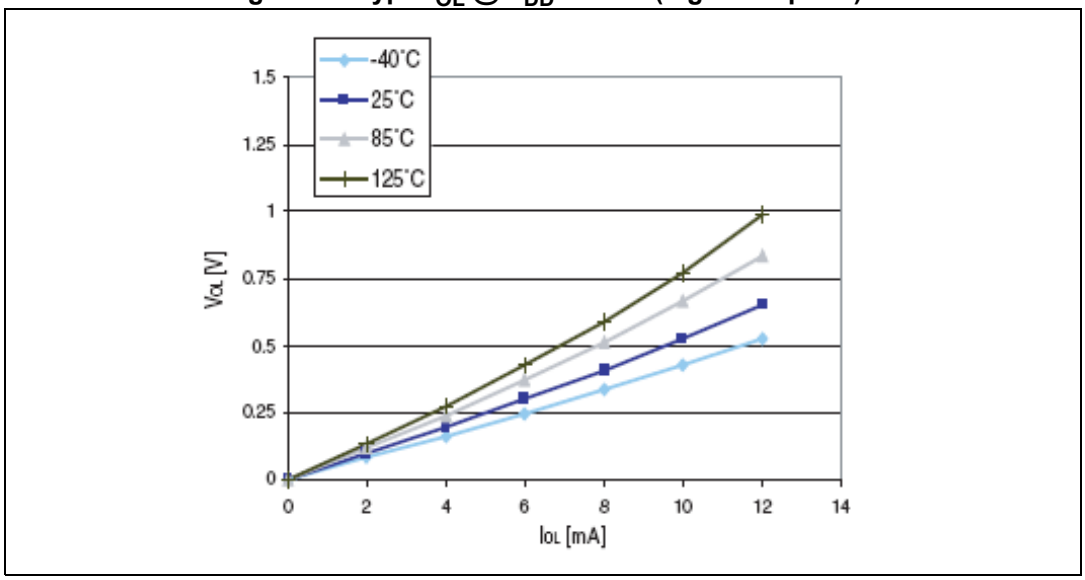


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports)

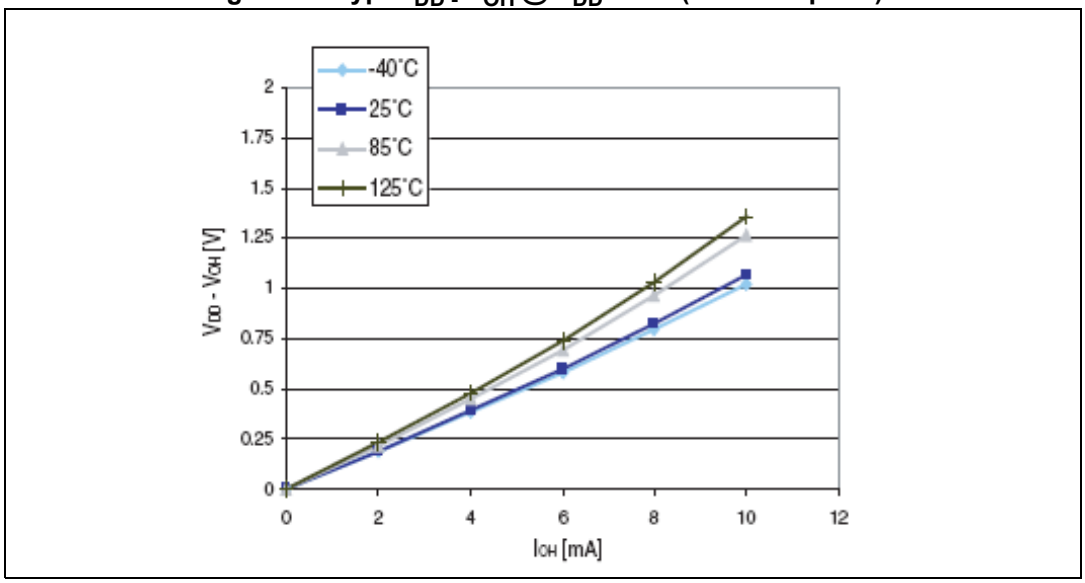


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

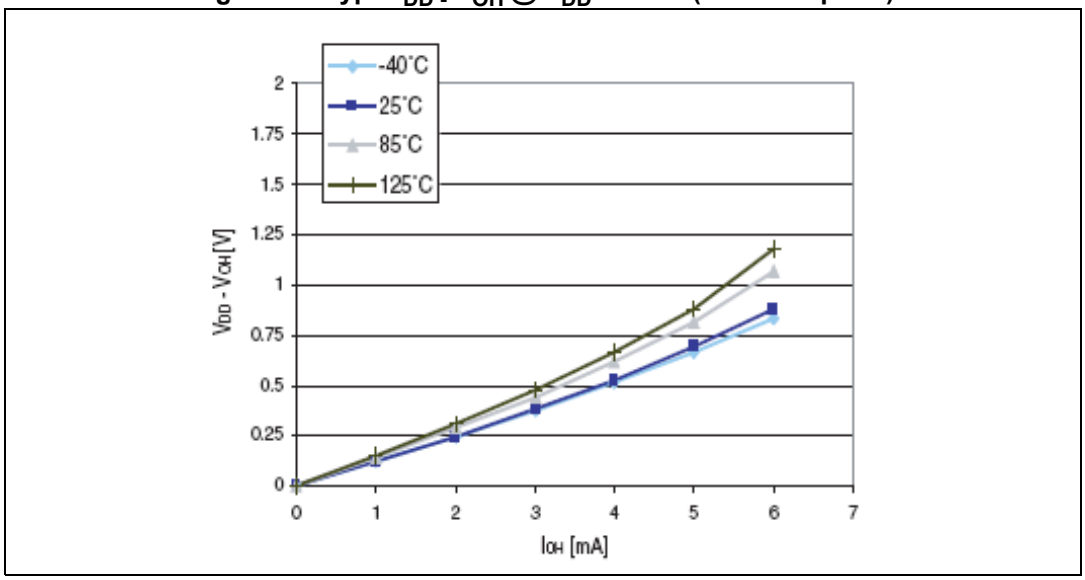


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports)

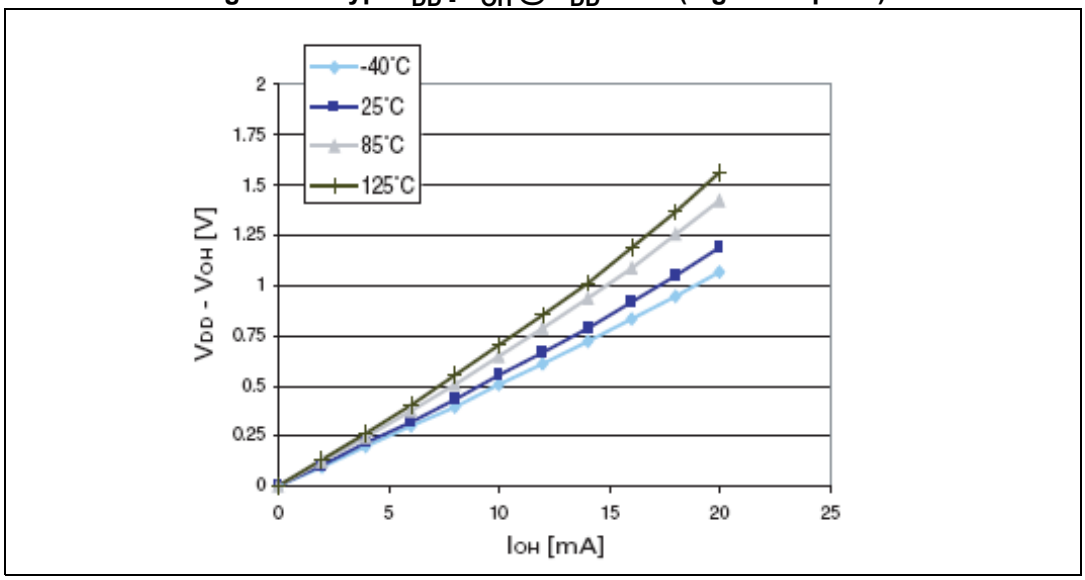
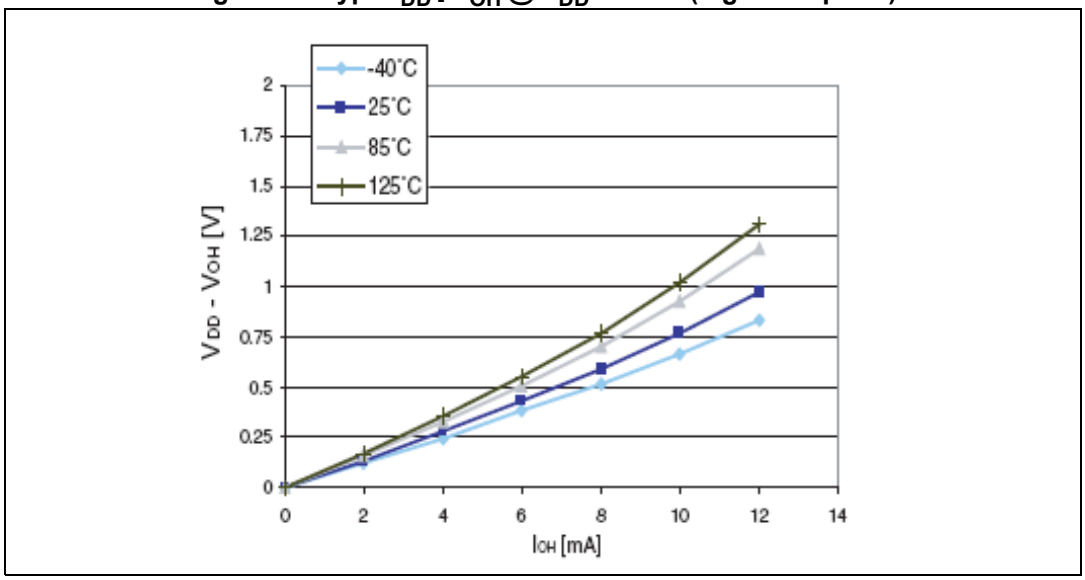


Figure 33. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)



1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Table 47. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\lvert E_T \rvert$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.6	3.5	LSB
		f_{ADC} = 4 MHz	1.9	4	
$\lvert E_O \rvert$	Offset error(2)	f_{ADC} = 2 MHz	1	2.5	
		f_{ADC} = 4 MHz	1.5	2.5	
$\lvert E_G \rvert$	Gain error(2)	f_{ADC} = 2 MHz	1.3	3	
		f_{ADC} = 4 MHz	2	3	
$\lvert E_D \rvert$	Differential linearity error(2)	f_{ADC} = 2 MHz	0.7	1.0	
		f_{ADC} = 4 MHz	0.7	1.5	
$\lvert E_L \rvert$	Integral linearity error(2)	f_{ADC} = 2 MHz	0.6	1.5	
		f_{ADC} = 4 MHz	0.8	2	

1. Data based on characterization results, not tested in production.
2. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 9.3.6* does not affect the ADC accuracy.

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) is performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 51. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

13 Revision history

Table 56. Document revision history

Date	Revision	Changes
12-Jul-2011	1	Initial release.
09-Jan-2012	2	Added N_{RW} and t_{RET} for data EEPROM in *Table: Flash program memory and data EEPROM*. Updated R_{PU} in *Table: NRST pin characteristics* and *Table: I/O static characteristics*. Updated notes related to V_{CAP} in *Table: General operating conditions*.
12-Jun-2012	3	Updated temperature condition for factory calibrated ACC_{HSI} in *Table: HSI oscillator characteristics.* Changed SCK input to SCK output in *Figure: SPI timing diagram - master mode.* Modified *Figure: 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)* to add the package top view.
18-Dec-2014	4	Updated the package information for the 20-pin TSSOP and the 20-pin UFQFPN.
21-Apr-2015	5	Added package marking examples in *Section: Package information*: – *Figure: LQFP32 marking example (package top view)*, – *Figure: TSSOP20 marking example (package top view),* – *Figure: UFQFPN20 marking example (package top view).*
26-Jun-2015	6	Addition of the footnotes about D and E1 dimensions to *Table 53: TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data*. Update of the standard for EMI characteristics in *Section : Electromagnetic interference (EMI)*.
23-Sep-2015	7	Correction of UART peripheral in *Figure 1: STM8S003F3/K3 value line block diagram*.
20-Apr-2016	8	Corrected text strings in *Figure 10: External capacitor CEXT* and *Figure 37: Recommended reset pin protection* PB4 line PP column value corrected in *Table 5: STM8S003K3 descriptions* PD1 line “floating” and “wpu” column values corrected in *Table 6: STM8S003F3 pin description* SPI_RXCRCR and SPI_TXCRCR reset values corrected in *Table 9: General hardware register map*