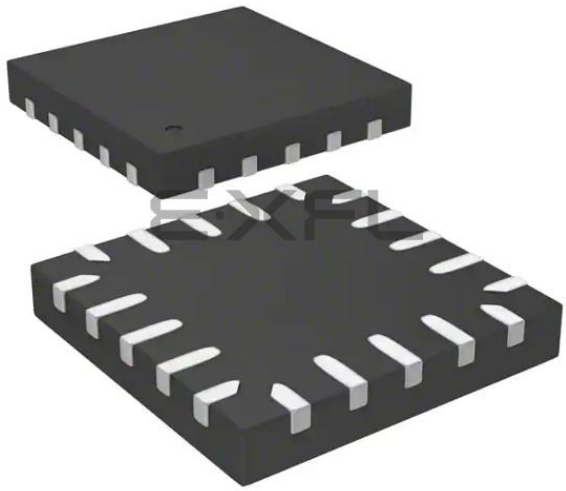

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.95V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8s003f3u6tr

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4.14.1 UART1

Main features

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: generates 13-bit synch. break frame
- Reception: detects 11-bit break frame

4.14.2 SPI

- Maximum speed: 8 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

5 Pinouts and pin descriptions

Table 4. Legend/abbreviations for STM8S003F3/K3 pin description tables

Type	I = input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = high sink
Output speed	O1 = slow (up to 2 MHz) O2 = fast (up to 10 MHz) O3 = fast/slow programmability with slow as default state after reset O4 = fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold **x** (pin state after internal reset release) Unless otherwise specified, the pin state is the same during the reset phase and after the internal reset release.	

Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/ crystal out	-
4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		-
5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		-
6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		-
7	PA3/TIM2_CH3 [SPI_NSS]	I/O	**X**	X	X	HS	O3	X	X	**Port A3**	Timer 2 channel 3	SPI master/ slave select [AFR1]
8	PF4	I/O	**X**	X	-	-	O1	X	X	**Port F4**	-	-
9	PB7	I/O	**X**	X	-	-	O1	X	X	**Port B7**	-	-
10	PB6	I/O	**X**	X	-	-	O1	X	X	**Port B6**	-	-
11	PB5/I^2C_SDA	I/O	**X**	-	X	-	O1	T(3)	-	**Port B5**	I^2C data	-
12	PB4/I^2C_SCL	I/O	**X**	-	X	-	O1	T(3)	-	**Port B4**	I^2C clock	-
13	PB3/AIN3 [TIM1_ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port B3**	Analog input 3/Timer 1 external trigger	-
14	PB2/AIN2 [TIM1_CH3N]	I/O	**X**	X	X	HS	O3	X	X	**Port B2**	Analog input 2/Timer 1 - inverted channel 3	-
15	PB1/AIN1 [TIM1_CH2N]	I/O	**X**	X	X	HS	O3	X	X	**Port B1**	Analog input 1/Timer 1 - inverted channel 2	-
16	PB0/AIN0 [TIM1_CH1N]	I/O	**X**	X	X	HS	O3	X	X	**Port B0**	Analog input 0/Timer 1 - inverted channel 1	-
17	PE5/SPI_NSS	I/O	**X**	X	X	HS	O3	X	X	**Port E5**	SPI master/slave select	-
18	PC1/TIM1_CH1/ UART1_CK	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1 UART1 clock	-
19	PC2/TIM1_CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	-
20	PC3/TIM1_CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	-

Table 5. STM8S003K3 descriptions (continued)

LQFP32	Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
			floating	wpu	Ext. interrupt	High sink(1)	Speed	OD	PP			
21	PC4/TIM1_CH4/CLK_CCO	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4/configurable clock output	-
22	PC5/SPI_SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	-
23	PC6/SPI_MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/slave in	-
24	PC7/SPI_MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	-
25	PD0/[TIM1_BKIN [CLK_CCO]	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 1 - break input	Configurable clock output [AFR5]
26	PD1/SWIM(4)	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	-
27	PD2 [TIM2_CH3]	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	-	Timer 2 - channel 3 [AFR1]
28	PD3/TIM2_CH2 [ADC_ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2/ADC external trigger	-
29	PD4/BEEP/ TIM2_CH1	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1/BEEP output	-
30	PD5/ UART1_TX	I/O	**X**	X	X	HS	O3	X	X	**Port D5**	UART1 data transmit	-
31	PD6/ UART1_RX	I/O	**X**	X	X	HS	O3	X	X	**Port D6**	UART1 data receive	-
32	PD7/TLI [TIM1_CH4]	I/O	**X**	X	X	HS	O3	X	X	**Port D7**	Top level interrupt	Timer 1 - channel 4 [AFR6]

1. I/O pins used simultaneously for high-current source/sink must be uniformly spaced around the package. In addition, the total driven current must respect the absolute maximum ratings given in *Section 9: Electrical characteristics*.
2. When the MCU is in Halt/Active-halt mode, PA1 is automatically configured in input weak pull-up and cannot be used for waking up the device. In this mode, the output state of PA1 is not driven. It is recommended to use PA1 only in input mode if Halt/Active-halt is used in the application.
3. In the open-drain output column, "T" defines a true open-drain I/O (P-buffer, weak pull-up, and protection diode to V_{DD} are not implemented).
4. The PD1 pin is in input pull-up during the reset phase and after the internal reset release.

6 Memory and register map

6.1 Memory map

Figure 6. Memory map

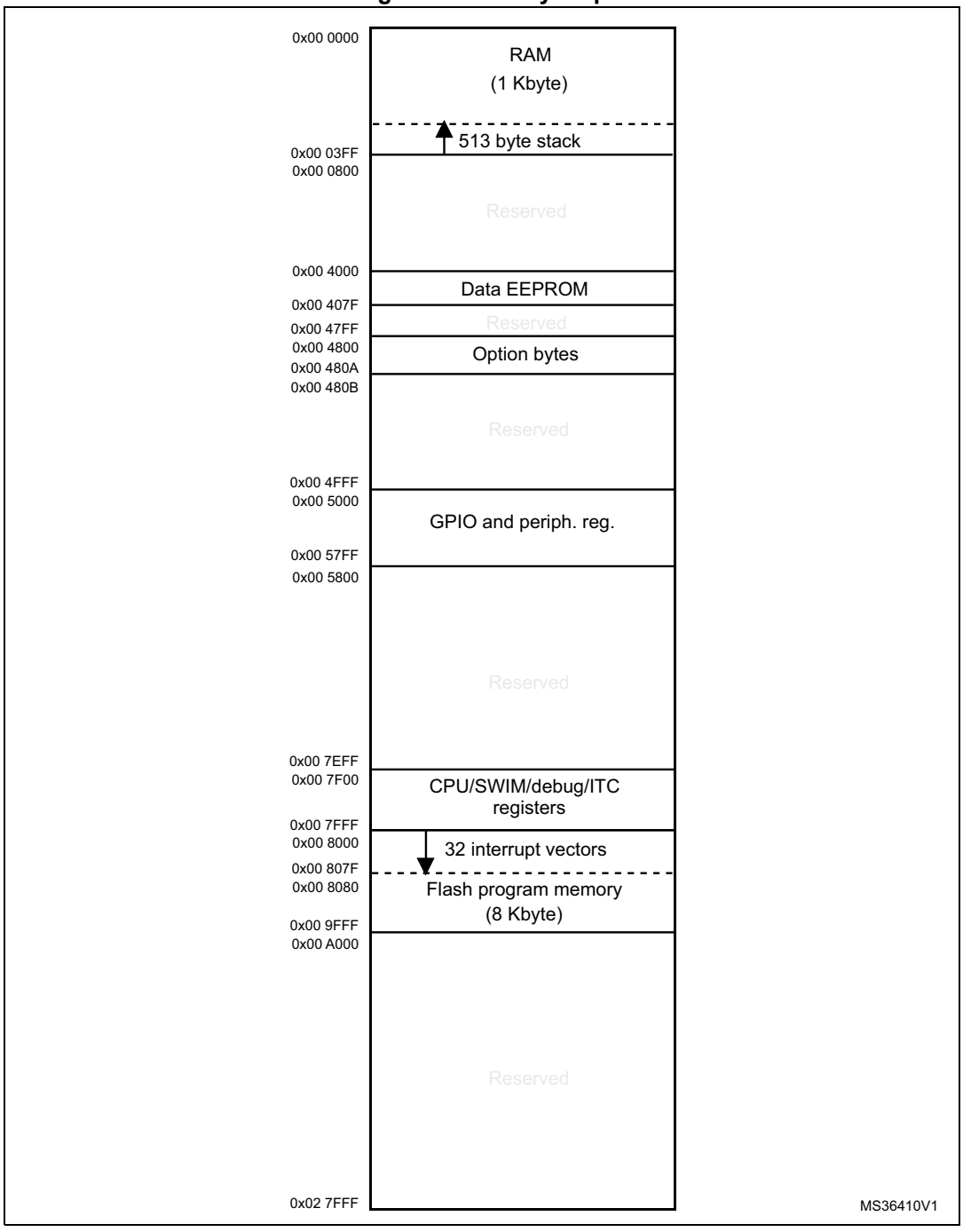


Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5216	I²C	I2C_DR	I²C data register	0x00
0x00 5217		I2C_SR1	I²C status register 1	0x00
0x00 5218		I2C_SR2	I²C status register 2	0x00
0x00 5219		I2C_SR3	I²C status register 3	0x00
0x00 521A		I2C_ITR	I²C interrupt control register	0x00
0x00 521B		I2C_CCRL	I²C clock control register low	0x00
0x00 521C		I2C_CCRH	I²C clock control register high	0x00
0x00 521D		I2C_TRISER	I²C TRISE register	0x02
0x00 521E		I2C_PECR	I²C packet error checking register	0x00
0x00 521F to 0x00 522F	Reserved area (17 byte)			
0x00 5230	UART1	UART1_SR	UART1 status register	0xC0
0x00 5231		UART1_DR	UART1 data register	0xXX
0x00 5232		UART1_BRR1	UART1 baud rate register 1	0x00
0x00 5233		UART1_BRR2	UART1 baud rate register 2	0x00
0x00 5234		UART1_CR1	UART1 control register 1	0x00
0x00 5235		UART1_CR2	UART1 control register 2	0x00
0x00 5236		UART1_CR3	UART1 control register 3	0x00
0x00 5237		UART1_CR4	UART1 control register 4	0x00
0x00 5238		UART1_CR5	UART1 control register 5	0x00
0x00 5239		UART1_GTR	UART1 guard time register	0x00
0x00 523A		UART1_PSCR	UART1 prescaler register	0x00
0x00 523B to 0x00523F	Reserved area (21 byte)			

Table 9. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5300	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5301		Reserved		
0x00 5302		Reserved		
0x00 5303		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5304		TIM2_SR1	TIM2 status register 1	0x00
0x00 5305		TIM2_SR2	TIM2 status register 2	0x00
0x00 5306		TIM2_EGR	TIM2 event generation register	0x00
0x00 5307		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5308		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 5309		TIM2_CCMR3	TIM2 capture/compare mode register 3	0x00
0x00 530A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 530B		TIM2_CCER2	TIM2 capture/compare enable register 2	0x00
0x00 530C		TIM2_CNTRH	TIM2 counter high	0x00
0x00 530D		TIM2_CNTRL	TIM2 counter low	0x00
0x00 530E		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 530F		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 5310		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5311		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5312		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5313		TIM2_CCR2H	TIM2 capture/compare reg. 2 high	0x00
0x00 5314		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5315		TIM2_CCR3H	TIM2 capture/compare register 3 high	0x00
0x00 5316		TIM2_CCR3L	TIM2 capture/compare register 3 low	0x00
0x00 5317 to 0x00 533F	Reserved area (43 byte)			
0x00 5340	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 5341		Reserved		
0x00 5342		Reserved		
0x00 5343		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 5344		TIM4_SR	TIM4 status register	0x00
0x00 5345		TIM4_EGR	TIM4 event generation register	0x00
0x00 5346		TIM4_CNTR	TIM4 counter	0x00
0x00 5347		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 5348		TIM4_ARR	TIM4 auto-reload register	0xFF

8.1 Alternate function remapping bits

Table 14. STM8S003K3 alternate function remapping bits for 32-pin devices

Option byte number	Description[1]
OPT2	**AFR7***Alternate function remapping option 7* Reserved. **AFR6** *Alternate function remapping option 6* 0: AFR6 remapping option inactive: default alternate function[2] 1: Port D7 alternate function = TIM1_CH4. **AFR5** *Alternate function remapping option 5* 0: AFR5 remapping option inactive: default alternate function[2] 1: Port D0 alternate function = CLK_CCO. **AFR[4:2]** *Alternate function remapping option 4:2* Reserved. **AFR1** *Alternate function remapping option 1* 0: AFR1 remapping option inactive: default alternate function[2] 1: Port A3 alternate function = SPI_NSS; port D2 alternate function TIM2_CH3 **AFR0** *Alternate function remapping option 0* Reserved.

1. Do not use more than one remapping option in the same port. It is forbidden to enable both AFR1 and AFR0
2. Refer to the pinout description.

Table 17. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(3)(4)	Injected current on NRST pin	±4	
	Injected current on OSCIN pin	±4	
	Injected current on any other pin(5)	±4	
$\Sigma I_{INJ(PIN)}$(3)	Total injected current (sum of all I/O and control pins)(5)	±20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. ADC accuracy vs. negative injection current: Injecting negative current on any of the analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

Table 22. Total current consumption with code execution in run mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode, code executed from RAM	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	1.8	-	mA
			HSE user ext. clock (16 MHz)	2	2.3	
			HSI RC osc. (16 MHz)	1.5	2	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSE user ext. clock (16 MHz)	0.81	-	
			HSI RC osc. (16 MHz)	0.7	0.87	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.41	0.55	
	Supply current in run mode, code executed from Flash	$f_{CPU} = f_{MASTER}$ = 16 MHz	HSE crystal osc. (16 MHz)	4	-	
			HSE user ext. clock (16 MHz)	3.9	4.7	
			HSI RC osc. (16 MHz)	3.7	4.5	
		$f_{CPU} = f_{MASTER}$ = 2 MHz	HSI RC osc. (16 MHz/8)(2)	0.84	1.05	
		$f_{CPU} = f_{MASTER}/128$ = 125 kHz	HSI RC osc. (16 MHz)	0.72	0.9	
		$f_{CPU} = f_{MASTER}/128$ = 15.625 kHz	HSI RC osc. (16 MHz/8)	0.46	0.58	
		$f_{CPU} = f_{MASTER}$ = 128 kHz	LSI RC osc. (128 kHz)	0.42	0.57	

1. Data based on characterization results, not tested in production.
2. Default clock configuration, measured with all peripherals off.

Total current consumption and timing in forced reset state

Table 30. Total current consumption and timing in forced reset state

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$I_{DD(R)}$	Supply current in reset state (2)	V_{DD} = 5 V	400	-	µA
		V_{DD} = 3.3 V	300	-	
$t_{RESETBL}$	Reset pin release to vector fetch	-	-	150	µs

1. Data guaranteed by design, not tested in production.
2. Characterized with all I/Os tied to V_{SS}.

Current consumption of on-chip peripherals

Subject to general operating conditions for V_{DD} and T_A.

HSI internal RC/f_{CPU} = f_{MASTER} = 16 MHz, VDD = 5 V.

Table 31. Peripheral current consumption

Symbol	Parameter	Typ.	Unit
$I_{DD(TIM1)}$	TIM1 supply current (1)	210	µA
$I_{DD(TIM2)}$	TIM2 supply current (1)	130	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)	50	
$I_{DD(UART1)}$	UART1 supply current(1)	120	
$I_{DD(SPI)}$	SPI supply current(1)	45	
$I_{DD(I2C)}$	I^2C supply current (1)	65	
$I_{DD(ADC1)}$	ADC1 supply current when converting(1)	1000	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 16 MHz. No IC/OC programmed (no I/O pads toggling). Not tested in production.

Table 33. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	External high speed oscillator frequency	-	1	-	16	MHz
R_F	Feedback resistor	-	-	220	-	kΩ
$C^{(1)}$	Recommended load capacitance (2)	-	-	-	20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.6 (stabilized)(3)	mA
		C = 10 pF, f_{OSC} = 16 MHz	-	-	6 (startup) 1.2 (stabilized)(3)	
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}^{(4)}$	Startup time	V_{DD} is stabilized	-	1	-	ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Data based on characterization results, not tested in production.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram

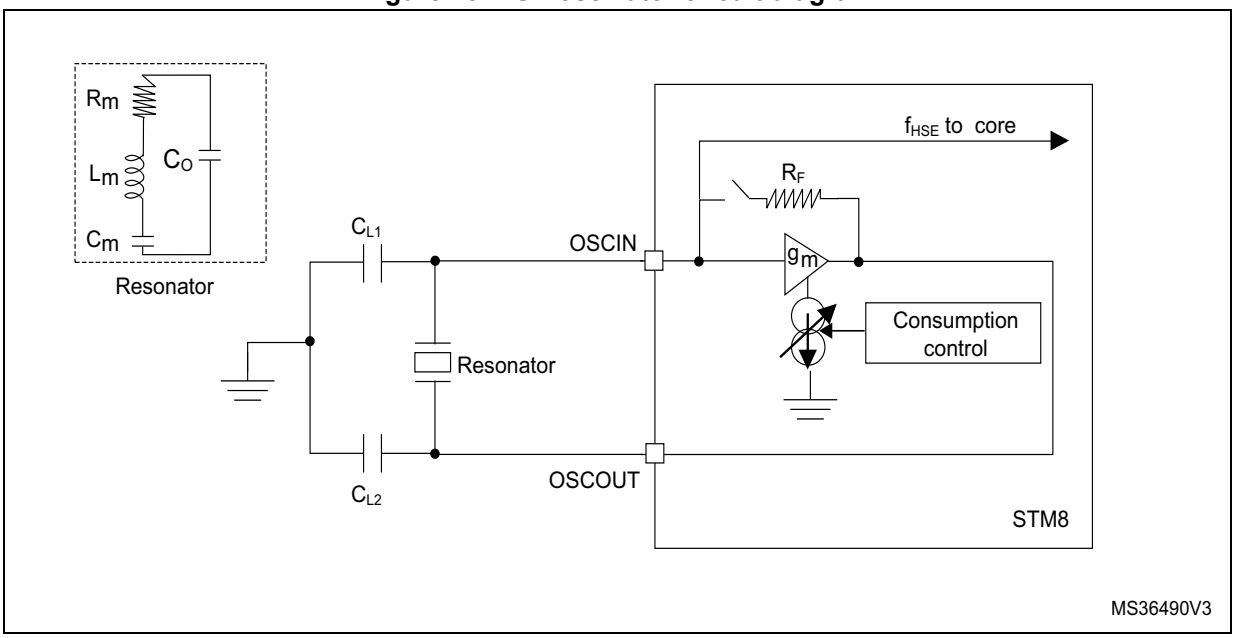


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

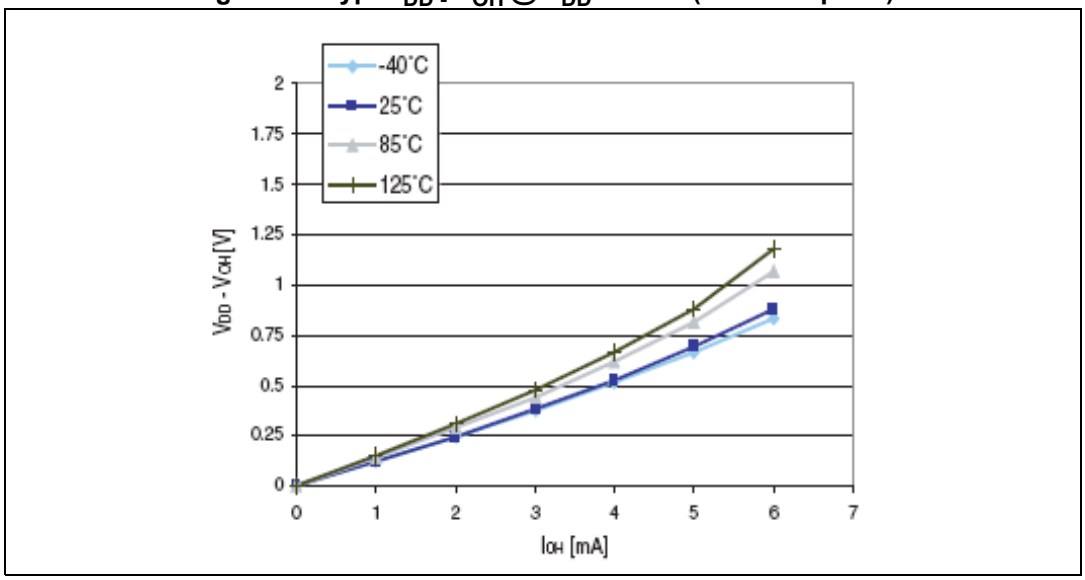
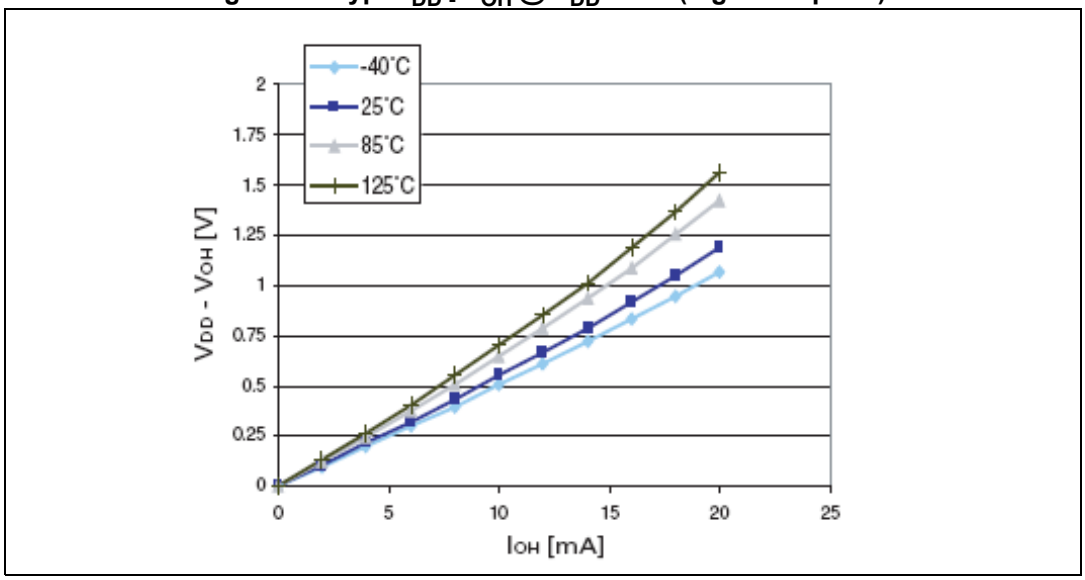


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports)



9.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 48. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-2	2B(1)
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{MASTER} = 16 MHz, conforming to IEC 61000-4-4	4A(1)

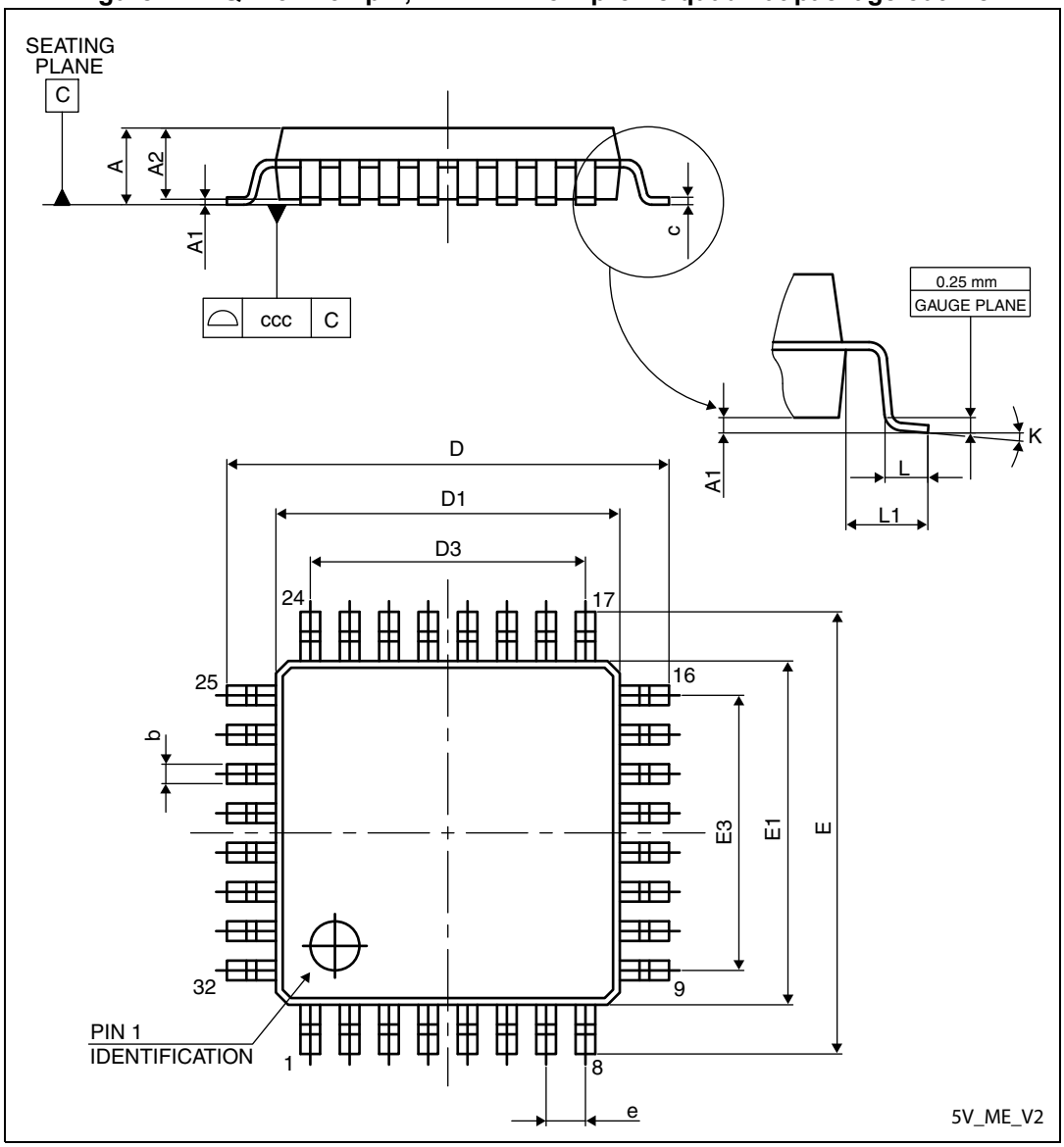
1. Data obtained with HSI clock configuration, after applying HW recommendations described in AN2860 - EMC guidelines for STM8Smicrocontrollers.

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*. ECOPACK® is an ST trademark.

10.1 LQFP32 package information

Figure 44. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline

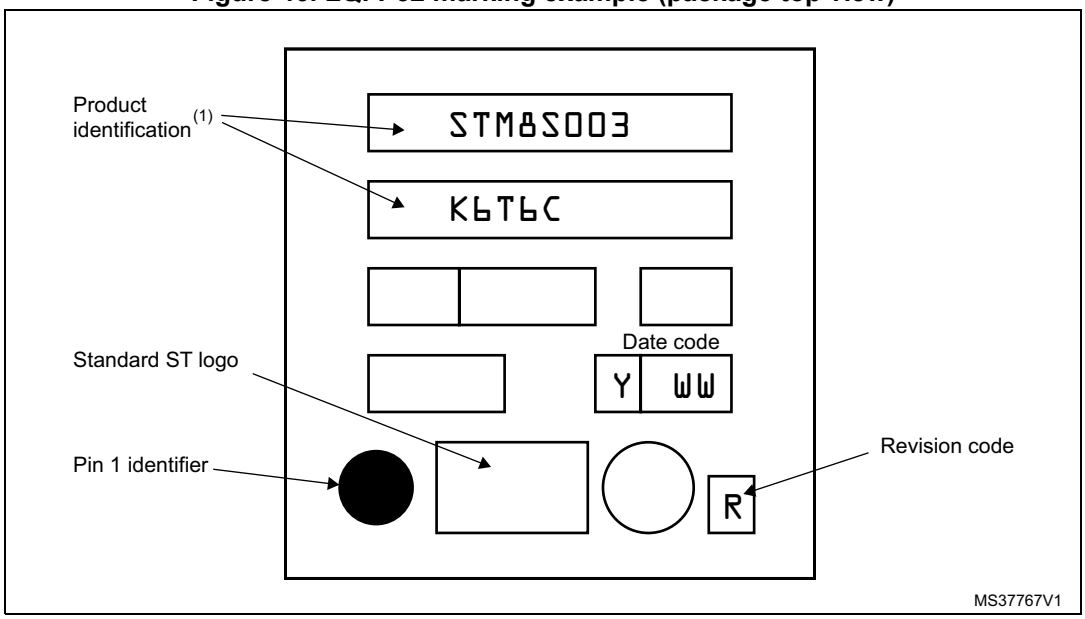


1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 46. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.